Low Voltage Sub-Nanosecond Pulsed Current Driver IC for High-Resolution LIDAR Applications

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***Abstract* — This paper introduces a new low voltage sub-nanosecond monolithic pulsed current driver for light detection and ranging (LIDAR) applications. Unique architecture based on a controlled current source and Vernier activation sequence, combined with a monolithic implementation that allows operation with low input voltage levels, high-resolution pulse width and sub-nanosecond rise and fall times. An on-chip low voltage pulsed driver sub-nanosecond prototype has been implemented in a TS 0.18μm 5V-gated power management process. It incorporates an integrated wide range sesnseFET based current sensor and a rail-to-rail comparator for current regulation. To characterize the avalanche capabilities of the integrated lateral MOSFET power devices required for the driver IC, a separate line of investigation has been carried out. Several lateral diffused MOS (LDMOS) power devices have been custom designed and experimentally evaluated for a life-cycle performance characterization. Post-layout analysis of the power driver IC is in a good agreement with the theoretical predictions. For a 5V input voltage, rise and fall times of the laser pulse light output are on the order of hundreds of picoseconds, with currents up to 5A. To validate the concept of high-resolution pulse width generation and short fall time, a discrete prototype has been constructed and experimentally tested.**

Keywords – Driver IC, LIDAR, laser diode, current pulse, power MOSFET, pulse circuits on-chip, controlled current source IC.

I. INTRODUCTION

Latest boost in development of autonomous vehicles, aerial drones and industrial robots creates a huge demand for a short-range environment-sensing interface [1]-[5]. LIDAR system (Fig. 1a), i.e. *Light Detection and Ranging*, employs an infrared laser for distance measurement, and it is one of the promising methods to be cost-effective, precise and reliable for mobile applications [1]-[6]. Range accuracy and resolution of a LIDAR depend on the rise-time and pulse-width of emitted light pulse, which in turn is a direct function of the current supplied to the laser diode by the driver [1], [4]-[6]. Implementation of a driver with sub-nanosecond rise-time and pulse width poses an extreme challenge due to intrinsic parasitic capacitances and inductances of the components [1], [5]. An ideal setup to drive a laser diode is a current source that generates short pulses with controllable pulse amplitude, width, and rise and fall times (Fig. 1b). In practice however, parasitic components limit the parameters above to a certain boundary, and perhaps more challenging is the relatively slow dynamic performance of high-impedance sources. As a result, the practical implementations of driving low-impedance loads are forced to compromise on some of the parameters.

Some of the earlier methods to drive a laser diode are using a BJT avalanche phenomenon [7]-[9]. While this method potentially results in fast rise times and short pulse width, it requires a number of transistor stages to improve the rise time in every subsequent transistors stage [9]. It also requires extremely high voltages, on the order of hundreds and even a thousand volts to generate an avalanche [7], [9]. Pulse shaping is complex and the efficiency of these methods is rather low, resulting in bulky and excessive heat generating installations, with low pulse repeat frequency (PRF) located within kilohertz scale. An alternative, simpler approach to drive a laser diode is to charge a capacitor to a predefined voltage, and then activate a switch that discharges the capacitor to the laser diode to generate a light pulse [8], [10]. This approach still requires a relatively high voltage, since the current is developed according to the impedance of the laser diode. The most significant drawback of this method is that switching device/s with extremely short transition and delay times are required [8]. Both methods require a special technology for integrated circuit implementation such as an expensive avalanche BJT or a GaN device with proper drive. Another method is to use a high voltage source and an inductor to create a high impedance path, which then forces the current through the laser diode [11]. An alternative concept is to build up a constant current that flows through an inductor and channel the current flow to and from the load using switch assembly. In this approach, the high-impedance characteristics of the inductor are utilized as well as the possibility of rapid transitions – this has been pursued in this study.

The objective of this study is to present a high and rapid current-sourcing power driver for LIDAR applications, as conceptually described in Fig. 1. The power driver features controlled current source and programmed pulse width with sub-nanosecond resolution as well as rapid transitioning (rise and fall times) in the range of less than one nanosecond. It is a further aim of this paper to detail the development process and present a fully monolithic IC implementation of the laser driver. The study also extends to include a wide dynamic range current sensor and a current sourcing stage, as well as

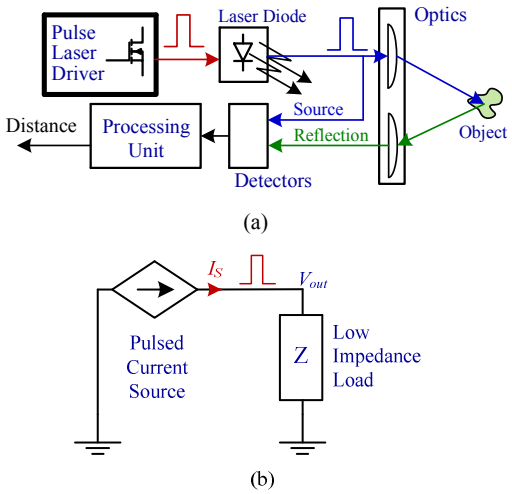

Fig. 1. LIDAR (a) Conceptual system block diagram; (b) Ideal pulse laser diode driver.

development and evaluation of lateral power devices with the ability to sustain high-energy bursts under breakdown conditions.

The rest of the paper is organized as follows: Section II describes the architecture and principle of operation of the new low voltage sub-nanosecond monolithic pulsed current driver. Section III details practical implementation challenges. The IC implementation and monolithic design considerations are delineated in Section IV. Experimental and post-layout results of the pulsed current driver, as well as evaluation and characterization of several LDMOS power devices are reported in Section V. Section VI concludes the paper.

II. Driver Architecture and Principle of Operation

An idealized current driving concept is depicted in Fig. 1b, it shows a controlled pulsed current source that drives a low-impedance load. Unfortunately, ideal current sourcing is not a feasible practice, in particular current source behavior is generated through a device or circuit that mimics high-output impedance within its bandwidth limitations. As a result, rapid transitions that exceed the system bandwidth cannot be obtained using this concept. An alternative approach that hinges on this precursor and inspired by rapid gate drives configurations has been adopted in this study and is depicted in Fig. 2a. It utilizes a regulated constant current source, I_S, followed by a network of power switches, Q_1-Q_3 that act as a current routing network. The operation of the driver is described with the assistance of Fig. 2b that illustrates an idealized gating sequence and load current. The operation is divided into an idle state and two phases: turning on and turning off transitions. In the idle state t_0 (Fig. 2b), the switch Q_1 is on, providing a closed path for the current flow of the source, while the switches Q_2 and Q_3 are turned off. At this point, the system is ready for outputting a current pulse. In the turn on phase t_1, Q_3 is on and Q_1 turns off, the current from the source is routed towards the load, laser diode in this case. The turn off phase t_2 is commenced by simultaneously turning Q_2 on and Q_3 off, causing the inductor current to rapidly route back off the load through Q_2. The use of the additional parallel transistor Q_2, as oppose to operation with Q_1 alone, allows

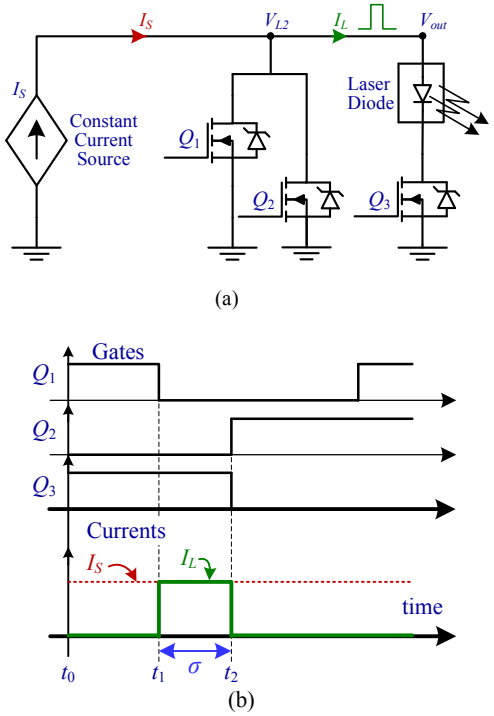

Fig. 2. Driver architecture: (a) Schematics; (b) Switching sequence.

flexible setting of the pulse duration with precise and high time resolution, which cannot be obtained using a single device due to the relatively long intrinsic delays and response time that are involved with high current devices [12]-[14]. The series transistor Q_3, when turned off, increases the impedance of the load path so that the current flow is rapidly halted. As will be detailed in the next section, it also assists to overcome the effect of stray inductances that in the practical case, introduces significant turn off delays.

It should be noted that the gating sequence can be repeated periodically, on demand. For energy saving purposes, between sequence cycles, and depending on the PRF and desired duty cycle of the load, the constant current source may be switched to lower amplitude, or completely turned off.

III. Implementation Challenges

A primary objective of this study is to develop a low-voltage pulse generator to drive LIDAR applications. The power driver is able to provide high-resolution pulse width adjustment, ultra-fast rise and fall times, controllable current amplitude, and it is compatible for IC implementation. There are several challenges associated with the objectives above.

A. Time Delays of Practical Components

The current routing switches are power MOSFETs with unavoidable intrinsic delay between turn on command and the conduction of the MOSFET channel, $t_{d(on)}$. In particular, for power devices that are designed to handle significant current ratings, these delays are on the order of several nanoseconds to some tens of nanoseconds. To achieve time resolution of some 100's picoseconds for the pulse width setting, a Vernier method [14]-[17] has been employed. Two MOSFETs, Q_1 and Q_2 (Fig. 2a), are placed in parallel to each other. One transistor Q_1 is designed and rated for high current whereas the second

transistor Q_2 is designed for speed (can be of smaller size for die optimization). Prior to the turn on phase, MOSFET Q_2 is turned off, while MOSFET Q_1 is left on. At the point t_1 (Fig. 2b) two gate commands that are offset from one another by the width of the pulse σ are generated, turning Q_1 off, and with delay of σ at time t_2, turning Q_2 on. As a result, this Vernier time-skewed command of Q_1 and Q_2, reroutes the current from the source to the load for σ seconds, enabling to achieve a pulse width that is significantly faster than the intrinsic delay of the device's $t_{d(on)}$.

B. *Parasitic Capacitances*

Switch Q_1 is the main path for high constant current generated by the current source. To attain high efficiency, the on state resistance of the switch, $R_{ds,on}$ needs to be as small as possible. Large MOSFET with low $R_{ds,on}$ is preferable. However, this comes at the cost of higher drain-source (output) capacitance of the device, C_{DS}. This capacitance imposes finite slew-rate of the voltage build up across the load, which in turn limits the rise time of the current due to stray inductances in series with the load. To achieve high voltage slew-rates, high currents are required from the source. In addition to limiting the slew-rate, the parasitic capacitance C_{DS}, resonates with parasitic inductance of the load path, setting up the limit for rise time.

To address the challenges described in this section, integrated circuit design is considered in this work. Adjustable design of the power device, and miniaturization of the whole circuit, i.e. on-chip implementation, allows achieving several goals. Reduction of the parasitic components in the current path, i.e. lower C_{DS} and lower parasitic inductances due to the on-chip interconnections. Achieving a better balance between on resistance and switch output capacitance according to the application, and integration of the gate driver with the power switches (Q_1-Q_3) to facilitate higher driving speeds.

C. *Parasitic and Stray Inductances*

Fall time of the current pulse through the laser diode depends on the parasitic inductances and the voltage that is applied to the laser diode during its turn off. In conventional current driving method such as [11], a freewheeling diode is added in parallel to the load to avoid high voltage damage as a result of the residual energy in the stray inductance. However, since the forward voltage of laser diodes is relatively low, if freewheeling is allowed, the turn off time extends and cannot be regulated. It should also be noted that during the turn off period, the current 'tail' circulates energy through the load path, an extremely undesirable scenario for LIDAR applications. To overcome this challenge additional switch Q_3 in the load path is employed (Fig.3 . Switch Q_3 turns off together with the turn on of Q_2 so that any residual current in load path charges the output capacitance of Q_3, which in turn boosts the voltage at the drain of Q_3. Increased voltage at the drain of Q_3 creates a high negative voltage across the parasitic inductance, resulting in rapid turn off time of the load. High voltages at the drain of Q_3 could potentially damage the laser diode. To protect the laser diode from very high reverse voltages, switch Q_3 is selected/designed with reasonable avalanche voltage level, so that at very high currents, the

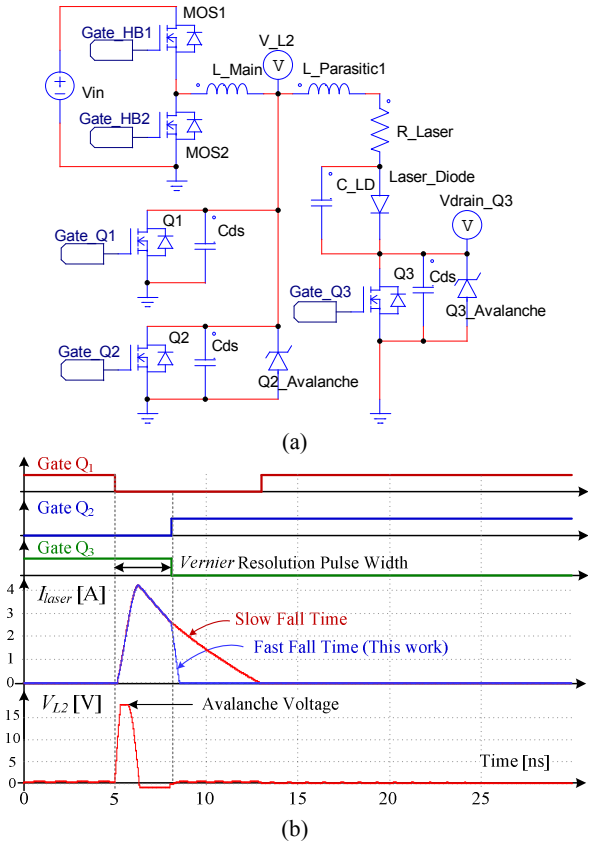

Fig. 3. Simulation test-bench for parasitics evaluation (a) Schematics; (b) Waveforms.

voltage is clamped to some maximum value by the MOSFET, as symbolically represented in the simulation schematics of Fig. 3a with a device named Q_3*_Avalanche*.

Additional effect of parasitic inductances in the presence of current source are instantaneous voltage spikes at the switching nodes. In this circuit, the node prone to this problem is V_{L2} (Fig. 3a), where $L_{Parasitic1}$ avoids an immediate current redirection to the laser diode. The voltage at the node rises as a function of current amplitude and the total node capacitance, and can reach very high values compromising the power switches Q_1 and Q_2. One way to overcome this challenge is to add an auxiliary Zener diode. This solution however, adds an extra parasitic capacitance and in terms of monolithic implementation, requires large silicon area. The solution developed in this study is based on avalanche rated integrated MOSFETs [7], [9], [19], and discussed in detail in Section IV, and represented with the device Q_2*_Avalanche* in Fig. 3a.

A cycle-by-cycle simulation test-bench has been constructed in PSIM (PowerSim, Inc.) (Fig. 3a) to evaluate the solutions for the discussed challenges. Vernier method is employed in the simulation, to generate high-resolution pulse width of the laser current I_{laser} as shown in Fig.3b. In addition, the voltage at node V_{L2} is clamped to the avalanche breakdown voltage, which is predefined in the simulation to 18V, and simulated by a Q_2*_Avalanche* device. An example of a fall time improvement over the conventional case without the additional switch Q_3, is given in the middle plot of Fig. 3b. The fall time of the system shown in this study (blue trace) is much shorter than the conventional freewheeling approach (red trace).

D. Controlled Current Source

One option to implement controlled current source, is a half-bridge synchronous rectifier that feeds an inductance to create high output impedance as shown in Fig. 3a. The series inductance satisfies the high impedance characteristics of the sourcing element. To assure virtually constant current delivery the inductance value is set sufficiently high so that the per-pulse energy that is delivered through the inductor results in a negligibly small discharge, i.e. $LI^2 > E_{dlivered}$. The switching frequency of the rectifier is selected to be sufficiently slower than the width of the load pulse, so that the current source is virtually constant to the pulse generation switches. To successfully control the half-bridge based current source, accurate current sensing over wide range is required, that in this work, has been developed and implemented on-chip.

IV. IC Implementation

The block diagram of a low voltage sub-nanosecond pulsed current driver IC prototype is shown in Fig. 4. The IC integrates power, analog and digital logic on one die. Layout constraints such as adding guard rings and isolation wells between the devices have been employed to reduce coupling noise and undesired holes/electrons injection. An extra care is taken to layout the high current routes. On one hand, wide metal routes potentially result in electromigration, while on the other hand low width metal routes contribute to parasitic resistance. This is solved by keeping the high current routes as short as possible to minimize redundant metallization resistance.

A. Half-Bridge Synchronous Rectifier

A unique feature of the IC driver developed in this study is the low voltage operation, V_{in}=5V, while capable to provide high amplitude current pulses to the load at high PRF. Since the size factor of the design is a valuable merit as well, the half-bridge power-stage is realized by standard 5V CMOS devices. As shown in Fig. 4, the synchronous rectifier includes a pMOS high-side switch and an nMOS low-side switch. The switches have been designed symmetrically with silicon on-resistance of 50mΩ (neglecting the parasitic resistances caused by the metallization and bond wires). The effective gate widths of the switches are $W_{g,pMOS}$ =152,000µm and $W_{g,nMOS}$ =52,800µm. Realizing the high-side switch by a standard pMOS device, enables a ground-referenced gating signal for the half-bridge (with gate voltage swing between 0 to 5V), i.e. neither level shifter nor isolation are required. The latter also implies that the driving stage of the synchronous rectifier can be simplified to a single cascaded buffers chain, conserving both the die-area and power consumption.

B. Power Switches Routing Network

As mentioned in Section III.C, the drain voltage V_{L2} (see Fig. 4) of the switches Q_1 and Q_2 can potentially rise over the rated breakdown voltage of the standard 5V CMOS devices. To guarantee the reliability in terms of overvoltage protection of a high performance power system on-chip, high breakdown voltage LDMOS power devices are used in this study [18]. The transistors Q_1, Q_2 and Q_3 have been implemented

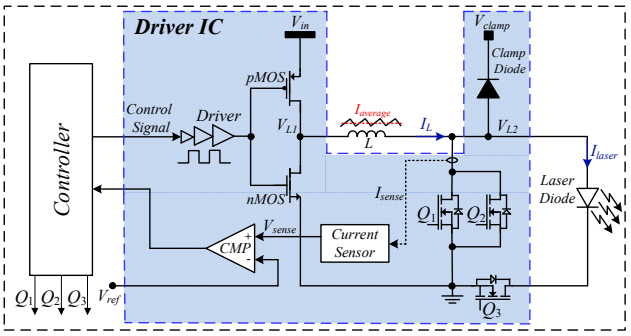

Fig. 4. Block diagram of the implemented IC.

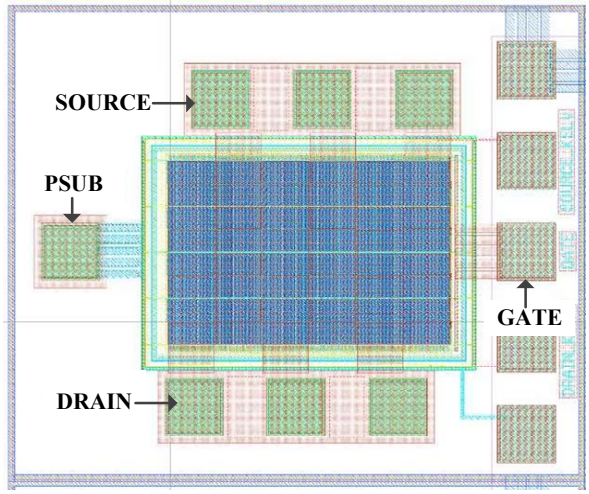

Fig. 5. Layout view of the fabricated basic LDMOS power device.

symmetrically by a high-voltage 5V-gated nLDMOS power device having a gate width of 15,000µm.

Another issue associated with power switches is voltage clamping, which is achieved in this work using an avalanche breakdown effect of the LDMOS. Up to-date, practice with lateral device does not allow exceeding more than half of the rated voltage since it may result in permanent damage of the oxides [19]-[22]. However, since in this study, the power driver configuration relies on the avalanche characteristics of the transistors for reliable execution, repetitive avalanche effect of the lateral devices has been investigated. A batch of three types of LDMOS transistors with different doping levels and oxide thickness have been fabricated and examined through a life-cycle test. The test forces avalanche conditions with various energy levels, at repetition rates of 1MHz over four weeks per device. It has been found that in case that the energy levels applied per avalanche do not exceed the safe operating area of the transistor, the device operates under breakdown conditions without any reliability issues such as drifts, or other oxide memory effects.

The layout of the basic LDMOS device that have been fabricated for avalanche evaluation is shown in Fig. 5, and the results of the experimental evaluation are given in detail in Section V.

To avoid any additional failure risks of the driver IC due to overvoltage at node V_{L2}, and to promote IC compatibility for gate drive application, a monolithic clamping diode rated up to

40V has been integrated as shown in Fig. 4. The diode may be connected to an external clamping voltage rail providing an additional low impedance path, if needed.

C. Current Sensor

One of the enablers for a fully monolithic sub-nanosecond pulsed current driver design is a high-performance current sensing. The sensor is required to provide a relatively accurate reading of the current swing from tens milliamperes to several amperes, under the frequency range of several MHz. There are several approaches for implementing an on-chip current sensor [23]-[26]. The current-sensing in this study is based on a senseFET approach, (Fig. 6) providing a relatively accurate sensing, while maintaining reasonable power consumption [23], [27]-[29]. The current sensor is realized by a matched senseFET LDMOS switch M_{SFET}, with a significantly smaller size than that of the main switch Q_1. To achieve an accurate sensing, equal current densities between the switches are required and assured by equating the operating points of both Q_1 and M_{SFET}. This implies that the same gate drive signal is provided to both Q_1 and M_{SFET}. A trans-impedance amplifier structure [30]-[32] is used to force the same voltage drop at nodes V_{L2} and V_{SFET}. These conditions result in mirroring of the inductor current I_L to the M_{SFET} with a ratio of M as follows:

$$I_{mirror} = I_L \frac{R_{on,Q_1}}{R_{on,M_{SFET}}} = \frac{I_L}{M}, \quad (1)$$

Given the ratio of M:1 between Q_1 and M_{SFET}, the current I_{mirror} is M times smaller than the actual inductor current I_L. To convert the current I_{mirror} to a voltage suitable for the controller operation, the current I_{mirror} is mirrored again to the output of the sensor, and flows through an on-chip poly based resistor R_{sense}. As a result, the voltage V_{sense} across R_{sense} is proportional to inductor current I_L. Sensing signal V_{sense} is expressed as

$$V_{sense} = I_{mirror} R_{sense} = I_L R_{sense} / M, \quad (2)$$

It should be noted that although Q_1 and M_{SFET} are implemented by LDMOS power devices, the sensing circuitry is implemented by standard CMOS devices only, resulting in better overall size and power consumption. The current mirror has been designed in cascode configuration to increase the output resistance reducing the systematic mismatches [33]-[35]. Additionally, the current mirror structure and transistor M_{PT} have been properly sized and matched to guarantee that a sufficient current can be pulled down, such that the amplifier will be able to force the voltages V_{L2} with V_{SFET} to be equal.

D. Rail-to-Rail Comparator

One way to set the current control is by hysteretic-type, reference-based control scheme. The inductor's current is compared to a reference level, triggering the operation of the half-bridge power-stage each time a reference level is crossed. Since the driver IC operates from the range of several milliamperes to several amperes, the comparator should be able to operate at full swing at the input as well as at the output. Thus, a rail-to-rail comparator has been realized as depicted in Fig. 7.

A complementary p-channel and n-channel differential pairs are used at the input stage to accommodate a rail-to-rail

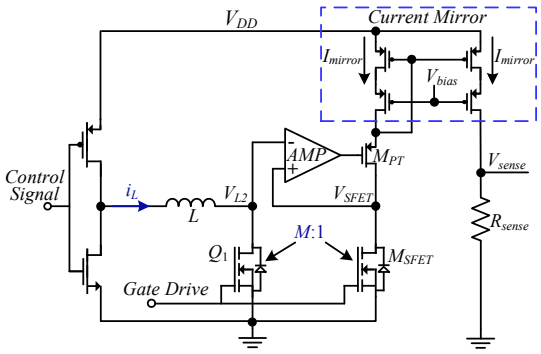

Fig. 6. Current-sensing scheme.

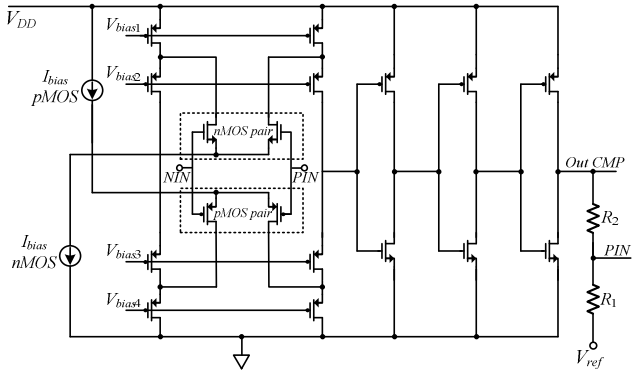

Fig. 7. Simplified schematic of the rail-to-rail comparator.

operation. For low input voltages, the differential pMOS pair is biased, amplifying the voltage difference at the input nodes (*NIN* and *PIN*). In a complementary manner for high input voltages the differential nMOS pair is biased to amplify the input.

Comparator's negative input *NIN* is connected to the sensed signal V_{sense} (from the current sensor), where the positive input *PIN* is connected to V_{ref} through a positive resistive feedback network. The feedback resistors R_2 and R_1 are for a hysteresis arrangement to improve the noise-immunity at the input of the comparator. The hysteresis band has been designed to be 60mV, whereas R_2 and R_1 have been designed to be 836Ω and 68kΩ, respectively. The output stage consists of three cascaded inverters to generate a rail-to-rail output. The post layout measurements of the comparator resulted in total current consumption of 750μA from the 5V supply voltage, at an operating frequency of 2.5MHz. The propagation delay of the comparator was measured to be 8ns for a slew rate of 2.7V/μs.

To guarantee high matching of both differential pairs for process, voltage and temperature variations, the input pairs have been addressed in the layout stage by using common-centroid technique [35]. The active load current mirror structures and bias currents have been implemented using inter digitation technique to guarantee proper matching between the transistors [35]. Additionally, to further increase the noise-immunity of the diff-pairs, isolating guard rings have been added.

V. Experimental and Post-Layout Verification

A low voltage sub-nanosecond pulsed current driver IC has been designed and fabricated in TS 0.18μm 5V-gated power management process. The overall die area is 2.56mm^2, the chip

layout is shown in Fig. 8. In addition, as discussed earlier in Section IV.B, three different LDMOS devices have been custom designed and fabricated for avalanche breakdown evaluation, micrograph of the packaged die is shown in Fig. 9.

The first step of the experimental validation is to characterize the avalanche ratings of the fabricated LDMOS devices. An experimental life-cycle test, which extended to four weeks per device, has been carried out by feeding the devices with a constant current source, while applying short turn off pulses repeated at 1MHz. The clamped voltage of the devices is measured continuously to monitor any potential degradation in the performance. During this experiment a different current amplitudes are applied to validate the change of the drain-to-source voltage, V_{DS} rise time. In terms of slew rate and stable avalanche voltage, the best performance including extreme current cases has been achieved for *LDMOS-2*, as presented in Fig. 10. There, an average avalanche rating of approximately 36V has been measured, for minimum current of 130mA (Fig. 10a) and maximum current of 1.5A (Fig. 10b). The results of the measured slew rates for *LDMOS-2* as a function of the different currents are summarized in Table I.

It should be noted that further increase of the current did not improve the voltage slew rate, this is explained by the limitations of the gate driver and relatively large parasitic inductances in the gate-driving path, present in the experimental setup, built of discrete components. According to the obtained results of the different LDMOS, a new generation of custom designed LDMOS has been constructed in the driver IC prototype, to attain an avalanche voltage of 18V.

The driver IC has been verified with post-layout results using Cadence Spectre simulator, demonstrating a closed-loop operation of the driver architecture. The laser diode has been modeled with forward biasing of 2V including the key parasitic elements as shown in Fig. 11. The control signal for the half-bridge power-stage and gate signals for Q_1-Q_3 generating Vernier sub-resolution pulse width method are produced by a control logic block that has been described through Verilog-A [36].

Fig. 12 depicts post-layout results for a target current I_L=2.5A from a 5V input, whereas the IC connects to an external inductor L=1μH. It can be observed that at steady-state the inductor current settles on the reference level V_{ref} =2.5V at an operating frequency of 2.5MHz (see Fig. 12a), validating the proper operation of the integrated current sensor and comparator. Fig. 12b top plot shows a zoom-in on node V_{L2} and on the laser diode current I_{laser}, with a PRF of 20MHz. Fig. 12b bottom plot is a single pulse zoom-in of the top plot, which shows the current I_{laser} with a pulse width of 3.5ns, and rise and fall times are approximately 900ps and 800ps, respectively. Furthermore, the target avalanche voltage of 18V is achieved.

To validate the principle of operation of the driver architecture and to validate the method to shorten the fall time of the laser diode current, a discrete prototype has been built and tested. A constant current source is followed by a network

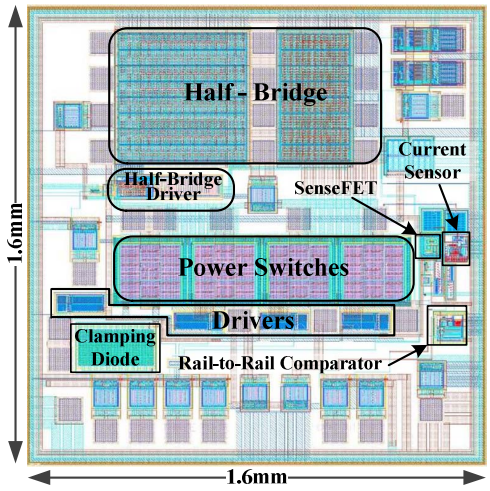

Fig. 8. Chip layout of the fabricated driver IC.

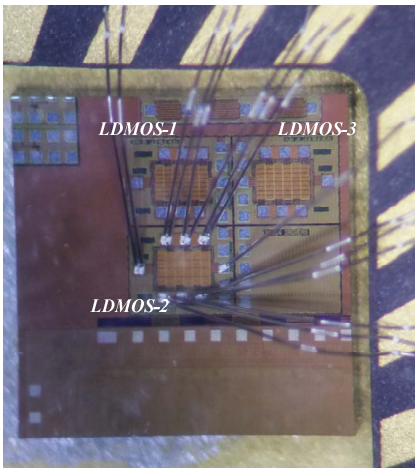

Fig. 9. Die photo of one fabricated LDMOS power devices for avalanche characterization and evaluation.

of power switches according to Fig. 2a. A photodiode from Hamamatsu Photonics (S5972) is used as a photodetector for the experimental setup. Experimental measurements of photodiode output voltage, light output, and anode voltage of the laser diode are shown in Fig. 13. The results without the series switch Q_3 are given in Fig. 13a, as can be seen the fall time of the current approximately 10ns. Fig. 13b shows experimental measurements with the aid of the series switch Q_3, it can be observed that a pulse width of 5ns is obtained, while a more noticeable benefit is that both the rise and fall times are ~2ns, i.e. five times shorter fall time. A small delay could be observed in the experimental results shown in Fig. 13, it is introduced by the optical sensor.

VI. Conclusion

A new low voltage sub-nanosecond monolithic pulsed current driver for LIDAR applications has been presented. Unique combination of driver architecture, based on controlled

Table I – *LDMOS-2* slew rate measurements for different currents

Current	130mA	225mA	400mA	600mA	800mA	1.5A
Turn ON slew rate [GV/sec]	3.3	5.8	14	23	32	33

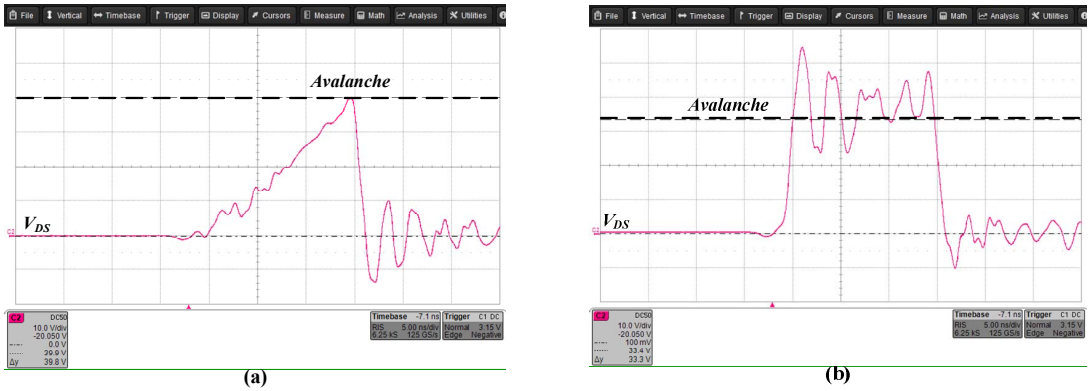

Fig. 10. Slew rate at: (a) 130mA current; (b) 1.5A current; Vertical scale: 10V/div, Horizontal scale: 5ns/div.

current source, and Vernier high-resolution pulse-width activation sequence that are developed in this study, demonstrate robust performance and very short rise and fall times. An on-chip low voltage driver prototype has been designed and implemented in a TS 0.18µm 5V-gated power management process. The IC includes power devices, wide range sensFET based current sensor, and a rail-to-rail comparator for current feedback loop. A characterization of the avalanche capabilities of the integrated lateral MOSFET power devices required for the driver IC has been carried out. Three different LDMOS power devices have been custom designed and experimentally evaluated for a life-cycle performance characterization.

Post-layout analysis of the power driver IC fed with 5V input voltage, demonstrates laser pulse light output rise and fall times on the order of hundreds of picoseconds, and currents of up to 5A, validating the theoretical predictions. A practical laboratory prototype based on discrete components has been constructed and the concepts of high-resolution Vernier pulse width and short fall time has been experimentally tested, demonstrating an excellent agreement with the theory. To the best of the authors' knowledge, this circuit presents the first integrated LIDAR driver that is based on a controlled current source architecture with a pulse width resolution on the order of hundreds of picoseconds.

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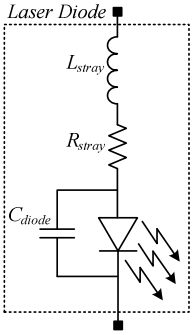

Fig. 11. Laser diode model used for post-layout analysis.

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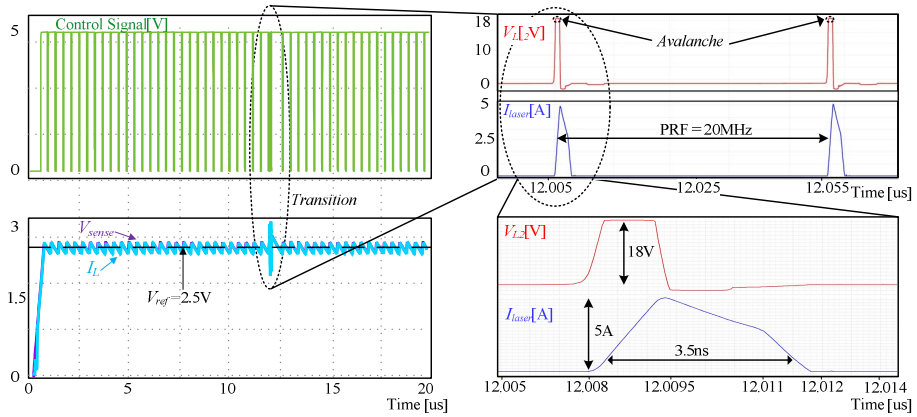

Fig. 12. Post-layout results of the driver IC for I_L=2.5A. (a) Control signal for the half-bridge and sensing signal from the current sensor; (b) Zoom-in on post-layout results of the voltage node V_{L2} and on the laser diode current I_{laser}.

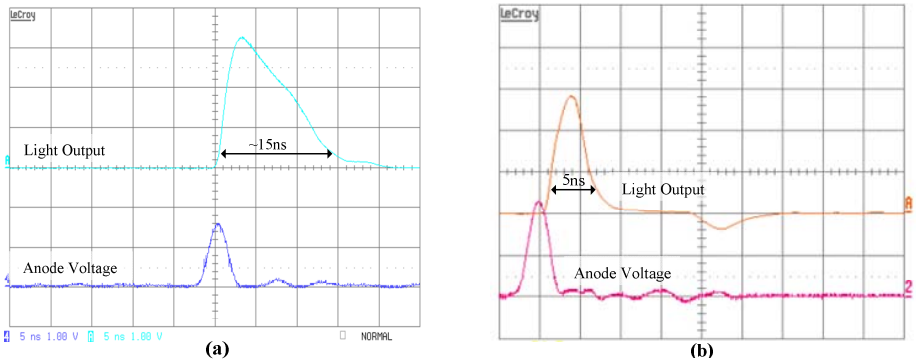

Fig. 13. Discrete prototype experimental results: (a) without series switch Q_3, (b) with series switch Q_3. Light output (top trace), laser diode anode voltage (bottom trace). Horizontal scale 1V/div, Vertical scale 5ns/div.

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