Merged PWM-Resonant Converter for Direct Panel to Grid-Level Conversion in Localized PV Energy Harvesting

Or Kirshenboim, *Student Member, IEEE*, Guy Sovik, Dor Yairi, and Mor Mordechai Peretz, *Member, IEEE*

The Center for Power Electronics and Mixed-Signal IC
Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev
P.O. Box 653, Beer-Sheva, 8410501 Israel
orkir@post.bgu.ac.il sovik@post.bgu.ac.il doryai@post.bgu.ac.il morp@ee.bgu.ac.il
http://www.ee.bgu.ac.il/~pemic

***Abstract*- This paper presents a merged PWM-resonant dc-dc converter topology for localized PV energy harvesting. The topology merges a boost as the front-end converter and a series-resonant converter as the back-end converter. The two converters are merged by sharing the switches for their operation while they are decoupled by separating their control variables. Merging of the converters is facilitated by a control scheme that can change both the duty-ratio and switching frequency. The boost converter provides the ability to obtain MPPT control by changing the duty-ratio and the series-resonant converter allows for output voltage regulation by controlling the switching frequency. By merging the two power stages, high efficiency is achieved due to zero-voltage switching that is obtained on both switches and the component count is reduced. Full analysis and characteristics of the converter are detailed, and experimental results using a 400V/240W prototype validate its operation and features.**

I. INTRODUCTION

Among the variety of grid-interactive photovoltaic (PV) systems, microinverters are an attractive option for modular and independent energy harvester. This concept disregards any mismatches among PV modules, provides possibility of individual PV-module optimal design, and allows independent maximum power point tracking (MPPT) [1], [2]. In many cases a PV microinverter is supplied by a single solar panel, with typical low voltage in the range of 20-30V. In such cases a high voltage-conversion ratio converter is required to produce the output's ac voltage [1]-[3]. Therefore, it is conventionally achieved by two-stage conversion; a dc-dc converter cascaded by an inverter is the most common arrangement for such systems [4]-[10].

The front-end converter that connects to the PV module steps up the voltage to a level compatible with the grid while performing MPPT. This compromises the output voltage regulation capability of the converter since the two control objectives that are distinctly different simultaneously super-impose on the control command. In the majority of applications, the tasks are separated for two decoupled converters. One facilitates MPPT and another regulates the voltage [11]-[12].

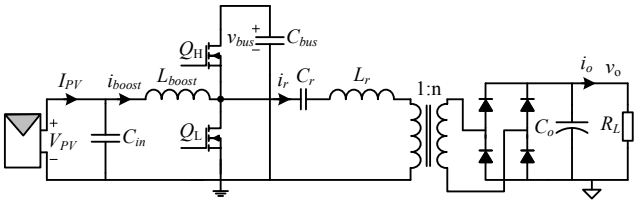

Fig. 1. Merged PWM-Resonant converter (MPRC) topology.

The idea of one converter performing a specific task and another converter obtaining a different objective has been investigated and implemented in variety of applications such as: power-factor correction applications and LED drivers [13]-[18]. An interesting and attractive solution is to integrate two stages into one, as suggested in [19]-[25]. Merging of the two stages contributes to achieve better power processing characteristics, high efficiency, lower requirements from the DC link capacitor and reduced components count at the cost of slightly more complex control. This has been pursued in this study.

The objective of this study is to introduce a merged PWM-resonant dc-dc converter (MPRC) topology with high voltage gain for localized PV energy harvesting. The topology, shown in Fig. 1, combines a boost front-end with a series-resonant converter as the back-end. Merging is facilitated by sharing the MOSFETs for the operation of both converters. Full decoupling is achieved by separation of the control variables and objectives. The boost front-end provides the ability to obtain MPPT and is controlled by variation of the duty-ratio whereas the series-resonant converter regulates the output voltage by changing the switching frequency. In addition, the operation of the converter provides ZVS on both MOSFETs, significantly lowers the power loss and maintains high efficiency.

The rest of the paper is organized as follows: Section II describes the MPRC topology and details its principle of

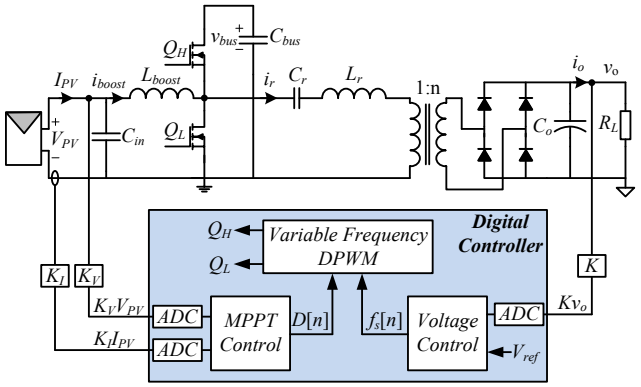

Fig. 2. Control scheme of the MPRC topology.

operation and control scheme. Primary characteristics and simulation results of the MPRC are provided in Section III. Experimental results using a MPRC prototype are given in Section IV. Section V concludes the paper.

II. Merged PWM-Resonant Converter Topology

The high conversion ratio required for converting a single PV module voltage to the input voltage of a grid-tied inverter can be achieved by variety of ways. For example, a series-resonant converter (SRC) with high turns ratio of its transformer. However, to obtain both regulated output voltage *and* operation at the maximum power point of the PV module, another degree of freedom is required. A possible solution to overcome this challenge is by adding a boost converter between the input and the resonant converter in order to be able to operate at the MPP while regulating the output voltage. However, this reduces the efficiency and results in higher components count.

The MPRC power stage, shown in Fig. 1, combines a synchronous boost converter that is connected to the PV module and a SRC that is connected to the input of the inverter (marked as the load R_L). Three components are common for the stages, these are the power MOSFETs (Q_H and Q_L) and the bus capacitor C_{bus}. Using this circuit, several key benefits are simultaneously obtained, the use of only two switches (instead of four) and single bootstrapped gate driver lowers the components count and cost. In addition, although the boost operates in CCM, the resonant nature of the SRC provides the ability to have zero-voltage switching (ZVS) on both MOSFETs, significantly reducing the switching losses.

The key principle in the operation of the MPRC is in the control scheme. The boost's control variable is the switches' duty-ratio D while the SRC control variable is their switching frequency f_s. These two control variables can be simultaneously controlled without having one control variable affecting the other. Therefore, it allows the boost and SRC to use common switching devices for their operation, as shown in Fig. 2. It should be noted that since the current waveforms of the two converters have different shapes, a small bus capacitor is still required. The bus capacitor voltage v_{bus} is unregulated and may vary depending on the type of MPPT algorithm that is realized.

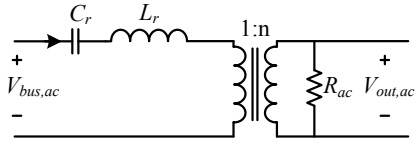

Fig. 3. Equivalent circuit of the SRC under FHA.

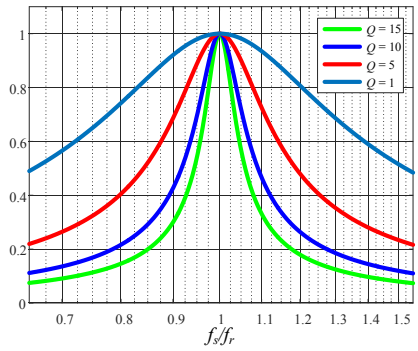

Fig. 4. Normalized voltage gain of the SRC.

Assuming that under variations of the switching frequency the boost inductor current ripple does not exceed the CCM boundary, the voltage gain of the boost converter depend on the duty-ratio and is given by:

$$M_{boost}(D)=\frac{V_{bus}}{V_{PV}}=\frac{1}{1-D} \quad (1)$$

where D is the duty-ratio of Q_L.

The SRC's equivalent circuit under first harmonic approximation (FHA) is depicted in Fig. 3 and its normalized voltage gain is given by:

$$M_{SRC}(f_s,D)=\frac{V_{out,ac}}{V_{bus,ac}}=\frac{\sin(\pi D)}{1+j\dfrac{n^2\sqrt{L_r/C_r}}{R_{ac}}\left(\dfrac{f_s}{f_r}-\dfrac{f_r}{f_s}\right)} \quad (2)$$

where $V_{bus,ac}$ and $V_{out,ac}$ are the first harmonics at the input and output ports of the SRC, respectively, as illustrated in Fig. 3. f_r is the resonance frequency given by $1/2\pi\sqrt{L_rC_r}$ and R_{ac} is the resistance seen at the transformer's secondary side, given by $8R_L/\pi^2$ [26] and n is the transformer's turns ratio. Fig. 4 depicts the expression in (2) for different values of the quality factor Q and D=0.5. It can also be seen in (2) that M_{SRC} depends on D for the amplitude value. However, since changes of the duty command are driven from the MPPT controller which varies D much slower compared to the change of f_s by the frequency controller, D can be considered constant for the dynamic response of M_{SRC}. A point that needs to be emphasized is that the resonant tank of the SRC should be designed so that Q is relatively high (typically higher than 5) for any load condition. This is necessary so that the current waveforms at the SRC is sinusoidal, even for cases that D is different from 0.5 as in conventional SRC operation.

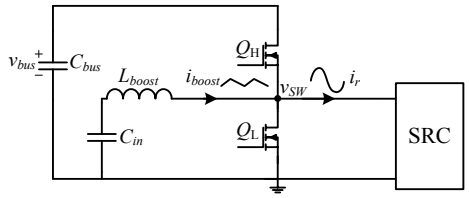

Fig. 5. Current waveforms at the switching node of the MPRC.

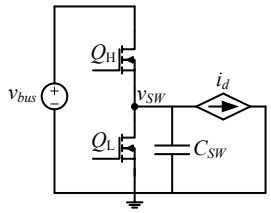

Fig. 6. Equivalent circuit for the dead-time period.

The total voltage gain of the MPRC is the multiplication of (1) and (2):

$$M_{MPRC}(D,f_s)=\frac{V_{out}}{V_{PV}}=M_{boost}M_{SRC} \quad . \tag{3}$$

The SRC stage can be considered with varying input voltage and regulated output voltage (by frequency control regulation). This varying input voltage is v_{bus} which depends only on D, governed by the MPPT algorithm. Since the output voltage needs to be regulated, in case that the MPPT controller increases D and M_{boost} is increased, the frequency controller increases f_s so that M_{SRC} is decreased and the output voltage remains constant. This way any input power can be extracted by controlling D while the output voltage is maintained regulated by controlling f_s.

III. Primary Characteristics of the MPRC Topology

Due to the inherent differences between currents waveforms of the boost and the SRC, achieving ZVS on both high and low-side switches is not immediate. The boost current that enters the switching node is triangular with a DC offset due to the CCM operation, while the SRC current at the switching node is sinusoidal, as illustrated in Fig. 5. A necessary condition to achieve ZVS on Q_H is that the current difference $i_d = i_r - i_{boost}$ is negative at its turn-on instance, i.e. $i_d < 0$. To achieve ZVS on Q_L it is necessary that the current difference will be positive at its turn-on instance, i.e. $i_d > 0$. Assuming a converter efficiency of η, a duty-ratio of 0.5 and under FHA, the resonant current i_r at the switching instances can be approximated to

$$i_r=\pm\left|\frac{\pi\eta V_{PV}I_{PV}}{2nV_{out}}\sin(\phi)\right| , \tag{4}$$

where ϕ is given by

$$\phi=\tan^{-1}\left(\frac{n^2\sqrt{L_r/C_r}}{R_{ac}}\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)\right) , \tag{5}$$

And the expression for i_{boost} is given by

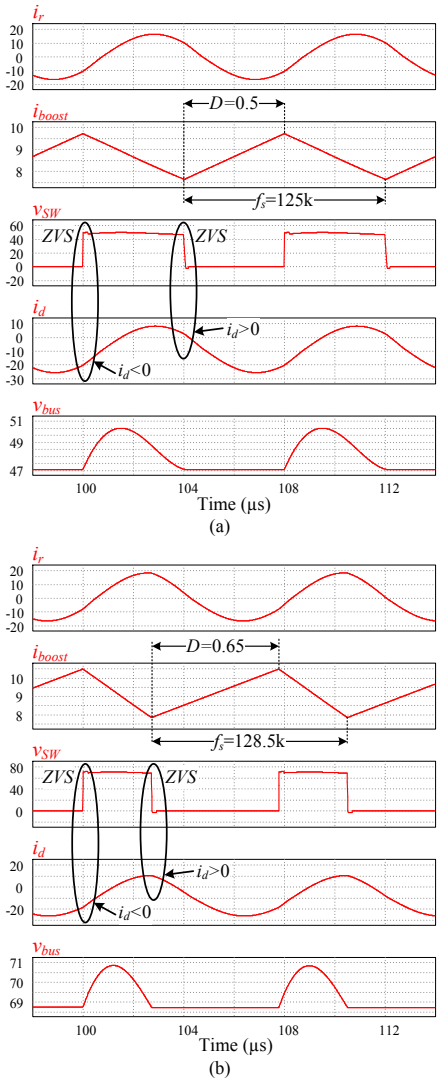

Fig. 7. Simulation waveforms of the MPRC for (a) D=0.5, (b) D=0.65.

$$i_{boost}=I_{PV}\pm\frac{V_{PV}}{4Lf_s} \quad . \tag{6}$$

Using (4)-(6) the necessary condition to obtain ZVS on Q_H is

$$-\left|\frac{\pi\eta V_{PV}I_{PV}}{2nV_{out}}\sin(\phi)\right|-I_{PV}-\frac{V_{PV}}{4Lf_s}<0 \quad , \tag{7}$$

whereas the necessary condition to obtain ZVS on Q_L is

$$\left|\frac{\pi\eta V_{PV}I_{PV}}{2nV_{out}}\sin(\phi)\right|-I_{PV}+\frac{V_{PV}}{4Lf_s}>0 \quad . \tag{8}$$

It should be noted that condition (7) holds for any case since at this point the actual current direction of both currents is always directed toward the switching node. The more strict condition is (8) since one current is entering the switching node and the other is pointed out of it. Taking into account the capacitance between the switching node and ground C_{SW} and approximating i_d to a constant current source and v_{bus} to a voltage source for the dead-

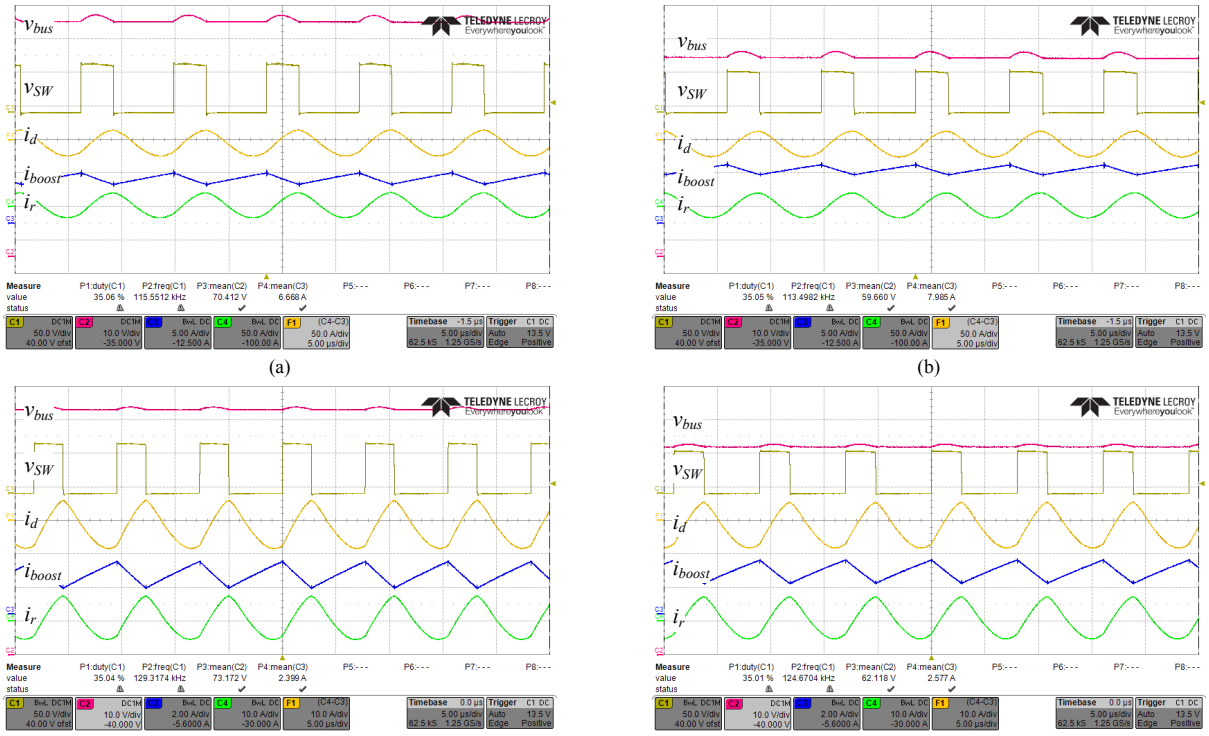

Fig. 8. Experimental waveforms of the MPRC experimental prototype in four different load and input voltage conditions for D=0.65: (a) V_{PV}=26.3V, R_{Load}=1KΩ, (b) V_{PV}=22.1V, R_{Load}=1KΩ, (c) V_{PV}=26.3V, R_{Load}=3KΩ, (d) V_{PV}=22.1V, R_{Load}=3KΩ. Signals from top to bottom: C2 – Bus capacitor voltage v_{bus}; C1 – Switching node v_{SW}; F1 – Current difference i_d; C3 – Boost current i_{boost}; C4 – Resonant current i_r. Time scale is 5µs/div.

time period t_{dt} as depicted in Fig. 6, the following conditions are sufficient to guarantee full ZVS on both MOSFETs:

$$ZVS\ on\ Q_H:\ t_{dt} > \frac{2C_{SW}V_{PV}}{\left|\frac{\pi\eta V_{PV}I_{PV}}{2nV_{out}}\sin(\phi)\right| + I_{PV} + \frac{V_{PV}}{4Lf_s}} > 0$$

$$ZVS\ on\ Q_L:\ t_{dt} > \frac{2C_{SW}V_{PV}}{\left|\frac{\pi\eta V_{PV}I_{PV}}{2nV_{out}}\sin(\phi)\right| - I_{PV} + \frac{V_{PV}}{4Lf_s}} > 0 \quad (9)$$

Fig. 7 shows simulation waveforms of the MPRC (obtained using PSIM) for two situations where D=0.5 and D=0.65. It can be observed that for both cases the two different duty-ratio values result in different values of v_{bus} and therefore it is compensated by the voltage regulation controller that changes the switching frequency accordingly to maintain the output voltage constant. In the case that D=0.5 v_{bus} is lower, and therefore f_s is lower as well. Also depicted is i_d, and it can be observed that for the two cases both conditions (7) and (8) hold at the switching instances and ZVS is obtained.

IV. Experimental Results

To validate the operation of the MPRC topology, a 400V/240W experimental prototype was built and tested. The components' parameters and values are detailed in Table I. The converter was digitally controlled by a dsPIC33F series microcontroller from Microchip [27], sensing the PV module's voltage and current for MPPT control and the output voltage for regulation, as illustrated in Fig. 2.

TABLE I – Experimental Prototype's Parameters

Component	*Value / Type*
Input voltage V_{PV}	20-30 V
Output voltage V_o	400 V
Bus capacitance C_{bus}	6 µF
Output capacitor C_o	10 µF
Transformer's turns ratio 1:n	1:26
Resonant frequency f_r	~107 KHz
Resonant capacitance C_r	110 nF
Resonant inductance L_r	20 µH
Boost inductor L_{boost}	100 µH
Power MOSFETs Q_H and Q_L	100V, 6.6mΩ

Fig. 8 and Fig. 9 show the experimental MPRC's prototype waveforms for various load, input voltage and duty-ratios conditions. The shown waveforms are the switching node, bus voltage, resonant current, boost current and their difference. Fig. 8 shows the case where the duty-ratio is D=0.65. It can be observed that the change between different input voltages [Fig. 8(a) vs. Fig. 8(b) and Fig. 8(c) vs. Fig. 8(d)] changes the bus voltage and to regulate the output voltage to 400V this change is compensated by variation of the switching frequency. For example, when V_{PV} is 26.3V the bus voltage is 73.1V and the resultant switching frequency is 129.3KHz [see Fig. 8(c)], and when V_{PV} is reduced to 22.1V the bus voltage is 62.1V and the switching frequency is lowered to 124.6KHz [see Fig. 8(d)] to keep the output voltage regulated. It can also be observed that the average input current (the mean of i_{boost}) is increased when the

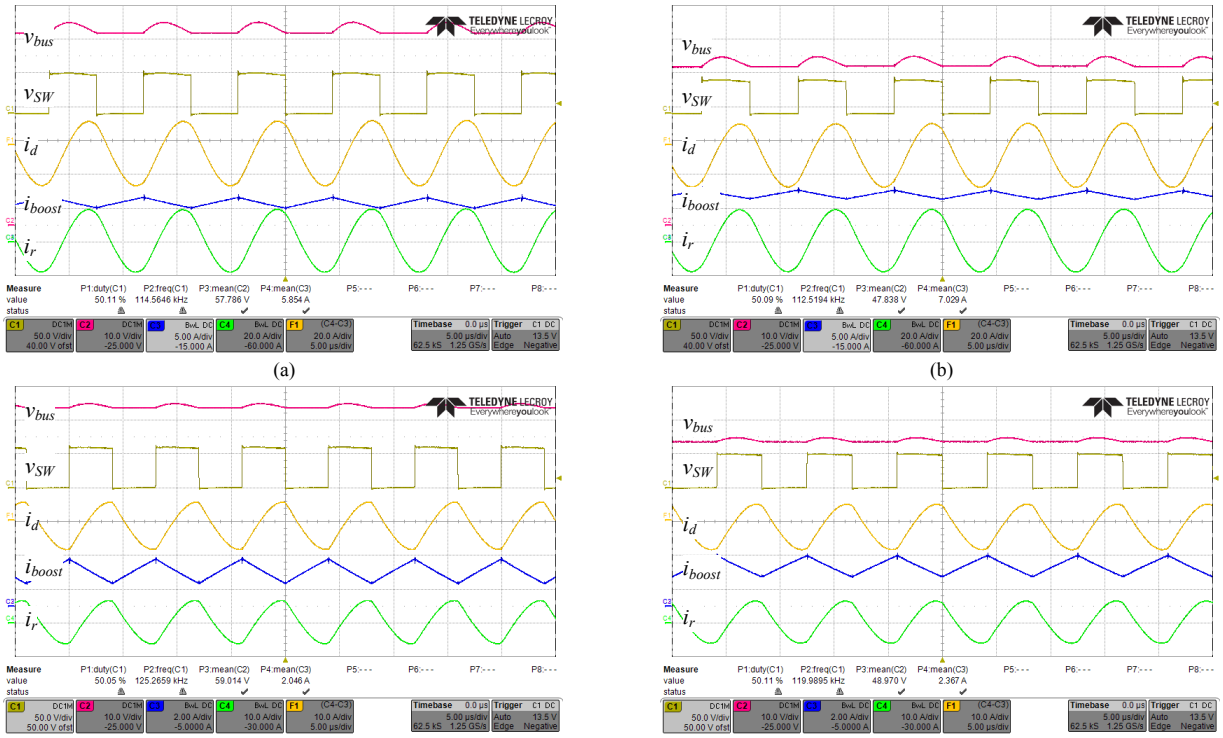

Fig. 9. Experimental waveforms of the MPRC experimental prototype in four different load and input voltage conditions for D=0.5: (a) V_{PV}=29.9V, R_{Load}=1KΩ, (b) V_{PV}=25.6V, R_{Load}=1KΩ, (c) V_{PV}=29.9V, R_{Load}=3KΩ, (d) V_{PV}=25.6V, R_{Load}=3KΩ. Signals from top to bottom: C2 – Bus capacitor voltage v_{bus}; C1 – Switching node v_{SW}; F1 – Current difference i_d; C3 – Boost current i_{boost}; C4 – Resonant current i_r. Time scale is 5µs/div.

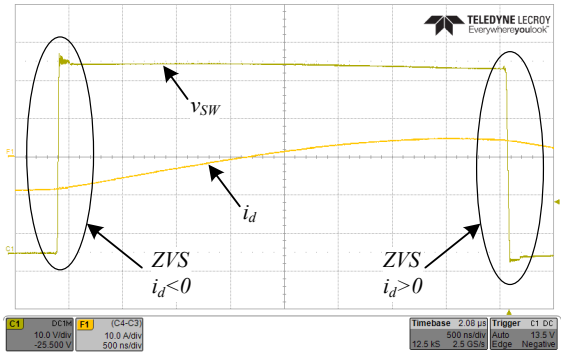

Fig. 10. Experimental waveforms of the MPRC experimental prototype demonstrating ZVS transitions. C1 – Switching node v_{SW} (10V/div); F1 – Current difference i_d (10A/div). Time scale is 500ns/div.

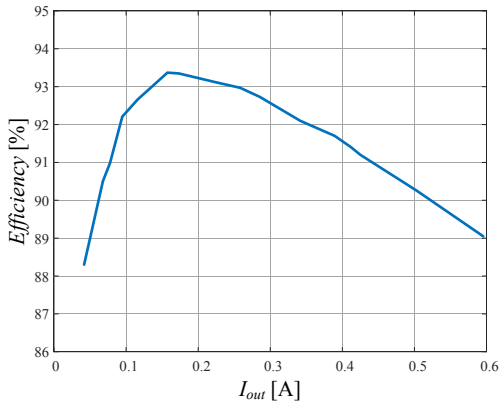

Fig. 11. Efficiency measurements of the experimental prototype.

input voltage is decreased, this is since the load in this case is kept constant. In addition, different load values results in different frequency variation for the same input voltages due to different Q values as expected by the analysis from Section II. When the input voltage changes from 26.3V to 22.1V the switching frequency is reduced from 115.5KHz to 113.5KHz for a 160W load [high Q – see Fig. 8(a) and Fig. 8(b)] while for a 53W load the switching frequency reduces from 129.3KHz to 124.6KHz [low Q – see Fig. 8(c) and Fig. 8(d)].

Fig. 9 presents the same waveforms for a duty-ratio of D=0.5 with different input voltages. Here the bus voltage values are lower and therefore the switching frequency values are lower compared with the cases shown in Fig. 8. In all the presented cases ZVS is obtained on both MOSFETs due to the polarity of i_d at the switching instance. Fig. 10 zooms in on the switching instances and depicts the switching node voltage v_{SW} and the current difference i_d to better view the ZVS on the MOSFETs. It can be observed that when Q_L is turned off i_d <0 which charges the capacitance during the commutation and the body diode of Q_H conducts before it is turned on. The opposite transition occurs when Q_H is turned off and i_d>0 which discharges the capacitance and the body diode of Q_L conducts until it is turned on, as predicted by the analysis from Section III. Efficiency measurements of the converter are provided in Fig. 11. As can be observed, the peak efficiency is 93.4% and above 89% for most of the load range.

V. CONCLUSION

A merged PWM-resonant dc-dc converter topology for localized PV energy harvesting has been presented in this study. The topology combines a boost front-end converter and a series-resonant converter as the back-end converter by using common power switches. Merging of the stages is facilitated by a controller that controls both the duty-ratio and switching frequency, allowing for both MPPT control and output voltage regulation while obtaining high efficiency due to ZVS on both high and low side MOSFETs. Steady-state analysis and primary characteristics have been presented, showing the benefits of the converter. The experimental results of the converter are in excellent agreement with the theoretical analysis, showing promising power processing characteristics and making the converter an attractive candidate for localized PV energy harvesting.

ACKNOWLEDGEMENTS

This research was supported by the Pazi foundation.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[2] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[3] R. Wai and W. Wang, "Grid-connected photovoltaic generation system," *IEEE Trans. Circuits Syst.-I*, vol. 55, no. 3, pp. 953–963, Apr. 2008.

[4] M. Andersen and B. Alvsten, "200W low cost module integrated utility interface for modular photovoltaic energy systems," in *Proc. IEEEIECON*, 1995, pp. 572–577.

[5] A. Lohner, T. Meyer, and A. Nagel, "A new panel-integratable inverter concept for grid-connected photovoltaic systems," in *Proc. IEEE Int. Symp. Ind. Electron.,* 1996, pp. 827–831.

[6] D. C. Martins and R. Demonti, "Grid connected PV system using two energy processing stages," in *Proc. IEEE Photovolt. Spec. Conf.*, 2002, pp. 1649–1652.

[7] T. Shimizu, K.Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[8] N. Kasa, T. Iida, and L. Chen, "Flyback inverter controlled by sensorless current MPPT for photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1145–1152, Aug. 2005.

[9] Q. Li and P. Wolfs, "A current fed two-inductor boost converter with an integrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 309–321, Jan. 2007.

[10] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 2003, pp. 1183–1190.

[11] S.-Y. Tseng, H.-Y. Wang, "A photovoltaic power system using a high step-up converter for DC load applications," *Energies 2013*, 6, pp. 1068-1100.

[12] T. V. Thang, A. Ahmed, C. I. Kim and J. H. Park, "Flexible system architecture of stand-alone PV power generation with energy storage device," *IEEE Trans. Energy Conv.*, vol. 30, no. 4, pp. 1386-1396, Dec. 2015.

[13] L. Yu and J. Yang, "The topologies of white LED lamps' power drivers," in Proc. International Conference on Power Electronics Systems and Applications, PESA-2009.

[14] Y. Zhongming, F. Greenfeld, and L. Zhixiang, "A topology study of single-phase offline AC/DC converters for high brightness white LED lighting with power factor pre-regulation and brightness dimmable," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, 2008, pp. 1961–1967.

[15] X. Qu, S.-C. Wong, and C. K. Tse, "Ballast for independent control of multiple LED lamps," in *Proc. IEEE Energy Convers. Conf. Expo. (ECCE)*, Sep. 2009, pp. 2821 - 2826.

[16] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in AC/DC power supplies for LED lightings", *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399-1408, May 2009.

[17] C.-L. Kuo, T.-J. Liang, K.-H. Chen, and J.-F. Chen, "Design and implementation of high frequency AC-LED driver with digital dimming," in *Proc. IEEE Int. Symp. Circuit Syst.,* 2010, pp. 3713–3716.

[18] J. Qian, "*Advanced single-stage power factor correction techniques*", Ph.D. dissertation, Virginia Polytechnic Institute and State University, 1997.

[19] M. Madigan, R. Erickson, and E. Ismail, "Integrated high quality rectifier-regulators," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 1992, pp. 1043–1051.

[20] T. F. Wu, T. H. Yu, and Y. H. Chang, "A systematic illustration of the applications of grafted converter trees," in *Proc. IEEE Ind. Electron., Contr., Instrum. Conf. (IECON)*, 1996, pp. 1536–1541.

[21] J. M. Alonso, A. J. Calleja, J. Ribas, E. L. Corominas, and M. Rico-Secades, "Analysis and design of a novel single-stage high-power-factor electronic ballast based on integrated buck half-bridge resonant inverter," *IEEE Trans. Power Electron*., vol. 19, no. 2, pp. 550–559, Mar. 2004.

[22] J. M. Alonso, M. A. Dalla Costa, and C. Ordiz, "Integrated buck–flyback converter as a high-power-factor off-line power supply," *IEEE Trans. Ind. Electron*., vol. 55, no. 3, pp. 1090–1100, Mar. 2008.

[23] M. A. Dalla Costa, J. M. Alonso, J. Cardesín, J. García, and D. G. Lamar, "A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal Halide lamps," *IEEE Trans. Ind. Electron*., vol. 55, no. 3, pp. 1112–1122, Mar. 2008.

[24] M. M. Peretz, N. Goyal, M. Chen, and A. Prodic, "A merged-stage high efficiency high power factor HB-LED driver without electrolytic capacitor". *International Exhibition and Conference for Power Electronics, PCIM-2012*, 357-364. Nuremberg, Germany, 2012.

[25] Y.-T. Huang, C.-H. Li, Y.-M. Chen, and Y.-P. Tong, "Analysis and design of a single-stage buck-type AC-DC adaptor," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APE)*, Mar. 2017, pp. 16-22.

[26] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in *IEEE Trans. Ind. Electron*., vol. 3, no. 2, pp. 174-182, Apr 1988.

[27] Microchip Technology, Inc., "16-bit digital signal controllers with high-speed PWM, ADC, and comparators" DS70318F, 2012.