Enhanced Performance Fully-Synthesizable ΣΔ ADC for Efficient Digital Voltage-Mode Control

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***Abstract*— This paper introduces a new approach for sigma-delta based analog to digital converter (SDADC) with enhanced performance suitable for digital voltage regulation. The new ADC increases the number of digital representations of the sampled signal per conversion cycle, for the same oversampling clock frequency. This advantage also translates to reduced power consumption for the same conversion rate since slower clock can be employed to obtain similar conversion rate. An all-digital, fully-synthesizable realization of the new architecture sets it as an attractive candidate for many digital application platforms, ranging from housekeeping and monitoring, and even as the primary ADC for the compensation loop. High accuracy and fast effective conversion rate have been verified through simulation and experiments, demonstrating wide range of sampled voltages with less than 1% error for wide operation range. An experimental closed-loop operation on a voltage-mode (VM) buck converter, with the digital voltage loop implemented on FPGA, demonstrates superior operation over a conventional SD operation. The digital controller core including the new SDADC have been also implemented as IC by an automated synthesis process and place-and route tools in a 0.18µm 5V CMOS process resulting in effective silicon area of 0.07mm^2.**

Keywords - Sigma-delta modulator, integrated circuit, analog-digital converter, voltage-mode control, digital control.

I. INTRODUCTION

Sigma-Delta modulators and converters are major enablers of the digital technology ramp up dating back to the late 1980s. The appearance of low-cost and reliable means to translate continuous-time signals onto the sample-data domain revolutionized the field of low and medium frequency range signal processing and in particular the audio world [1]-[4]. Nowadays, the availability of simple and efficient interface from the analog world to the digital hardware is still extremely important in all fields of electronics. In particular for power management, where fast performance with reasonable cost is critical, analog implementation of the controller core is still predominant [5], [6]. In the last decade or so there has been a significant progress in digital power management thanks to the development of dedicated hardware that is tailored to its unique needs [7]-[12]. With the integration of digital technology, the power management system transforms as well. Now comprises design flexibility, scalability, and upgrade options; communication and power quality logging; plug-and-play operation; and of course, improved performance.

Since a typical digital compensation loop must have at least comparable dynamics to its analog precursor, a high-performance peripherals are essential, i.e., the digital PWM (DPWM) and ADC [7], [8], [11], [12]. Conversion of 10bit word within 100ns is a common requirement to accommodate switching frequencies in the range of 300kHz (where the control bandwidth is approximately $1/6f_s$). As a consequence, high-performance ADCs such as pipeline or successive approximation are employed [13], [14]. Since Sigma-Delta analog to digital converters (SDADC) are operated through oversampling concept and require very high speed clock, in the order of 100s MHz to generate comparable conversion rate, they are typically avoided for compensation purposes and mostly used for slower tasks such as housekeeping and user interfaces. On the other hand, the very simple hardware of a SDADC is an attractive feature, which should be further pursued.

A typical voltage-mode (VM) compensation loop for switch-mode power supply (SMPS), as illustrated for a buck converter in Fig. 1, operates on the basis of one sample per cycle to regulate the average value of the output voltage and fully utilize the correction rate (switching frequency) of the loop. For a compensator based on conventional SDADC, this calls for oversampling clock of at least 2^n time the switching frequency (where n is the number of ADC bits) with a bit stream of similar size. However, since convergence of a linear control scheme takes several switching cycles, this strict requirement are eased in this study by trading some of the accuracy with faster reading. The data of the long string, for precision, is generated out of lower resolution, shorter strings. Information of the output voltage status continuously updates the loop, and since it is of shorter duration, the potential deviation in the output voltage is lower which agrees with the momentary lower resolution reading. In this way, with minor hardware additions, a SDADC can be

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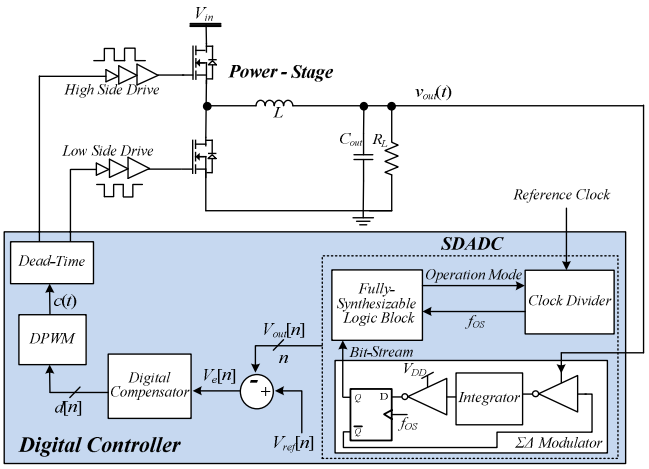


Fig. 1. Simplified schematic diagram of digital voltage-mode control loop for a buck converter utilizing the SDADC.

considered as an attractive candidate for various tasks, and even for core control in digital voltage regulation.

The objective of this study is therefore to introduce a modified architecture for Sigma-Delta Analog to Digital Conversion. The SDADC digitizes wide range of sampled voltages with high accuracy and wide dynamic range to capture fast variations without sacrificing precision. These attributes make the new ADC suitable in digital voltage regulation and in particular for applications of Adaptive Voltage Scaling (AVS). It is a further objective of this study to delineate a simple all-digital voltage feedback loop, as in Fig. 1, implemented on IC.

The rest of the paper is organized as follows: section II details the architecture of the SDADC and covers its principle of operation. The all-digital voltage loop compensation is described section III. Section IV covers issues of practical implementation, including design flow, IC layout, and silicon size estimation. Experimental system implementation and validation are presented in section V. Section VI concludes the paper.

II. Enhanced Performance SDADC Principle of Operation

The principle of operation of the modified SDADC is described in comparison to a conventional SDADC and with the aid of Figs. 2 and 3, which show a conceptual block diagram of the modified conversion scheme and high-level operation flowchart, respectively. It is assumed here that a first-order SD modulator is used to generate a bit stream with average value that is proportional to the sampled signal $v_{out}(t)$. A detailed full-digital realization of the modulator will be described later in the practical implementation, Section IV. To produce an n-bit digital value representation of the sampled signal, the amount of 'ones' of the bit-stream is stored in a main n-bit counter (see Fig. 2). The counter acts as a sinc Low-Pass Filter (LPF), and resets at pre-determined intervals to perform decimation [1]-[3].

The sampled output voltage $v_{out}(t)$ is translated to a digital representation $v_{out}[n]$. In the SDADC of this study, the sampled signal is updated several times, with coarser resolution, during a full conversion cycle. These mid-cycle time updates are generated by a state machine combined with a digital logic block, and pre-defined according to the overall number of bits of the counter. An n-bit register holds the most recent digital value of the sampled signal, and is updated throughout the conversion cycle in both mid-cycle and full-cycle update points. Thus, a coarse result of the sampled signal is generated, which is refined through the conversion cycle, and after 2^n over sampling clock cycles (f_{OS}) a full resolution digital representation of $v_{out}[n]$ is obtained.

Typically SDADCs are designed to sample signals that do not vary between two reset operations of the counter [1], [3], [15]. The concept employed in this study is designed to accurately track the sampled signal variations between two or more reset events of the counter, exploiting the SDADC advantages without the penalty of slower dynamics, power consumption, or increased design efforts [1]-[4], [15]-[18]. This enables to update the result more than a single time per conversion cycle and fast digitizing of the sampled signal with high accuracy. Effectively, wider dynamic range is achieved even for fast variations without sacrificing precision.

For the modulator operation (detailed in Section IV), given 2^n clocks cycles since the latest reset operation the value of the reconstructed continuous-time equivalent for the digitization process, $V_{out}^*(t)$, is found with respect to the main counter's value, and can be expressed as

$$v_{out}^{\ *}(t) = V_{ref}\frac{2^n}{CNTR_n}, \qquad (1)$$

where V_{ref} is the reference value for the modulation process, and CTR_n is the counter's value for a given number of bits. For intermediate updates during the conversion cycle (referred throughout the text as *mid-cycle updates*), the effective number of bits is smaller than n and the reconstructed value is scaled and normalized according to the bits difference as follows

$$\frac{2^n}{CNTR_{mid}} = \frac{2^m}{CNTR_n} \quad \Rightarrow \; CNTR_{mid} = \frac{2^n}{2^m}CNTR_n \quad , \qquad (2)$$

where m is the number of bits during mid-cycle update command and CTR_{mid} is the digital representation of the sampled signal at mid-cycle update points.

One of the drawbacks of typical SDADCs is power consumption due to relatively high operating frequencies to assure Nyquist sampling criterion [1], [3], [15]. Employing the modified operation concept, power saving option is enabled. This is achieved by setting the SDADC into two operation modes: (a) transient detection, (b) steady-state. For transient event or any other sudden potential variation of the sampled signal, the system operates at high clock. The latter combined with mid-cycle updates, results in fast responses of both the SDADC and the overall control loop. However, if the system is in steady-state mode, i.e. a system governor detects minor deviations of the conversion output along a predetermined number of cycles, the clock frequency can be lowered. This reduces the power consumption without

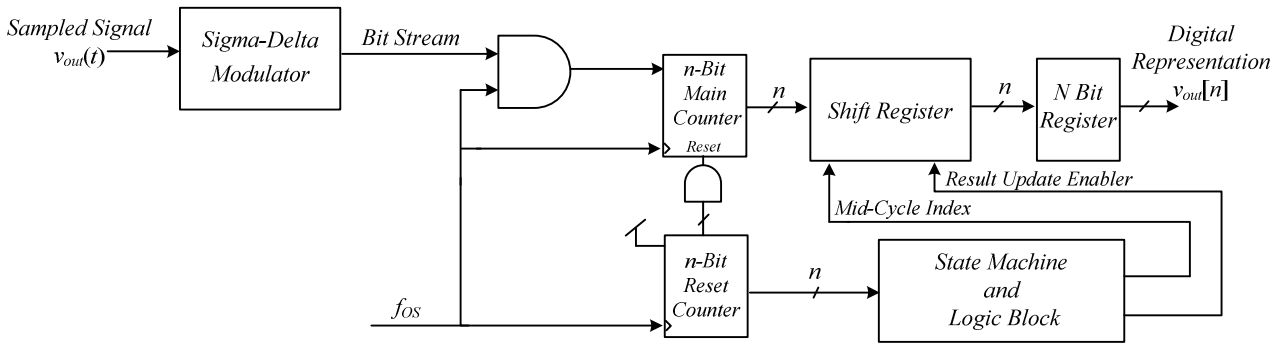


Fig. 2. Simplified block diagram of the new architecture for SDADC.

sacrificing precision of the sampled signal. The selection procedure between the modes is illustrated in the flowchart of Fig. 3.

III. All Digital Voltage Loop Compensation

Digital VM compensation for SMPS is a simple and streamlined approach [12], [19], [20], to regulate the output voltage to a desired reference voltage over wide range of operating conditions. Since a single state variable (the output voltage) is controlled, it requires moderate hardware complexity. It should be noted however, that the dynamic performance of this control scheme may not suffice all applications and therefore an additional current loop is added which may be either analog [5], [21] or digital [7]-[10]. In the context of this study, which aims to introduce a new ADC architecture, a voltage feedback loop has been selected as a demonstrative tool for simplicity.

A conceptual block diagram of a typical single-loop VM control scheme is depicted in Fig. 4. As can be seen, the output voltage $v_{out}(t)$ (or a scaled version of it) is sensed and then sampled by the SDADC, to produce a digital representation of the output voltage value $v_{out}[n]$. Then allows, the sampled voltage is compared with a digital reference value, and results in an error signal $v_e[n]$. The error signal is passed through a digital compensator (either PI or PID), which then updates the DPWM unit to generate drive signals for the low and high side power switches of the converter. $K_{A/D}$ and K_{DPWM} are the gains of the SDADC and DPWM, respectively. The power stage that has been selected for evaluation is a buck converter, with idealized control-to-output transfer function $G_{vd}(s)$ that can be expressed as [7], [11]

$$G_{vd}(s)=\frac{V_{in}}{\frac{s^2}{\omega_0^2}+\frac{s}{\omega_0 Q}+1}\ ;\ \omega_0=\sqrt{\frac{1}{LC_{out}}},\ Q=\sqrt{\frac{C_{out}}{L}}R_L\ . \quad (3)$$

Fig. 5 shows a conceptual timing diagram for an output voltage variation for both a conventional SDADC and the enhanced performance SDADC developed in this study. Output voltage regulation is achieved by properly adjusting the duty-ratio command $d[n]$ as a function of the generated error signal $v_e[n]$. Fig. 5a shows that the conventional SDADC is being updated only at the end a of a full conversion cycle, resulting in relatively slow closed-loop

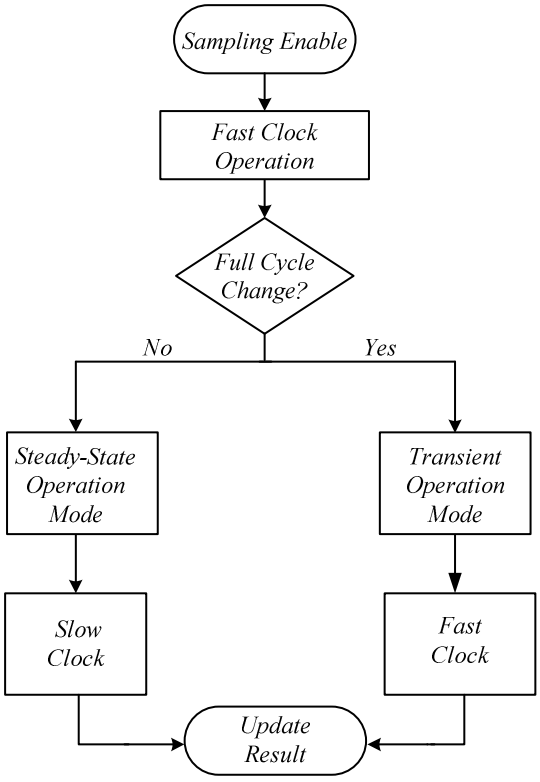


Fig. 3. High-level flowchart of the clock selection mode.

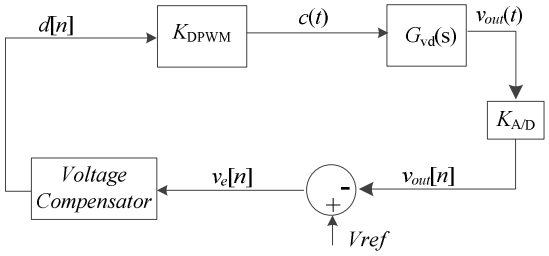


Fig. 4. Block diagram of the digital VM control system.

response due to limited sampling and correction rate. For similar settings of the digital hardware (i.e., clock speed and calculation hardware), the new SDADC employs coarse corrections throughout the operation cycle at shorter intervals, which provides more information on the voltage, but with lower resolution than the end-of-cycle result. Consequently, the output voltage is corrected faster, and

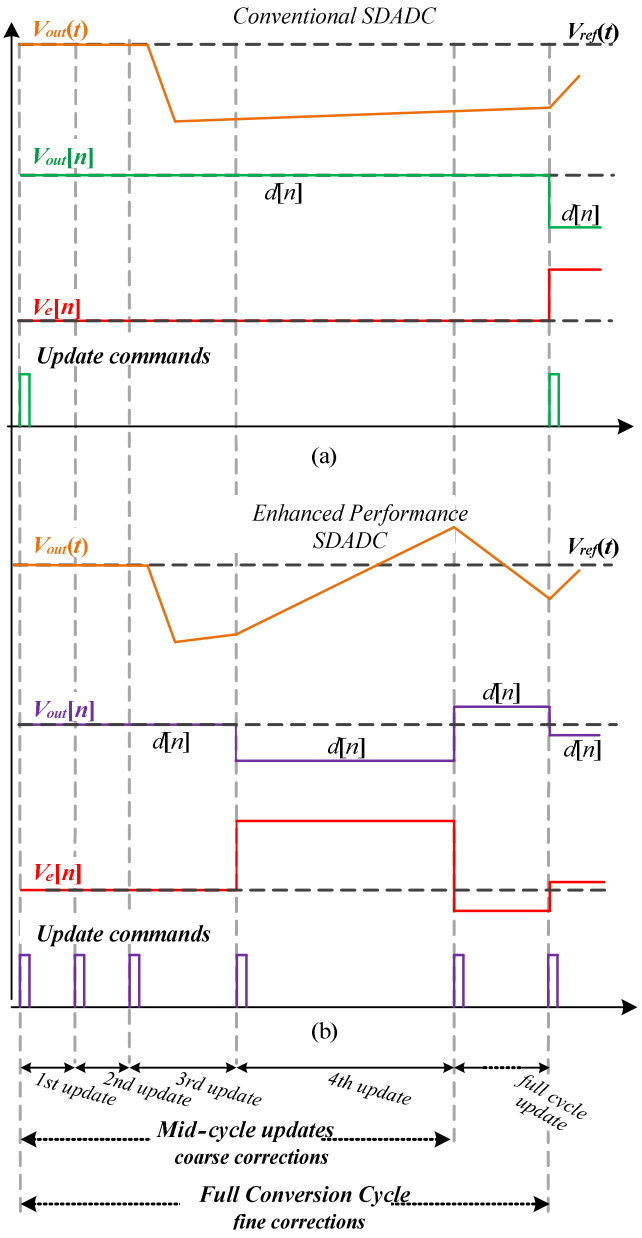


Fig. 5. Conceptual timing sequence of duty-ratio updates in response to voltage reference change: (a) Conventional SDADC, (b) Enhanced performance.

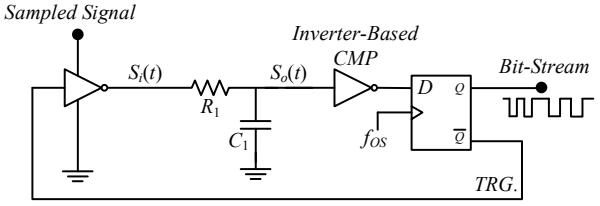


Fig. 6. SDADC modulator schematic circuit.

convergence to desired reference value V_{ref} is obtained. While information of coarser resolution apparently distorts the tracking capability of the loop, the information flows in a faster rate and as a result compensates for lower accuracy. It should be noted that, the ratio between the effective sampling rate and resolution is virtually identical for samples at mid-cycle as the one obtained at the end of the longer cycle. The faster and more accurate response of the new SDADC implies that higher effective bandwidth of the closed-loop system is achieved for the same hardware complexity and running frequency of the controller.

IV. Practical Implementation

Practical implementation and design considerations of the SDADC's main functional units are discussed in this section. Since this design is ultimately IC oriented, with automatic tools, emphasis is made to reduce the use of analog peripherals.

A. Modulator Stage

Conventional SD modulators comprise difference amplifier followed by an integrator and comparator [2], [4], [15]. In this study, a digital-oriented approach is considered and is shown in Fig. 6. An inverter is used as the modulator's front-end, with the sensed signal as the high logic level (supply) of the inverter. This can be implemented in variety of ways such as variable supply [22], [23], current-starved inverter [24], [25], or digital differentiator or comparator [20]. To reduce circuit complexity, the integrator is realized by a simple RC network (may be double RC for further size reduction) with a corner frequency of at least one order of magnitude lower than the clock frequency. The one-bit quantizer is also realized by another inverter, where the threshold value of the inverter is the comparison [20]. Finally, the quantized value is held for a clock cycle using a D flip-flop which also drives the first inverter data path. Utilizing this configuration of Fig. 6, a simple and efficient SD modulator with streamlined IC implementation is facilitated.

Fig. 7 depicts an example for steady-state operation of the SDADC's modulator. The modulator produces the bit-stream such that the voltage at node $S_o(t)$ is toggled around the threshold voltage of inverter-based comparator V_{th}. This is achieved by feedback link between the flip-flop and the input sampling inverter operation as can be seen in Fig. 7, resulting in a square signal $S_i(t)$ between 0 and the sampled voltage value, which charges/discharges the integrator's output. The relationship between the sampled signal and the generated bit-stream is according to (1), and it is a primary concept for the new SDADC architecture.

B. Operation Mode Detector

As discussed in Section II, the SDADC in this study has a clock selection mechanism to reduce the power consumption at steady-state operation. An algorithm to identify transitions is described with the aid of Figs. 8 and 9. Every four sequential full cycle results are held in the registers as shown in Fig. 8. The results are continuously compared and as long as they are equal, the system operates at a lower clock frequency. For a case that the comparison block detects a single change between the four sequential results, the system immediately switches to fast clock mode with rapid transitions to obtain the most accurate value of the

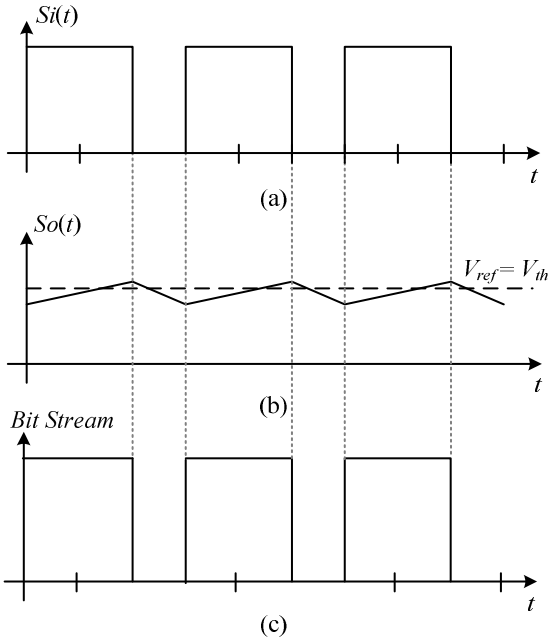


Fig. 7. Typical steady-state sampling operation of the SDADC. (a) Output voltage of the sampling inverter (b) Integrator's output (c) Generated bit-stream representing the sampled signal.

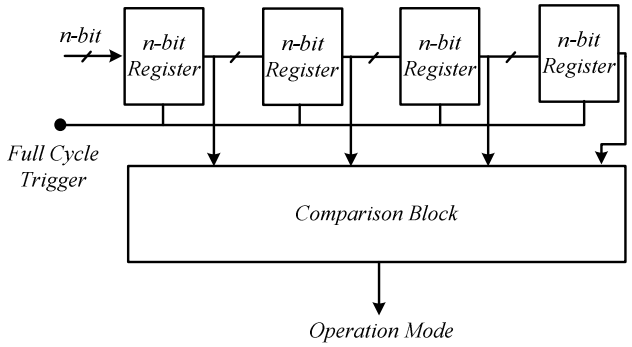


Fig. 8. Simplified block diagram for operation mode decision making algorithm.

sampled signal. It should be noted that full cycle conversion is generated when the reset counter (see Fig. 2) reaches 2^n-1.

Fig. 9 shows simulation example demonstrating the clock selection algorithm for a 10-bit SDADC to an input signal that periodically toggles between 3V to 4V. As can be seen, while the sampled voltage is constant the reset counter increases with slow clock, however, whenever transition occurs, the reset counter rapidly increases with the aid of the fast clock within in the system.

C. IC Implementation

The realization of the digital control in this study primarily relies on an automated digital implementation flow, using vendor's standard cells. The IC implementation of the voltage control loop is described through three main steps. In the first step, digital custom design is carried out for SDADC's modulation stage and inverter-based comparator. Second, the controller's units including the SDADC core are described in HDL as standalone units. This is done for simplicity of the verification and functionality simulations.

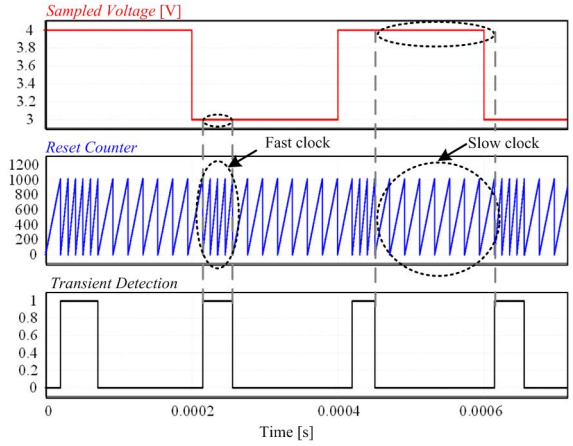


Fig. 9. Simulation results of clock selection entering and exiting power saving mode.

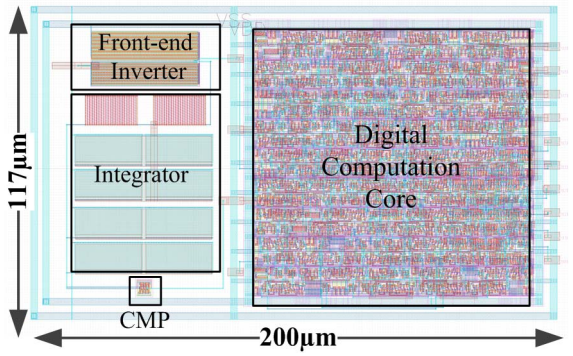


Fig. 10. SDADC layout 200µm x 117µm.

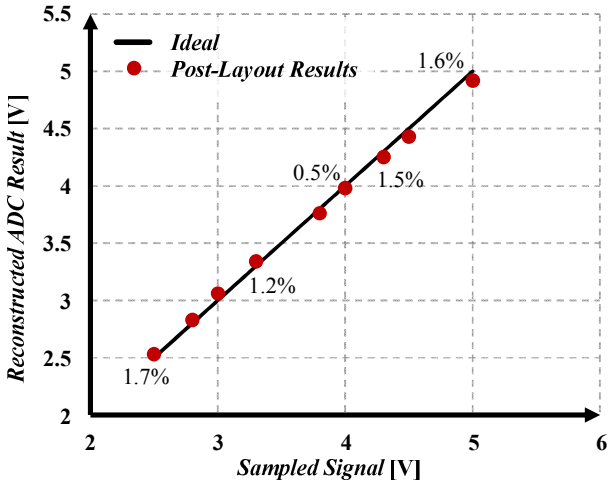


Fig. 11. Accuracy post-layout results of the SDADC for wide range of sampled voltages.

Then, each unit is translated to hardware using synthesis and timing verification tools into an optimized gate-level representation, given a set of design constraints. The silicon layout for each unit is generated by an automated place-and-route process. In the third step, all units are integrated together onto the higher hierarchy of the digital controller, and the resultant overall die-area is 0.07mm^2 (with 5V CMOS realization). It should be emphasized however, that

for higher density assignment or scaled technology (such as deeper sub-micron process), the area and power consumption can be further reduced.

The implemented SDADC comprises of a double RC network based integrator, front-end custom designed inverter, standard cell based inverter that functions as a comparator, and a digital computation core that operates at f_{OS}=6.25MHz. Fig. 10 shows the SDADC layout which results in effective silicon area of 0.023mm^2, which is significantly compact in comparison to other ADCs with similar performance. Fig. 11 depicts post-layout results of the SDADC for a wide range of sampled voltages to characterize and quantify the sampling accuracy. As can be seen, for sampled voltages in the range of 2.5-to-5V the obtained sampling error is less than 1.7%.

V. Simulation Case Study

Using the analysis and observations from the previous sections, set of simulations have been conducted in PSIM (PowerSim, Inc.) to verify the effectiveness of the new enhanced performance SDADC in a closed-loop operation of a buck converter as illustrated in Fig. 1.

Fig. 12 shows the response to reference changes of the buck converter operating in closed loop for different settings of the operating frequency, output capacitor and inductor. In the first case (Fig. 12a) a conventional SDADC is examined, and switching frequency f_{sw1} is as follows

$$f_{sw1} = \frac{f_{os}}{2^n}, \tag{4}$$

where f_{os} is the oversampling clock frequency.

In the second test case (Fig. 12b), the new SDADC is used, demonstrating improved performance compared to the results obtained in Fig. 12a. It should be noted that for this evaluation, the values for inductance and capacitance in the buck converter remain the same. Since the effective sampling frequency is higher when utilizing the new approach, the switching frequency may exceed to f_{sw2}, which can be expressed as:

$$f_{sw2} = \frac{f_{os}}{\frac{m}{2}}, \tag{5}$$

and the ratio between f_{sw2} and f_{sw1}, using (4) can be written as

$$\frac{f_{sw2}}{f_{sw1}} = \frac{2^n}{2^m} \Rightarrow f_{sw2} = \frac{2^n}{2^m} f_{sw1} \quad . \tag{6}$$

As can be observed from Fig. 12b, the new loop settings that allowed increased switching frequency f_{sw2}, result in improved convergence of the output voltage to the new steady-state value.

The advantage of utilizing the new SDADC becomes widely apparent in response of the third test case of Fig. 12c. Since higher switching frequency is allowed, the inductance and capacitance values may be adjusted to satisfy similar ripple constraints as in Fig. 12a. This implies that effectively higher bandwidth can be achieved, resulting in better dynamic response (for the same control hardware) and lower

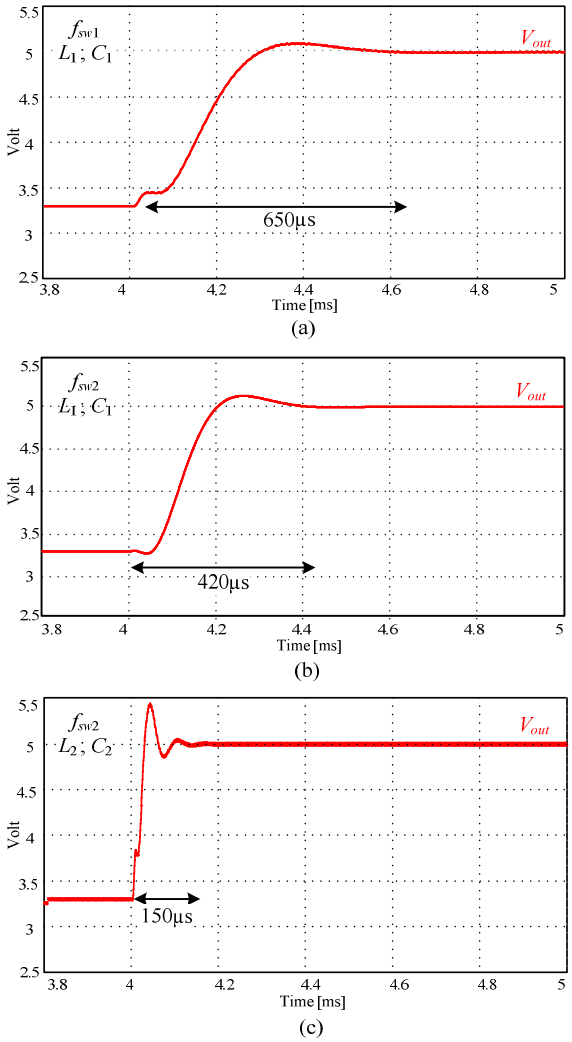


Fig. 12. Response to changes in the reference voltage for the digitally controlled buck converter: (a) Conventional SDADC with sampling frequency f_{sw1}, (b) New SDADC with sampling frequency f_{sw}, and same components (c) New SDADC adjusted f_{sw} and components.

volume of the overall solution. For the example of Fig. 12c, the frequency is adjusted $f_{sw2}=4f_{sw1}$ so that same target ripples as in Fig. 12a.the output capacitor C_2 and inductor L_2 can be calculated as

$$C_2 = \left(\frac{f_{sw1}}{f_{sw2}}\right)^2 C_1 \quad ; \quad L_2 = \frac{f_{sw1}}{f_{sw2}} L_1 \,. \tag{7}$$

Fig. 13 shows a simulation closed-loop VM operation of a buck converter with L=75µH and C_{out}=100µF at operating frequency 100 KHz For a step event of the output voltage reference, Fig. 13a shows the transient response of the converter using a conventional SDADC with f_{OS}=6.25 MHz. Fig. 13b shows the transient response of the converter using the new SDADC for the same operating conditions and n=10. It can be seen that both the overshoot and settling time are significantly reduced when the sampling frequency is increased as a result of the mid-cycle updates.

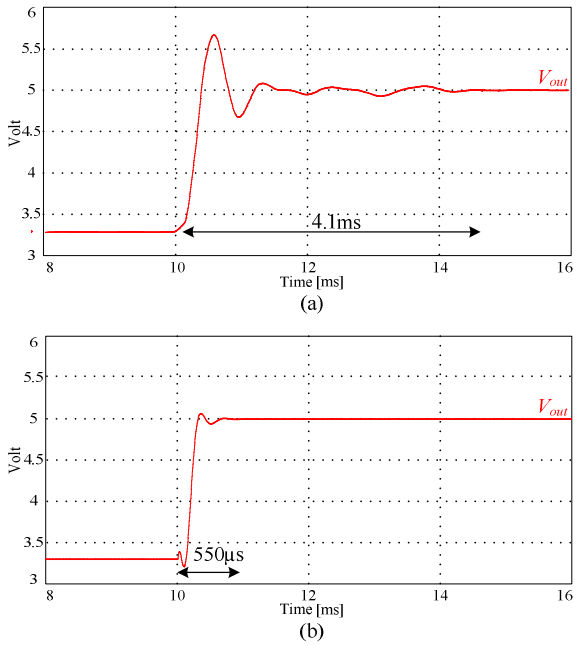


Fig. 13. Output voltage transient response of the simulated buck converter for 3.3V to 5V: (a) Conventional SDADC with full-cycle update (b) New SDADC with mid-cycle updates.

VI. Experimental System Implementation and Validation

To validate the operation of the new SDADC in a VM control loop, an FPGA based controller utilizing 10-bit counter based SDADC has been fully coded in Verilog and implemented on a Cyclone IV FPGA using Quartos environment, resulting in approximately 205 logic cells. The operation has been demonstrated with a buck converter prototype operating at 100 kHz for a nominal output voltage of 3.3V. Table I summarizes the experimental setup main characteristics. The first step of the experimental validation is to characterize and quantify the sampling accuracy of the SDADC. This is done for a wide range output voltages of the buck converter prototype. Fig. 14 shows the results for varying the output voltage in the range of 2.8v to 8V. It can be seen that in the range of the nominal output voltage that the error of the SDADC is less than 1%, while worst-case error of 4.6% is obtained for sampled voltage of 8V.

To further validate the effectiveness of the enhanced SDADC, the experimental prototype has been evaluated through a closed-loop VM operation. Fig. 15 shows the results for a step event of the output voltage reference, such that the output voltage varies from 3.3V to 5V, which are in good agreement with the simulation results in Fig. 13. Shown in Fig. 15a is the response of the system with the developed SDADC, it can be seen that system is well regulated validating the proper functionality of both the SDADC and digital control loop, where a 100mV overshot is obtained. Fig. 15b shows the response of the experimental prototype while using a conventional SDADC, it can be observed that the obtained overshot is 8.8V that is 38 times larger overshoot compared to the SDADC developed in this study. In addition, 3.6 times shorter settling time is achieved

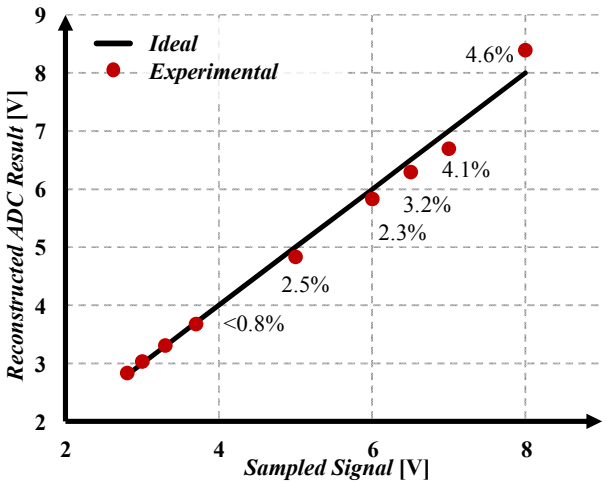


Fig. 14. SDADC accuracy experimental measurements for wide range sampled output voltages.

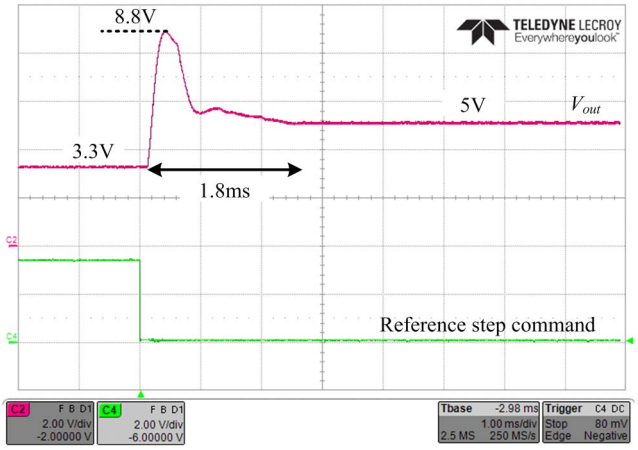
TABLE I – Experimental Prototype Characteristics

Parameter	*Value/Type*
Input voltage V_{in}	10V
Output voltage V_{out}	3.3V
Switching frequency f_s	100kHz
Inductor	75µH
Capacitor	100µF, ESR=0.5Ω
Counter number of bits *n*	10-bit
Number of mid-cycle updates	4
Modulator's clock frequencies	3.125/6.25 MHz

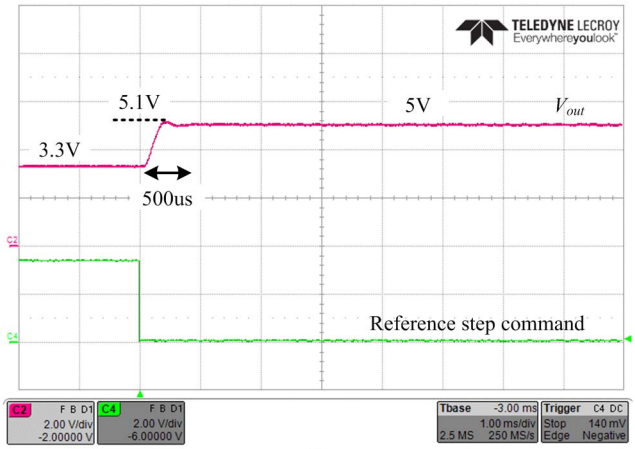
while using the new SDADC. Fig. 16 depicts a zoom-in on transient event of the output voltage within the system. It can be well observed that during the transition, the duty-ratio is varied according to the pre-defined mid-cycle update commands, which in this case are set in the range of 6-bits to 10-bits. The duty-ratio is increasingly growing to compensate for the variation at the output voltage, eliminate the need to wait for an update command every 2^{10} clock cycles.

VII. Conclusion

An enhanced performance fully-synthesizable SDADC has been presented, and verified through simulation and experimental data. The new SDADC has less hardware and silicon requirements compared to a conventional SDADC, while presenting much better dynamics, generating fast digitizing of the sampled signal with high accuracy and wide dynamic range, even for fast variations without the penalty of sacrificing the precision. In addition, a digital VM compensation has been realized and experimentally verified with a buck converter. The accuracy of the SDADC has been experimentally characterized by measuring the output voltage over wide range operating points, demonstrating worst-case error of 4.6%, while in the vicinity of the nominal operating conditions 99% accuracy has been achieved. The VM control including the new SDADC have been designed in digitally-oriented approach without any power hungry analog blocks, and implemented in 0.18µm 5V CMOS process resulting in total effective silicon area of 0.07mm^2.



(a)



(b)

Fig. 15. Output voltage transient response of the experimental buck prototype for 3.3V to 5V: (a) Conventional SDADC with full-cycle update (b) SDADC with mid-cycle updates. Output voltage (top – pink) 2V/div, voltage reference step (bottom – green) 2V/div. Time scale 3ms/div.

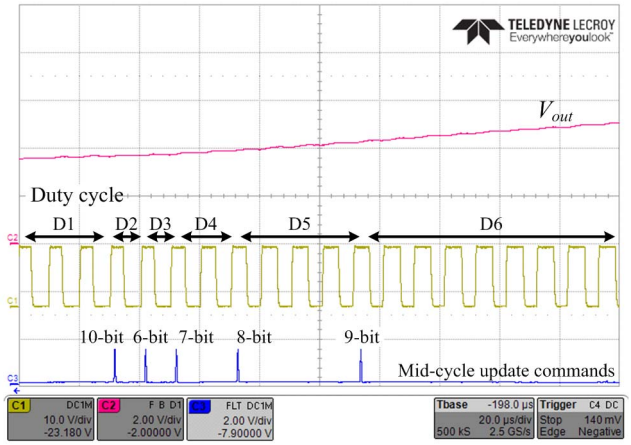


Fig. 16. A zoomed-in view on a transition event with increasingly growing duty-ratio based on mid-cycle time update results.

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