Enabling Criteria and Circuits for Low-Power High-Density Off-Grid Converters

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***Abstract* – - This paper presents a hardware efficient realization of a low power grid-tied power supply. The SMPS is enabled through flyback configuration accompanied by simple control circuitry for voltage-dependent constant on-time, which have been designed to maximize power density. It also includes start and power up circuits to enable operation from 85Vac to 120Vac. The design is entirely based on off-the-shelf components and customized magnetic element and results in a well-regulated 3V output voltage from 110Vac, with peak efficiency of 84%, and volume of 1 cm^3. The very high power density (3kW/Liter, 50W/cui) is enabled by an optimization process for characterizing the magnetic element, mode of operation and values of key components to facilitate a ratio of I_{avg}/I_{rms} close to unity throughout the range of the input voltage. Experimental results validate the optimization method, and verify the operation of the control and power up circuits.**

I. Introduction

Grid-tied power supplies are amongst the most common applications, with variety of converter topologies, control methods employed, and wide range of power levels. However, applications below 5 watts are somewhat overlooked in this family. In volume-sensitive grid-powered systems, such as smart dimmers, sensing nodes, IoT end-units, etc. that are rated in the range of 1 to 3 watts, off-the-shelf options are rather limited. In particular, control methods and available controllers that yield reasonable voltage regulation come often at the cost of relatively low efficiency and large dimensions. These are resolved by either implementation of a dedicated controller IC, which in many times financially prohibitive, especially for applications manufactured in low quantity. The other option is to adapt existing controllers that are less suitable for low power and compensate by oversizing the power components [1-10]. A common example of the latter can be found in various 5V 5W USB-compatible power supply. To exploit the full potential of the power stage a dedicated controller designed for specific power level is required. This study pursues the concept of hardware-efficient controller platform, specifically tailored for high conversion ratio at low power levels. The control logic adjusts the operation according to the power and input voltage level. This degree of freedom enables to choose system parameters so that performance is optimized at lower power level, such as the 1-3 watt mentioned earlier, and maintains high efficiency.

There are several challenges associated with discrete controller implementation. One of the major challenges for volume sensitive grid powered applications is to start-up the system [11-15], i.e. creating an efficient auxiliary supply that will power up the controller and bring the power stage to a nominal operating point avoiding the extra strain on the components associated with step turn on [1-3]. Additional challenges include an efficient implementation of the control and housekeeping functions present in an integrated standalone controller [4].

The objective of this study is to present a hardware efficient solution for low power high-density grid-tied conversion as detailed in Fig. 1. It includes a customized, high conversion ratio flyback converter, regulated by an adaptive on-time voltage mode controller that is realized by simple logic [16]. The system also includes the start and power up circuits, which facilitate soft-start through the auxiliary periphery. It is a further objective of this study to present a design procedure optimization and circuit implementation targeted to achieve high efficiency over a wide input voltage range posed by the grid [17-20].

The rest of the paper is organized as follows: Section 2 presents the power up circuits and soft start operation that have been developed. The realization of simple adjustable on-time generator is detailed in Section 3. Experimental validation is provided in Section 4. Section 5 concludes the paper.

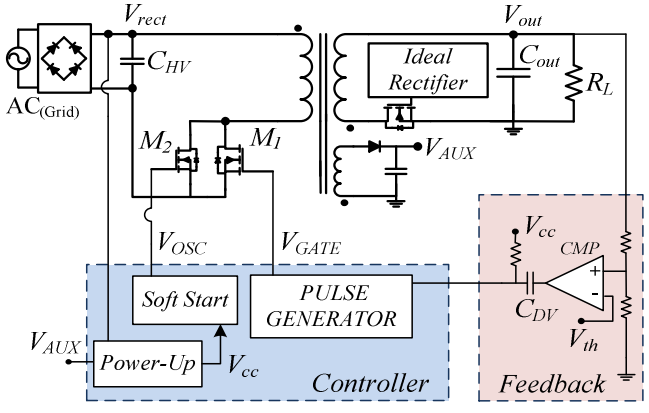

Fig. 1. Flyback converter and major control blocks

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II. POWER-UP AND SOFT START

DC-DC converters operated off a high voltage source such as the AC grid require a way to initiate the operation of their low voltage logic, i.e. a start-up power supply. One practice is by a current sourcing element that builds up the voltage gradually on an auxiliary capacitor. An alternative common practice to create a low voltage initial power source is to charge the auxiliary capacitor either using a bleeding resistor connected to the rectified high voltage point, or by a voltage divider. In both cases, a clamping mechanism is employed to ensure that the low voltage circuitry is not exposed to the high voltages. In this study, a simple voltage divider is used to start up the system. To disable the voltage divider, two zener diodes are used. The parallel zener diode D_{Z2} (Fig. 2) ensures overvoltage protection and creates the lower voltage threshold for start-up circuit operation. The series zener diode D_{Z1} comes to create a second, higher voltage level, where the operation of the start-up circuit begins. To avoid excessive power draw from this low efficiency start up supply during the continuous operation of the converter, a high efficiency auxiliary power supply is added to the converter through an additional secondary winding of the flyback converter. The auxiliary power supply is designed to reach slightly higher voltage than the voltage achieved using the bleeding resistor mechanism, so that during the running mode, the current draw from the resistive branch is blocked by the diode D_1, and the combination of two zener diodes D_{Z1} and D_{Z2}, as shown in Fig. 2. This combination results in a setup where high efficiency auxiliary power supply is providing the power to the control logic and gate drive circuits.

After initial power up of the control logic, there is the main challenge to be addressed - soft start of the power converter. During turn on, a large inrush current may develop, because both the inductors and the capacitors are at zero current/voltage. This current may exceed the rating of the components. Moreover, turn on transients may create voltage overshoot and exceed the maximum voltage rating of the components. To avoid high currents and dangerous overshoot conditions, during the soft-start, main control loop is suspended, and the converter is controlled by a secondary, many times open loop system that gradually increases the exposure of the system to the nominal stress. Once the converter approaches desired operation point, the main control loop takes over.

As can be seen from Fig. 3 the soft-start system is implemented using a dedicated, low power oscillator. The idea is to create a self-oscillating circuit that starts the switching of the converter at some lower frequency, and brings the system to a state where it generates sufficient output voltage to maintain the logic and driving circuitry. At that point, the low power oscillator is disabled and the main control loop takes over. The soft start system in this work is also a wake up system. Due to the strict implementation of the main control unit using the logic gates, it's functionality is limited to a certain range around the desired operation point. To further limit the inrush current two different switches are used, one for start-up and one for normal operation. The start-up switch has much higher resistance to limit the inrush current, while the main switch is optimized for efficiency operation of the circuit and has a lower conduction resistance.

Low power, start-up oscillator implementation using logic gates is shown in Fig. 3. It is based on a conventional NAND-gate a-stable multi-vibrator assembly with duty ratio adjustment. The circuit includes several features: first is the separate on-time setting using R_{on} and the diode that used to limit the maximum current in DCM operation. Second is the OFF time setting, implemented using R_{off} and antiparallel diode, which together with R_{on} sets up the switching frequency of the oscillator. In addition, it includes the shutdown circuitry and power good signal that turns the oscillator off once the power stage reaches the operating point, enables the main controller and signals the availability of the output power to the load.

The oscillator is based on two NAND logic gates, $NAND_1$ and $NAND_2$ that are closed in a loop with $NAND_2$ operating as inverter. Each of the gates introduces 180 degrees phase, to create a positive feedback oscillator. The timing, as previously mentioned, is set by the capacitor C_{osc} and two resistor-diode pairs R_{on}, D_{on} for on-time, and R_{off}, D_{off} for off time (Fig. 3a).

Oscillator principle of operation could be divided into two parts. First part begins with the output of the oscillator V_{osc} at logic '1', and the voltage node V_c (Fig. 3b) is at the voltage equal

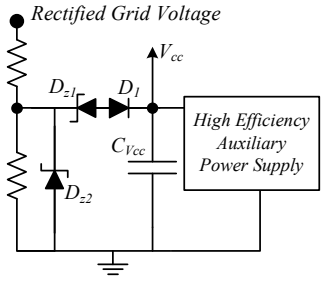

Fig. 2. Initial power up circuit and it's shutdown mechanism for higher efficiency.

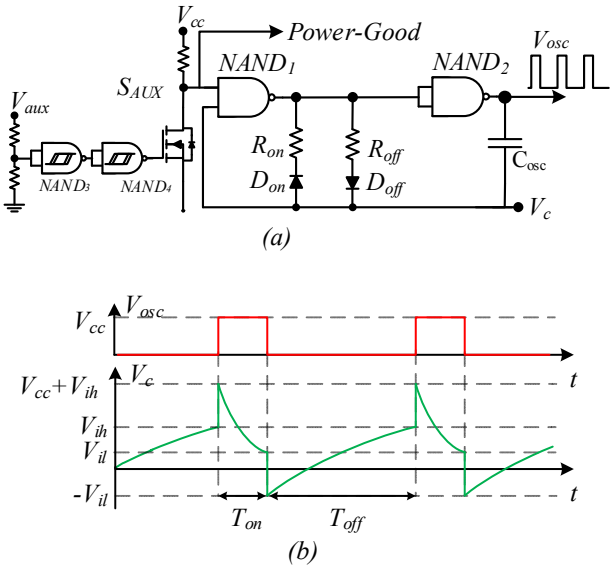

Fig. 3. Low power soft start oscillator: (a) Schematics; (b) Operation waveforms.

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to (V_{cc} + V_{ih}), V_{ih} is the threshold voltage for the NAND gate to transition to logic state '1'. If there is no auxiliary power available, $NAND_1$ inputs are both '1', and it outputs '0'. The capacitor C_{osc} discharges through the resistor R_{on}, to the value of V_{il}, setting the on-time. V_{il} is the threshold voltage for the NAND gate to transition to logic state '0'. Second part begins once the $NAND_1$ output changes to '0'. The voltage at node V_c will drop to (-V_{il}) and capacitor C_{osc} begins to charge, bringing the node V_c back to V_{ih}. Then the cycle repeats. On and off times are calculated using the RC charge/discharge equation (1), and are a function of the V_{cc}, V_{ih}, V_{il} voltages (diode voltage drop is assumed zero here) and the resistors R_{on}, R_{off}. The equations are summarized below:

$$T_{on} = \tau \ln\left(\frac{V_{il}}{V_{cc}+V_{ih}}\right);\ T_{off} = \tau \ln\left(\frac{1}{V_{cc}-V_{ih}-V_{il}}\right), \qquad (1)$$

where τ = RC is the time constant of the relevant RC circuit ($R_{on}C_{osc}$ during T_{on}, and $R_{off}C_{osc}$ during T_{off}).

Enabling/disabling of the start-up oscillator is implemented through logic. It is based on the built-in hysteresis of the gates. Once the auxiliary power supply is running and provides the voltage, it triggers the gate $NAND_3$ (Fig. 3a), which is then inverted by $NAND_4$ that turns on the switch S_{AUX} (Fig. 3a). S_{AUX} is then changes one of the $NAND_1$ inputs to be '0' (Fig. 3a), and stops the oscillations of low power oscillator. This is further utilized to generate a power-good signal based on the OV/UV conditions of the voltage rail that is generated. This switches between the main controller and low power oscillator using a NOR gate (Fig. 4).

III. Adjustable On-Time Pulse Generator

One of the challenges with grid connected systems is the wide input voltage range, and associated requirement for wide conversion ratio of the converter. The control method used in this work is a constant on-time controller, with hysteretic feedback for the off time. It is a simple control algorithm, that while paired with a converter operated in DCM, transfers constant portions of charge to the output, assuming constant voltage is at the input. Constant on-time control sets a hard limit on the conduction time of the main switch, this in turn provides in a secondary way, cycle-by-cycle input overcurrent protection functionality.

To create a more robust practical circuit, two additional features are implemented in the generator. One is adjustable time constant that governs the width of the on-time, and the other is excitation blanking, or minimum off-time to maintain DCM operation of the converter and to create better noise immunity to potential spurious double pulse excitations.

Converter design is implemented to ensure the ability to provide nominal output power at the minimum input voltage. However, for the same inductor, at the maximum input voltage case, the charge per cycle supplied to the output is larger proportionally to the voltage. As a result, relatively long off times are generated that scale down the switching frequency, which translate into large output voltage ripple, and high RMS currents for the same load. Large peak current also require physically larger inductors that won't saturate. One possible remedy to this condition is an adjustable on-time. This limits the peak current at a maximum predefined value for any input voltage. Nominal output power supply is achieved by increasing the switching frequency of the converter to maintain the same amount of charge per cycle (which is automatic with the hysteretic ripple-based feedback that is employed).

Full circuit implementation of the constant on-time pulse generator exhibiting input voltage feedforward for the on width, minimum off-time or blanking time, and a hysteretic feedback is shown in Fig. 5. Constant on-time is generated by a logic-based one-shot timer, built around two NAND gates and two delay networks. Where one delay network consists of C_B and R_B is responsible for timing a window where the timer is enabled and ready to receive excitation for the next pulse. This way, time constant C_BR_B limits the total minimum on+off period. Second adjustable delay network consists of the capacitor C_T and controlled capacitor discharge circuit built around an operational amplifier (Fig. 5) generates on-time pulses with the width proportional to the amplitude of the input voltage. Simple implementation of the pulse generator, provides the functionality, and the limitation of ratio change of the on relatively to off-time could be taken into account at the design stage.

Input NAND gate - $NAND_5$ receives an excitation signal from the feedback comparator and initiates the two delay networks. At this point capacitors C_B and C_T begin to charge with different time constant, and an on-time pulse begins at the output of the second NAND gate - $NAND_6$. At the same point, inverting gate INV_1 that provides the feedback path locks the input of the $NAND_5$ gate for further excitations by switching V_{FDB} to logic low. Capacitor C_T has shorter time constant and finishes the on pulse before the capacitor C_B switches the inverting gate back to logic high to allow further excitations from the feedback, and finishes the OFF time blanking time.

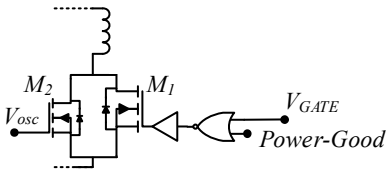

Fig. 4. Selection mechanism between the low power oscillator and the main controller.

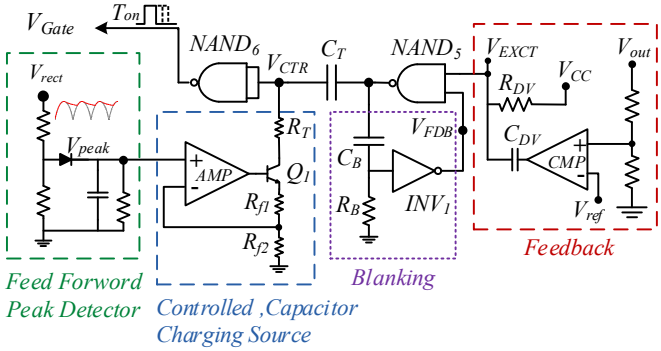

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Fig. 5. Adjustable on-time and minimum off time square wave generator based on a one-shot circuit.

From this point the process repeats periodically upon feedback comparator excitation. Ripple-based hysteretic feedback is implemented using a comparator and a derivative circuit of a resistor R_D and capacitor C_D (Fig. 5). Derivative network at the output of the feedback comparator comes to limit the width of the excitation pulse, and to keep it at minimum to enable short on-times.

To remedy the efficiency disadvantage of a simple constant on-time control in a presence of wide input voltage variation a feedforward mechanism is introduced. A controlled charging source is inserted into the on-time part of the one-shot generator. In a simple one-shot implementation, the on-time of the square wave generator is dependent on the time required to charge the capacitor to V_{il}, which in turn is a function of the timing resistor and capacitor R_T and C_T values. To adjust the amount of charge transferred to the output of the flyback at different input voltage levels, an adjustable on time one-shot implementation is presented in this work. The adjustment is done using a controlled capacitor-charging source (Fig. 5). The source is implemented using a BJT transistor Q_1 and an operational amplifier, closed in a feedback to regulate the capacitor discharge current to the reference level. The reference level is provided by the feedforward signal from the input voltage, V_{peak}, passed through a low bandwidth, peak detector circuit. In this manner, a higher input voltage of the grid, results in a higher capacitor charging current, and consequently shorter on-time of the square wave generator. This will ensure equal charge amount transferred by the flyback to the load, despite the wide variation of the input voltage presented by the grid.

IV. Design Considerations

Due to low power, high conversion ratio, and high power density of the converter, a custom designed magnetic element is major enabler. One of the crucial parameters of the flyback inductor is the absolute value of the uncoupled, leakage inductance. It depends on the proximity of the primary winding to the secondary, and as a secondary effect the value also proportional to the permeability of the core. The challenge is to create high ratio windings to allow a good step-down flexibility, while lowering the leakage inductance. Extra challenge is the overall low number of turns, so the secondary winding may have one to three turns, which need to be well coupled. For example, two turns of the secondary windings need to be in a good proximity to all the fifty turns of the primary at once. The way we solve that in this work, is by substituting thick secondary wire with a distributed litz wire, consistent of many small strands as shown in Fig. 6. The primary coil is created by winding a single strand thin wire in one or two passes over the bobbin. Next, the secondary litz wire is spread evenly along the bobbin and allowed to penetrate into the voids created by the primary winding. Coupled inductor side cut is schematically presented in Fig. 6, where the thicker blue circles represent the primary winding wire, and each circle or turn is in series to it's neighbors turn, and the thinner red circles represent the secondary litz wire, where each circle is in parallel to it's neighbors. It is important to highlight that the purpose of the litz wire here is not to overcome the skin effect (which could be it's secondary function

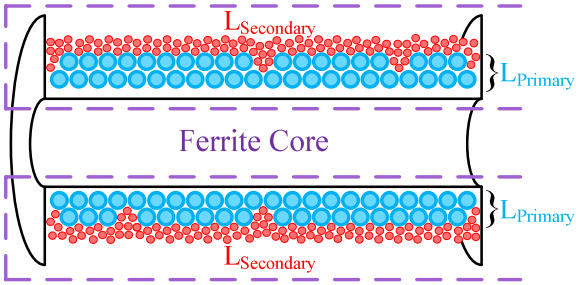
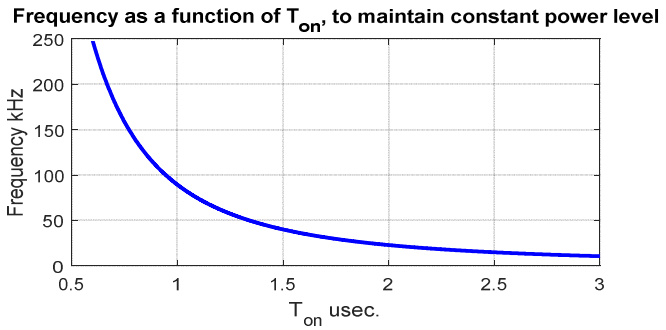


Fig. 6. Minimum leakage winding method.

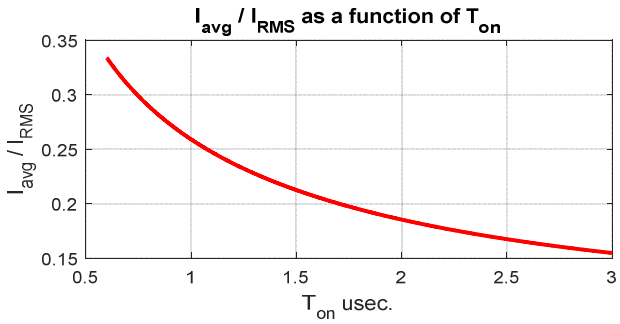
here), instead it is used to create the conditions where the primary and the secondary windings are in the most possible proximity to each other, over the maximum available area.

The method described above allowed implementing inductors of 2.6mH with leakage as small as 17µH. It should be noted however, that this method is appealing to applications where isolation requirements are moderate. For example non-isolated flyback or tapped buck converters, that require high conversion ratio. It should be considered more carefully for applications where high voltage isolation between the primary and the secondary is needed.

Important design consideration is the efficiency of the converter. The losses in a converter many times are related to the RMS current, i.e. the current that circulates in the converter, while the average current is the effective, DC current eventually transferred to the load. The metrics of the losses used in this work are the ratio between the average and RMS currents.



(a)



(b)

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Fig. 7. Constant on-time control characteristics: (a) Expected frequency range for 3W system discussed in the experimental section. (b) Expected average to RMS ratio over the range of the on-times that cover the input voltage range.

Average to RMS currents ratio is summarized as:

$$\frac{I_{avg}}{I_{RMS}} = \frac{\sqrt{3}}{2}\sqrt{T_{on} \cdot f_{sw}}\,, \qquad (2)$$

where I_{avg} is the average input current, and I_{RMS} is the RMS input current. f_{sw} is the switching frequency of the converter. Since the switching frequency of a grid tied converter with rectifier and smoothing capacitor, controlled with constant on-time and variable frequency is not constant an average switching frequency f_{avg} is calculated. The behavior of f_{avg} as a function of T_{ON} and constant power in the system described above is shown in Fig. 7.

Frequency range, where the system is able to supply nominal output power over the expected input voltage variation, V_{rect}, is calculated and presented as a function of on-time in Fig. 7a. Expected average to RMS current ratio is calculated using (2), where switching frequency was substituted with average switching frequency over the grid cycle, f_{avg}, and is shown in Fig. 7b. It can be concluded from Fig. 7b that despite the square root behavior of (2), higher switching frequency that is required due to shorter on-times, results in a better I_{avg}/I_{RMS} ratio, and consequently higher potential efficiency of the system.

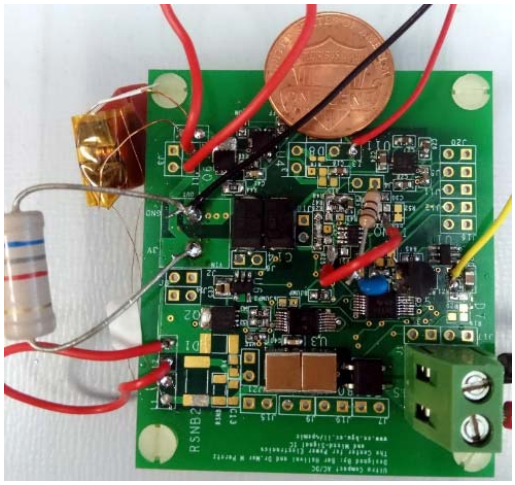

Fig. 8. Experimental prototype.

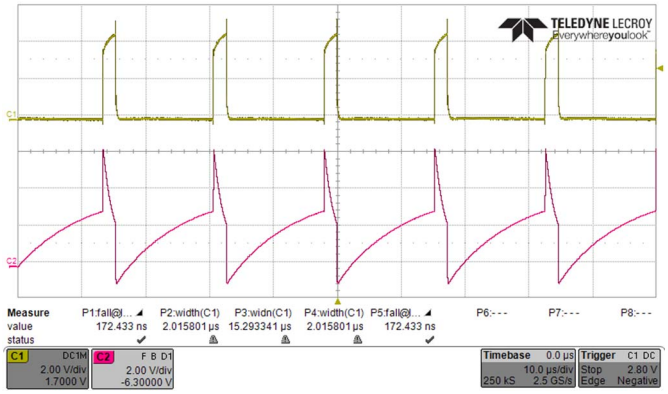

Fig. 9. Low power oscillator operation. Upper trace – Oscillator Output (2V/div); Middle trace – Oscillator timing capacitor voltage V(C_{osc}) (5V/div). Time scale 10µs/div.

V. Experimental Results

To validate the start-up and control circuitry presented in this work an experimental prototype has been constructed (Fig. 8). System parameters are summarized in table 1. Operation of the low power oscillator with different on and off times is shown in Fig. 7. The experimental results are validating the theoretical waveforms presented in Fig. 3b. The operation of an adjustable on-time square wave generator is presented in Fig. 10, Fig. 11 and Fig. 12. Fig. 10 presents the operation of the flyback converter and the one-shot based square wave generator during the low input voltage grid conditions. Adjustable timing capacitor circuitry creates longer on-times, 1.5 µs in this case, and allows developing higher currents despite relatively low input voltages, thus maintaining the output voltage regulated during the worst input voltage conditions. Fig. 11 and Fig. 12 demonstrate the operation of the flyback converter and the generator during the high input voltage conditions of the grid. In this case the on time is shorter than in the previous case and stands on approximately 1 µs. Shorter on time for the higher voltages results in the same peak current, and higher switching frequency, which prevents large unnecessary rms currents. Efficiency results as a function of the input voltage and load conditions are demonstrated in Fig. 13. Overall efficiency achieved with the prototype is 70-75% for most of the loading range, while some peak values of 84% were recorded at lighter load conditions. In the current design the power density above 3kW/liter was achieved. Volume distribution of the system modules is summarized in Fig. 14.

TABLE I – Experimental Prototype Values

Component	***Value/Type***
Input voltage V_{in}	85-110 VRMS
Nominal output voltage V_{out}	3V
Nominal output current I_{out}	1A
Switching frequency f_{sw}	30 - 250kHz
Inductor L	1.375mH, 50mΩ DCR
Capacitor C_{out}	330µF, 5mΩ ESR
Primary MOSFET	STL3NM60N
Coupled inductor turns ratio	25:1

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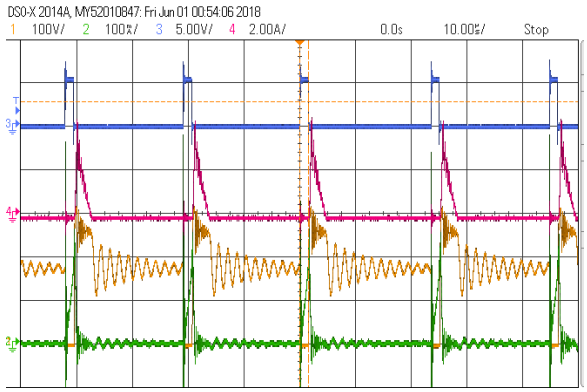

Fig. 10. Flyback converter operation: Low voltage grid conditions – Long T_{on} of the one-shot (1.5 µsec); Upper trace – Gate signal (5V/div). Second top trace - secondary inductor current (2A/div), Second bottom trace – MOSFET Drain voltage (100V/div); Bottom trace – Primary side current (100mA/div). Time scale is 10µs/div.

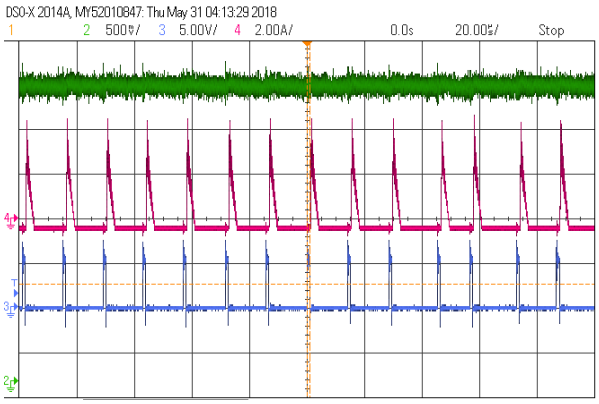

Fig. 11. Flyback converter operation: High voltage grid conditions – short T_{on} of the one-shot (1 µsec); Upper trace – output voltage (0.5V/div); Middle trace – secondary inductor current (2A/div), Bottom trace – Gate signal (5V/div). Time scale is 20µs/div.

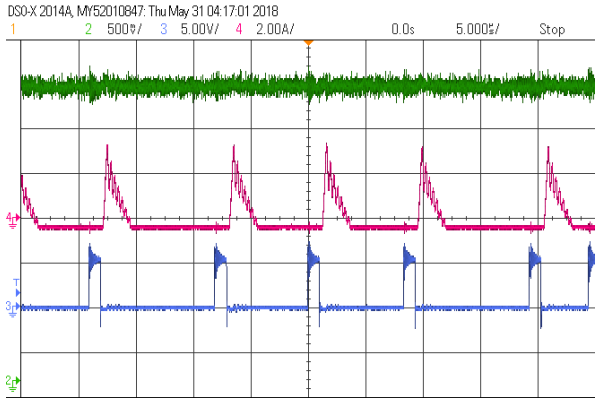

Fig. 12. Flyback converter operation: High voltage grid conditions – short T_{on} of the one-shot (1 µsec); Upper trace – output voltage (0.5V/div); Middle trace – secondary inductor current (2A/div), Bottom trace – Gate signal (5V/div). Time scale is 5µs/div.

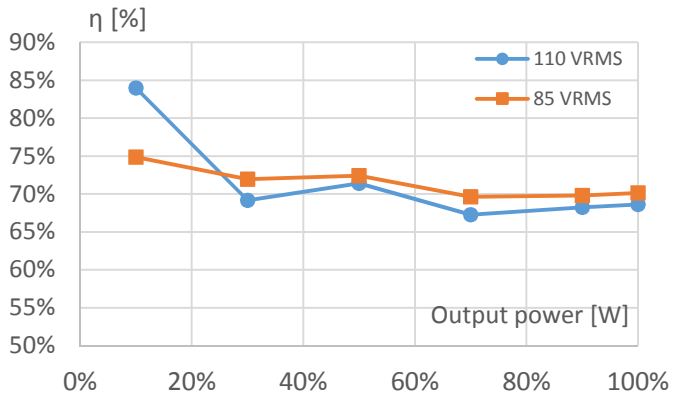

Fig. 13. Efficiency curves as a function of the load at different input voltage levels. Nominal load is 3W.

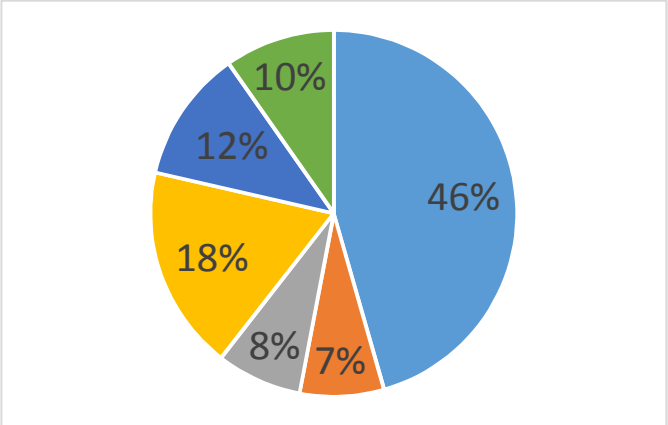

Fig. 14. Volume distribution of the converter components: (clockwise) 46% Magnetics, 7% Controller, 8% Output capacitor, 18% Input capacitor, 12% Bridge rectifier, 10% power stage switching components.

VI. Discussion

The options available to design a high density, low power off the grid converter are still limited due to economic reasons. Adapting an off the shelf, all in one controller, optimized for higher power is the option of choice for many designers today. The major advantage is short development time. In addition, these controllers provide some extra benefits such as noise immunity, integrated protection mechanisms, and reduced component count. The option explored in this study, i.e. implementation of the controller using discrete components, is a much more time-consuming procedure in terms of design, circuit tune up, system stability and protection implementation. Some of the unique advantages of the approach that are unavailable using the integrated solution, are that certain operation range could be selected much more precisely, for example peak current at the primary, to maintain low input spikes, or switching frequency limits to avoid audible whine. In terms of system efficiency, comparable results could be achieved both using some best-fit integrated controller and using discrete components implementation approach as was demonstrated in this study.

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VII. CONCLUSION

A full control system to regulate a low power, high density off the grid-operated converter is presented. Start-up and soft start procedures are described and simple and effective control scheme to overcome wide input voltage variation is shown. The system includes start-up, soft start and adjustable control logic to provide high efficiency conversion over the input voltage of the grid. Design suggestions have been validated by experimental results. It is concluded that discrete implementation approach would be useful if the application has certain limits on the operation range and or emissions of the converter, while expected development time becomes longer than the mainstream approach, using off the shelf high power integrated controller. Comparable results in terms of efficiency are achieved in both cases.

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