Regulated Power Transfer Using Self-Tuned Networks for Capacitive Wireless Systems

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***Abstract* — In this paper, an adaptive multi-loop controller for capacitive wireless power transfer (WPT) systems is introduced. The new controller approach combines continuous frequency tracking and matching networks tuning on both the primary and secondary to regulate a target current to the receiving side at best power transfer conditions. This enables to effectively disengage the power delivery capabilities from the cross-coupling interactions between the transmitting and receiving sides, variations of the electrical circuits and capacitive medium. This paper highlights the complex functional relationships of the multi mixed-signal controller, and provides better insights on the dynamics and on the practical implementation of a closed-loop capacitive power transfer (CPT) system. An experimental self-tuned capacitive WPT prototype has been designed and implemented to verify closed-loop operation at the MHz range.**

Keywords* — *capacitive power transfer, capacitive coupling, multi-loop controller, closed-loop capacitive wireless system, impedance matching, self-tuned system, wireless power transfer.

I. Introduction

Capacitive power transfer (CPT) approach has been investigated in recent years, as an alternative near-field power transfer method to well know magnetic field based approaches. One of the more attractive advantages of capacitive-based WPT is the avoidance of undesired Eddy currents and electromagnetic interfaces (EMI) that comes with magnetic based WPT methods [1], [2] . In addition to efficiency improvements, CPT systems are potentially with lower volume and construction complexity [2]-[7].

A main challenge of general near-field WPT systems including CPT is that the power transfer capability and efficiency depends on the distance and alignment between the transmitting and receiving sides [6]-[8]. In addition, the coupling coefficient of the transfer medium and load conditions are sensitive to changes in the environment conditions, component aging and temperature drifts, which dramatically decreases the power transfer capabilities of the system. Reducing the sensitivity of the WPT system to variations can be alleviated by designing matching networks that provide loose coupling between the transmitting and receiving sides [3]-[5], [7]. In this solution however, the system characteristics still strongly depend of the component values and the precision of the operating frequency. To fully disengage the system's characteristics from any drifts, changes and variations, a closed-loop active compensation is essential.

Several methods to reduce the effects of components and medium variations of WPT systems have been proposed for general power transfer, which can also be adapted to CPT [8]-[14] such as: frequency tuning, compensation networks impedance matching, and post regulation DC-DC conversion. It should be noted that although existing closed-loop methods enable to overcome some system variations and to extend the power delivery range, a single control method is not sufficient to guarantee reliable operation of WPT systems. On the topic of magnetic field based WPT and in particular magnetic resonance, combined control methods has been investigated [9], [15], however, a closed-form control mechanism for CPT has not been addressed hitherto.

The objective of this study is therefore to introduce an adaptive multi-loop controller for CPT technology, which compensates on the fly for variations of source and the load circuits, coupling interface (distance and/or alignment) and matching networks as detailed in Fig. 1. The new controller

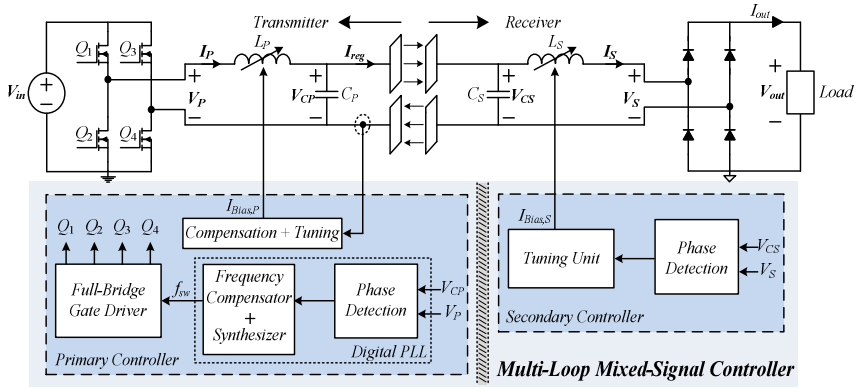


Fig. 1. Simplified schematic diagram of a double-sided *LC* capacitive WPT system with an adaptive multi-loop controller.

approach effectively disengages the power delivery capabilities from drifts or variations, which enables spatial freedom of the transferred energy to the receiving side. It relies on continuous tuning of the operating frequency to the resonant one, and adjusts both the transmitter's and receiver's matching networks such that the best power transfer conditions are obtained for any given combination of distance, displacement misalignment or component values. It is a further objective of this study to present a tuned network realization that is based on a variable inductor, i.e. it is not based on relays or semiconductor switches, and therefore enables continuous self-tuned impedance matching.

The rest of the paper is organized as follows: Section II describes the principle of operation of the multi-loop controller and details its algorithm. The control architecture and functional analytical relationships are delineated in Section III. Section IV provides details regarding the practical implementation. Experimental verification of a CPT prototype with the adaptive multi-loop controller is provided in Section V. Section VI concludes the paper.

II. Closed-Loop Tuning of a Double-Sided LC Capacitive WPT System

A high-level view of the tuning procedure utilizes the control loops is illustrated by the flowchart in Fig. 2. When the tuning procedure initiated, a default set of pre-loaded values are used to determine the switching frequency f_{sw}, and the variable inductors L_P and L_S. These values are determined by the target operating conditions of the system. The adaptive tuning operation is conducted per feedback loop. First, the switching frequency to drive the full-bridge is being tuned by the DPLL, where its inputs are the voltages V_P and V_{CP} such that a phase difference between the signals is detected. To guarantee that the switching frequency f_{sw} follows the resonant frequency f_0 for any given variations of the primary circuit, 90º phase angle between V_P and V_{CP} is maintained at all times. In the case that the detected phase difference between the signals is not 90º, an error signal is generated to the DPLL frequency compensator and generates new switching frequency until $f_{sw}=f_0$. The next stage of the tuning process is adjusting of the secondary side's inductance value, L_S. This results in a tuned secondary matching network, according to the operating frequency of the primary side. Similar to the previous stage, a phase difference between V_S and V_{CS} is detected and is maintained at 90º. The correction signal in this case adjusts the inductance value rather than the drive frequency (which has been determined by the primary circuit). This is carried out by a driver that feeds the bias winding of the inductor [20] until the network is at resonance and the phase difference between the signals V_S and V_{CS} equals 90º (further details regarding the variable inductor operation are given in Section IV). In the final stage the regulated current I_{reg} (Fig. 1) from the primary circuit is sensed and compared to a target/reference one. The tuning block generates a correction signal that effectively adjusts the inductance L_P through bias winding until the desired current is achieved. It should be noted that the inductance tuning (to adjust the transfer current) results in different resonant characteristics of the system, and consequently, the frequency tuning loop operates to lock the switching frequency to the new resonant frequency. To satisfy proper operation with reasonable dynamics of this multi-loop scheme, the compensators are decoupled by their bandwidth. The frequency tracking loop, is designed to be with highest bandwidth within the controller, i.e., responds the fastest among the multiple control loops. The frequency loop is followed by the secondary's loop, which is also designed to be a relatively high-bandwidth loop compared to current control loop. This practice, employed in many multiple-loop compensation schemes, assures that the faster loop is virtually transparent to its following and by doing so, significantly simplifies the system dynamics and complexity of the compensators.

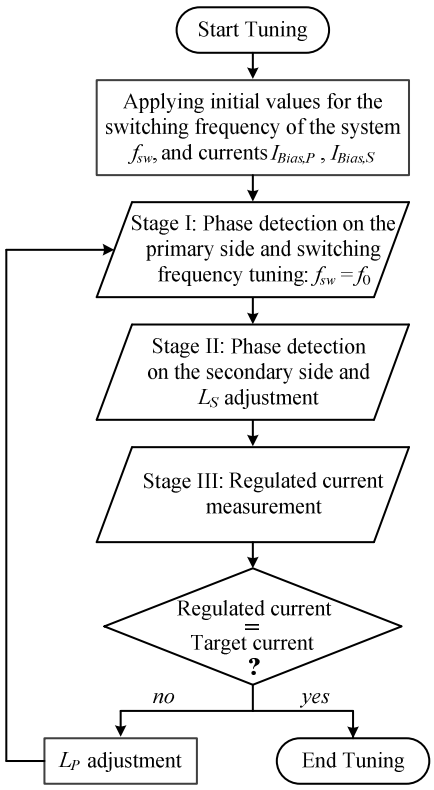


Fig. 2. Flow chart of the controller's tuning procedure.

III. Controller Architecture

Considering the description of the control algorithm given in the previous section, a simplified functional block diagrams that describe the dynamic behavior of this self-tuned system is depicted in Fig. 3. The diagram comprise both linear and non-linear transfer functions to reflect the specific operation of each 'transformation unit' (i.e. 'block') [20]. It should be emphasized that throughout the functional derivations, small signal transfer functions are denoted by small letters. The diagram of the control scheme of the primary circuit includes two major loops to satisfy current sourcing behavior to the transfer plates (Fig. 3a). A third, independent loop is located at the secondary side to adjust the receiving network to the signal's frequency (Fig. 3b). In addition, for both the primary and secondary circuits, the bias driver of the variable inductors is designed as a closed feedback loop configuration to maintain a forced current control. This enables to reduce the order of the outer feedback loop, and therefore it is simpler to stabilize the overall system. By employing self-calibrating

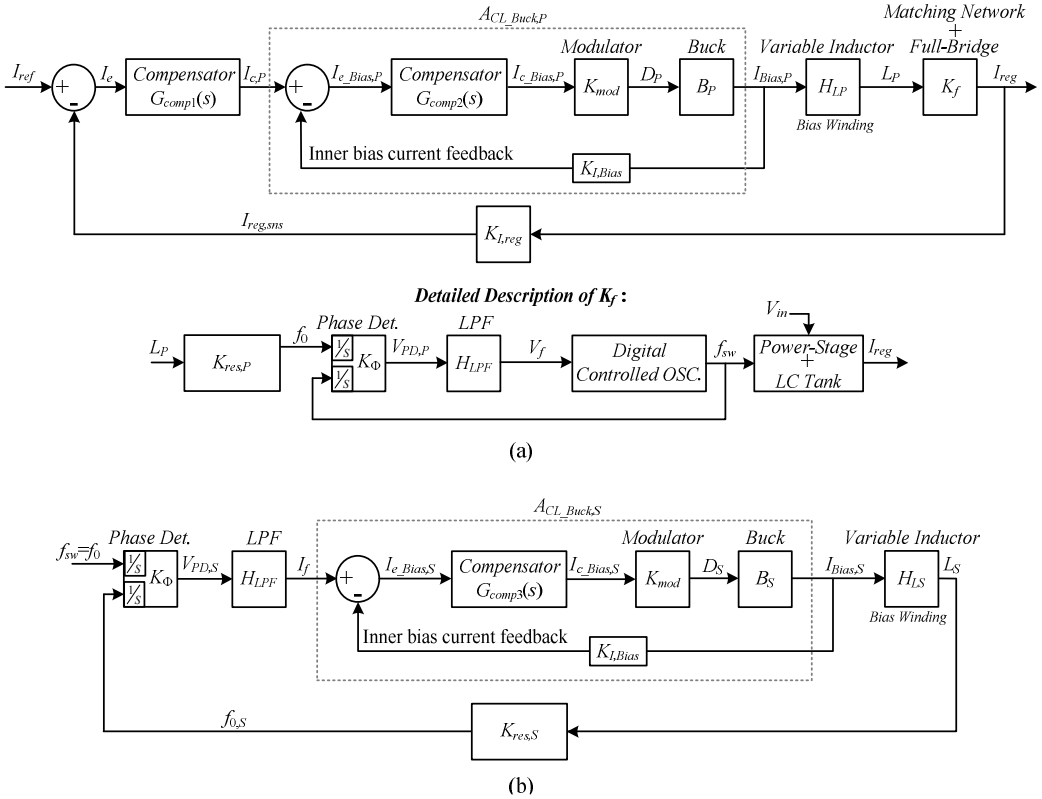


Fig. 3. Simplified functional block diagram of the multi-feedback controller: (a) Primary side control loops, (b) Secondary side control loops.

frequency loop and adjusting the system parameters, regulation of the primary's output current, I_{reg}, can be achieved at the same time that the system is kept at resonance (while soft-switching conditions are met).

Starting from the left side of Fig. 3a, I_{ref} is a proportional representation of the target regulated current from the primary to the secondary, where $I_{c,P}$ represents the correction signal generated by the current compensator, and $I_{e\_Bias,P}$ is the error signal of the inner bias current loop. K_{mod} stands for the transfer ratio of the modulator, i.e., bias current correction signal, $I_{c\_Bias,P}$ to duty-cycle of the bias current driver. The bias driver in this study has been realized by a buck converter, and its transfer function is represented in the block diagrams by B_P. The bias current for the inductor L_P can be expressed as

$$I_{Bias,P} = D_P B_P(s) = \frac{D_P V_{Buck}}{sL_{Bias} + R_{DCR}}, \quad (1)$$

where L_{Bias} is the inductor of the buck converter, R_{DCR} is the dc resistance of the inductor, D_P and V_{Buck} are the duty-cycle and the input voltage of the buck converter, respectively. After linearization, the small signal transfer function between the duty-cycle and the inductor current $b_P(s)$ is expressed as

$$b_P(s) = \frac{i_{Bias,P}(s)}{d_P} = \frac{V_{Buck}}{sL_{Bias} + R_{DCR}}, \quad (2)$$

where $i_{Bias,P}$ is the small signal bias current and d_P is the duty-cycle perturbation. Thus, the closed-loop transfer function of the buck converter is

$$A_{CL\_Buck,P}(s) = \frac{i_{Bias,P}(s)}{i_{c,P}(s)} = \frac{G_{comp2}(s)K_{mod}b_P(s)}{1 + K_{I,Bias}G_{comp2}(s)K_{mod}b_P(s)}, \quad (3)$$

where $G_{comp2}(s)$ is the transfer function of the inner compensator and $K_{I,Bias}$ is the gain due to the bias current sensing [20], [21]. By neglecting R_{DCR} and by assuming that the compensator has been designed properly to meet both phase margin and loop gain bandwidth, (3) can be further rearranged and simplified to a first order system [20]

$$A_{CL\_Buck,P}(s) = \frac{1/K_{I,Bias}}{1 + s/\omega_{Buck,P}} \quad ; \quad \omega_{Buck,P} = \frac{K_{I,Bias}K_{p2}K_{mod}}{L_{Bias}}. \quad (4)$$

where K_{p2} is the gain due to the compensator. The expression in (4) implies that for the frequency range $\omega < \omega_{Buck,P}$ the inner current feedback has transformed the bias buck converter (from error signal to bias current) from a first order system to a zero order system.

H_{LP} represents the bias winding such that the relationship between the bias current and the primary side inductance is

$$L_P = H_{LP}(I_{Bias,P}). \quad (5)$$

The relationship of $H_{LP}(I_{Bias,P})$ can be obtained by experimental measurements, advanced simulation tools such as Maxwell, or by analytical analysis which discussed in detail in Section IV-A. Thus, a local linearization around the operating point determines the non-linear small signal of H_{LP} as follows

$$h_{LP} = \frac{dL_P(I_{Bias,P})}{dI_{Bias,P}} = \frac{H_{LP}(I_{Bias,P0}) - H_{LP}(I_{Bias,P0} + \Delta I_{Bias,P})}{\Delta I_{Bias,P}}, \quad (6)$$

where $I_{Bias,P0}$ is the nearest measure value of the bias current for a given operating point, and $\Delta I_{bias,P}$ is the increment

between the two nearest measured values of the bias current around the operating point. Finally, K_f is the response of the matching network combined with power-stage to the variable inductor generated by H_{LP} (the ratio of the regulated current I_{reg} to a change of the resonant characteristics).

The bottom block diagram in Fig. 3a details the transfer characteristics of K_f. The output of H_{LP} dictates the resonant frequency f_0 of the CPT system such that

$$K_{res,P}(L_P) = f_0 = \frac{1}{2\pi\sqrt{\underbrace{H_{LP}(I_{Bias,P})}_{L_P} C_P}}. \quad (7)$$

Considering $H_{LP}(I_{Bias})$ is constant, a derivation of the large signal $K_{res,P}(L_P)$ around the operating point yields the small signal transfer function of the resonant tank [20]:

$$k_{res,P} = \left.\frac{df_0}{dL_P}\right|_{L_P(I_{Bias,P0})} = -\frac{1}{2L_{P0}} f_0 . \quad (8)$$

where L_{P0} is the primary's resonant inductor value around the operating point. Assuming that the frequency tuning is the fastest control loop within the system, f_0 is continuously compared to the switching frequency f_{sw} of the full-bridge to guarantee that $f_{sw}=f_0$. K_Φ represents the gain of the phase detector, consequently, the phase detector can be described as a module that includes two integrators at the input that translates frequencies into phases and a gain block. The outcome of the phase detection operation, $V_{PD,P}$, can be expressed as

$$V_{PD,P} = K_\Phi \varphi_{diff,P} = \frac{V_{DD}}{\pi}\varphi_{diff,P}, \quad (9)$$

where V_{DD} is the supply voltage of the phase detector, and $\varphi_{diff,P}$ is the phase difference between the target resonant frequency and the drive switching frequency signals. $V_{PD,P}$ which represents a proportional phase mismatch between the inputs of the phase detector for every switching cycle of the system is filtered by a lag-lead low-pass filter (LPF) network that is represented in the continuous domain as

$$H_{LPF}(s) = \frac{1+sCR_2}{1+sC(R_1+R_2)}, \quad (10)$$

thus, the zero frequency is always higher than the pole frequency. By doing so, the stability of the digital controlled oscillator (DCO) is improved since its phase margin can be increased compared to a simple LPF [22]. The voltage V_f is then translated by the DCO unit to a drive frequency for the power-stage combined with the LC tank, which in turn generates the desired target current.

Fig. 3b depicts the functional block diagram of the secondary's control loops, there, the operating resonant frequency of the system is compared throughout a phase detector to the resonant frequency of the secondary. It should be noted that for stable operating CPT system $f_{0,S}=f_{sw}=f_0$. Similar to the above given relationships of the primary side, the output signal of the secondary's phase detector $V_{PD,S}$ is given as

$$V_{PD,S} = K_\Phi \varphi_{diff,S} = \frac{V_{DD}}{\pi}\varphi_{diff,S}, \quad (11)$$

where $\varphi_{diff,S}$ is the phase difference between the primary's and secondary's resonant frequencies. $V_{PD,S}$ is filtered and translated to a current representation I_f, which with the aid of the inner bias current feedback $I_{Bias,S}$ for the variable inductor L_S, generates the modulation signal D_S for the buck converter, such that the closed-loop transfer function of the secondary's bias buck driver is

$$A_{CL\_Buck,S}(s) = \frac{i_{Bias,S}(s)}{i_f(s)} = \frac{1/K_{I,Bias}}{1+s/\omega_{Buck,S}}, \quad (12)$$

$$\omega_{Buck,S} = \frac{K_{I,Bias}K_{p3}K_{mod}}{L_{Bias}}$$

where K_{p3} is the gain due to the secondary's inner bias current loop compensator. As mentioned above, by sensing the buck current and feeding the signal back to inner compensation, for $\omega<\omega_{Buck,S}$ the dynamic effect of the bias loop is eliminated. The resultant inductance value of L_S dictates new resonant frequency $f_{0,S}$ until phase difference $\varphi_{diff,S}$ equals 90º, implying that the transmitting and receiving sides are matched, and the system is operating under optimal power transfer conditions. It should be noted that the transfer functions of h_{LS} and $k_{res,S}$ are obtained in a similar manner to h_{LP} and $k_{res,P}$ as given in (6) and (8), respectively

IV. Practical Implementation

A. Variable Inductor

One possible implementation of variable inductor is shown in Fig. 4a, where a magnetic structure is described with the ability to change the inductance of the inductor independent of other power transfer circuit parameters [20], [23]. The structure comprises an *E*-core type magnetic element whereas the primary inductor is constructed on the middle, gapped leg. The bias/control winding is formed on the outer, non-gaped, and their windings are connected in series but with opposite polarity. By doing so, the ac coupling between the center leg to the bias winding is cancelled. Passing dc current through the auxiliary winding would partially saturate this portion of the core, resulting in variable inductance, as illustrated by Fig. 4b.

The inductance value L can be found with the aid several design parameters such as: number of turns n, air-gap l_g, and the effective magnetic path length l_e, and thus, the expression of L can be expressed as [24]

$$L = \frac{n^2\mu_0 A_e}{l_e}\frac{\mu_r(I_{Bias})}{1+2\frac{l_g}{l_e}\mu_r(I_{Bias})}, \quad (13)$$

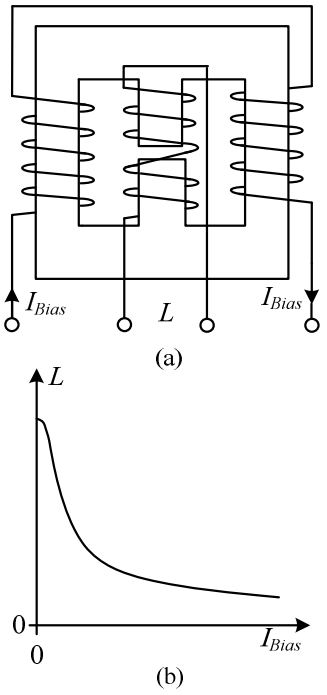


Fig. 4. (a) Variable inductor practical implementation, (b) Relationship between the inductance value and the bias current.

where μ_0 is the air permeability, μ_r is the magnetic core permeability, and A_e is the core area. μ_r depends on the bias current I_{Bias} and can be obtained from either the manufacturer data or by experiment [24], [25]. A simplistic expression of μ_r is given by

$$\mu_r(I_{Bias}) = \frac{\mu_{mi}}{1+\left(H(I_{Bias})/H_{\text{pole}}\right)^j}, \tag{14}$$

where μ_{mi} is the permeability initial value, i.e., $\mu_{mi} = \mu_r(H{=}0)$, H_{pole} is the magnitude of the saturation field and j sets the permeability slope. The variable H is proportional to the bias current, and is expressed as follows

$$H\left(I_{Bias}\right) = {nI_{Bias}}/{l_e}. \tag{15}$$

B. Limit-Cycle Oscillations in Digitally Controlled Resonant Converters

A major practical issue that should be considered when designing closed-loop resonant based WPT systems are limit-cycle oscillations, which resulted from the presence of the quantizing units of the controller, i.e., analog-to-digital converter (ADC) and the DCO (assuming the compensators does not add quantization error) [26]. Primary cause for limit-cycle oscillations in resonant converters is that the input-output gain is not constant and varies as a function of the frequency. In capacitive WPT systems, which operate at resonance the effective impedance is very high due to the coupling plates, and a very high parallel quality factor Q is considered, which translates to a very high voltage gain. In addition, as discussed in the previous sections, one of the key parameters to successfully regulate the power, is that the system locks on the resonant frequency. However, to guarantee optimal power transfer conditions, soft-switched operation should be satisfied, that is to generate a drive frequency which is slightly above the resonant frequency. This objective requires very sensitive calibration which may also result in limit-cycle oscillations, since in resonant converters the frequency resolution highly depends on operating conditions and the location of the drive frequency with respect to the network's resonance [5], [7]. Another issue is that since the quality factor Q is not constant and depends on the capacitive medium characteristics (distance, alignment, etc.), it affects the input-output gain of the system. Therefore, to assure proper operation worst case of the resolution sensitivity should be considered, i.e., the highest Q that the system might have. Thus, the ADC and DCO units in this study have been designed such that limit-cycle oscillations are remedied. A key criterion for determining the existence of limit-cycle oscillations in resonant systems relies on the comparison between the LSB value (i.e., resolution) of the ADC and the output signal variation due to a LSB change of the control [26]-[28], i.e., a necessary condition for no limit cycles is that the variation of the output ΔS_{out}, due to a LSB change of control is smaller than the ADC resolution Δ_{ADC} [26]

$$\Delta S_{out} < \Delta_{\text{ADC}} = \frac{V_{\text{ADC}}}{2^{N_{\text{ADC}}}}, \tag{16}$$

where V_{ADC} and N_{ADC} are the ADC's reference voltage and number of bits, respectively.

Digitally synthesized frequency is normally carried out by timers that are programmed to reset at a desired value, while maintaining a fixed 50% duty ratio [26]. The generated frequency can be expressed as follows

$$f_{\text{DCO}} = \frac{1}{N_{per}TB}, \tag{17}$$

where N_{per} is an integer and TB is the time base of the unit clock. The frequency resolution can be calculated as the LSB change in N_{per}

$$\Delta f_{\text{DCO}} = \frac{1}{N_{per}TB} - \frac{1}{\left(N_{per}-1\right)TB} \approx \frac{1}{N_{per}^2TB} = TBf_{\text{DCO}}^2. \tag{18}$$

From (18), it can be well observed that the frequency steps of the DCO are limited by the system clock frequency, and increase as the square of the operating frequency, i.e., at lower running frequency, the frequency resolution would be finer than what can be achieved at a higher frequency. In the case that finer resolution than the one obtained by the system DCO is required, an effective fast dynamics and low distortion frequency dithering procedure has been employed as detailed in [29].

C. Phase Detector

The phase detection for both the transmitter and receiver sides in this study has been realized as illustrated by Fig. 5. Typically in capacitive WPT systems the voltages of the resonators are significantly higher than the operating voltage levels of the controller periphery. Therefore, the input voltages V_P and V_{CP} (V_S and V_{CS}) are scaled down using a simple high-resistance divider network to a voltage level suitable for the phase detector unit. The sensed high-frequency scaled voltages are fed into a comparator that acts as zero-cross detector. Then, the digital represented signals of the zero-cross detection are fed into an exclusive-or operator (XOR).

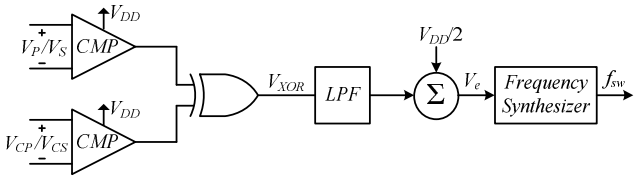


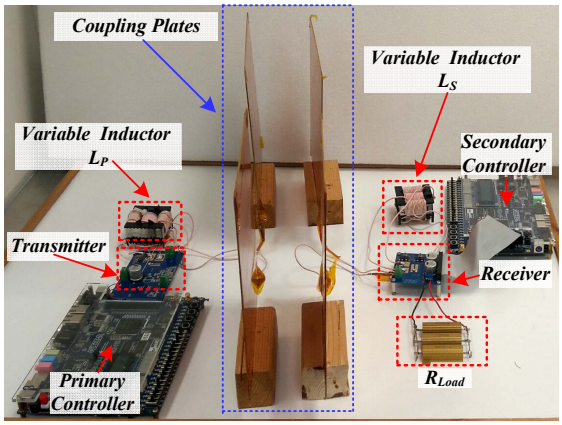
Fig. 5. Simplified schematic of the phase detector.

V. Experimental Verification

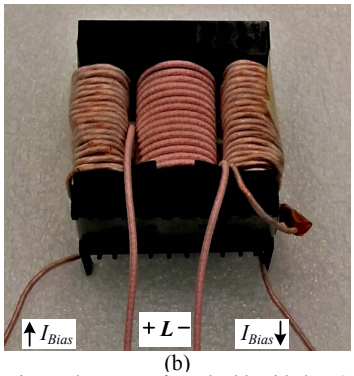
To validate and demonstrate the operation of the adaptive multi-loop controller, an experimental double-sided *LC* capacitive WPT prototype with four copper plates that form the capacitive coupling has been constructed as shown in Fig. 6a. In addition, Fig. 6b shows the custom designed variable inductor which comprises an *E*-core type ETD49 -3F3 magnetic element as discussed in detail in Section IV-A. The controller core have been fully coded in HDL and implemented on a Cyclone IV FPGA. For the various experiments in this study, the coupling plates have been designed symmetrically, such that each plate is 30x30cm. The matching networks have been also designed to be symmetrical; in nominal operation the inductors' values are set to $L_P = L_S \approx 75$ µH and the matching capacitors $C_P = C_S = 250$ pF. High-voltage multilayer SMD ceramic capacitors have been used for the matching capacitors. The operating frequency slightly above the resonance $f_0 \approx 1.2$ MHz, guaranteeing soft-switching. The full-bridge inverter has been realized with GaN power modules operable in several MHz. The overall nominal operating conditions and parameters of the experimental prototype are summarized in Table I.

The first step of the experimental validation has been carried out by characterizing the inductance of the variable inductor, and the resulting operating frequency of the CPT prototype as a function of the bias current. Fig. 7 shows the measured results for varying the bias current in the range of 0 to 2 A. It can be seen that in the vicinity of the nominal operating conditions the inductance and operating frequency f_0 are approximately 75 µH and 1.2 MHz, respectively, for a bias current of 0.5 A.

Fig. 8a shows the behavior of the primary's current I_P and the secondary's voltage V_S during tuning process for an input voltage V_{in}=30 V for an air-gap of 20 mm approximately. It can be observed that initially, the system is not tuned and the regulated current on the primary side has a higher peak amplitude compared to the one at the end of the tuning procedure. This is due to the fact that at the beginning the system is not calibrated and best operating conditions are not satisfied, thus undesired circulating current is drawn from the source. On the other hand, at the end of the tuning procedure the voltage V_S has a higher peak amplitude, since the system is calibrated to resonance and is operated under (local) optimal power transfer conditions according to the target current. Fig. 8b and Fig. 8c show a zoomed-in views of the tuning process with the waveforms of the switching nodes voltages and resonant currents upon initialization (Fig. 8b) and the end (Fig. 8c) of the tuning process. It can be seen that the switching frequency increases from 892 kHz to 1.2 MHz. The output parameters (I_S and V_S) also increase, delivering more energy to



(a)



(b)

Fig. 6. (a) Experimental setup of a double-sided *LC* capacitive WPT prototype; (b) *E*-core type based variable inductor.

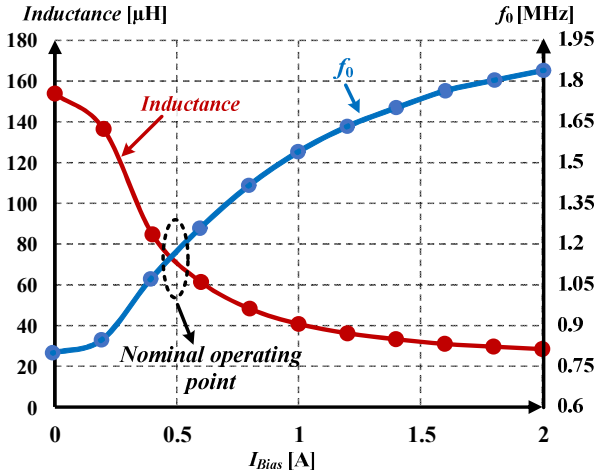


Fig. 7. Experimental measured inductance of the variable inductor and the resultant operating frequency of the CPT prototype as a function of the bias current.

TABLE I – Experimental Prototype Parameters at Nominal Operation

Parameter	*Value/Type*
Input voltage V_{in}	30 V
Output current	1 A
Coupling plates	30x30 cm
Air-gaps	15-100 mm
Full-bridge transistors	LMG5200, 80 V, 15 mΩ
Variable inductors L_P and L_S	~75µH
Capacitors C_P and C_S	250 pF
Operating frequency f_0	1.2 MHz

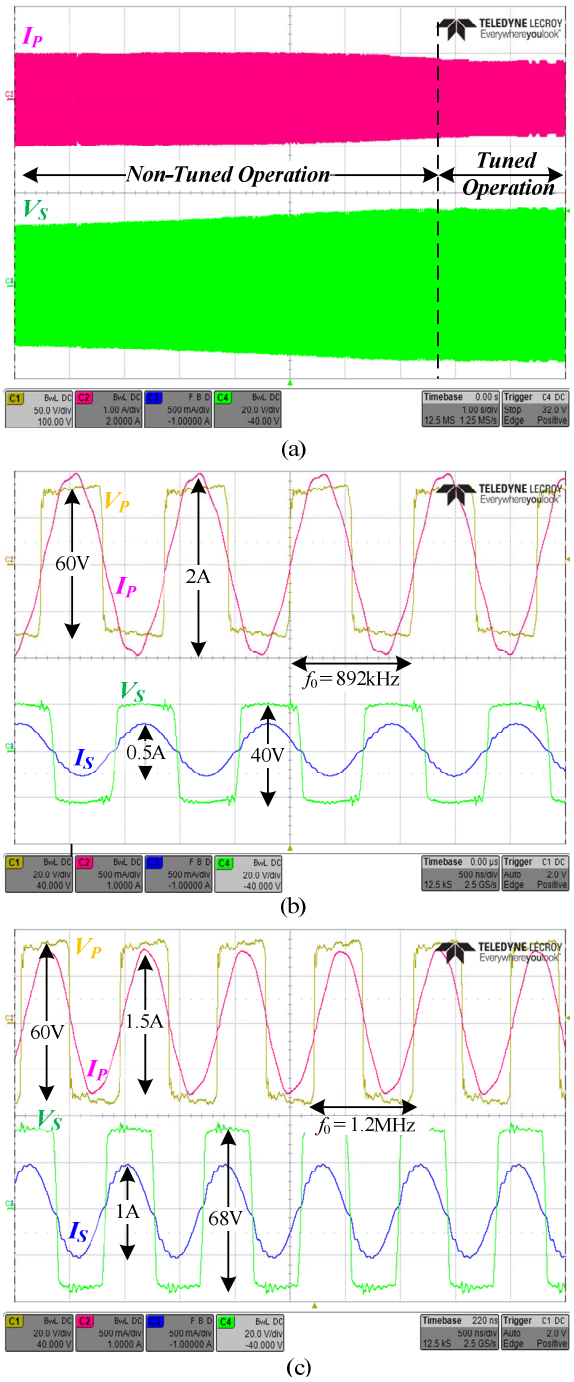


Fig. 8. Experimental results of the tuning process: (a) Full view of the envelopes of I_P and V_S, (b) Zoom-in view on the initial stage, (c) Zoom-in view on the final stage. Voltage scale 20V/div; Current scale 500mA/div; Time scale 500ns/div.

the load by more than 2.5 times. In addition, it can also be noticed that the primary current I_P is slightly lagging the primary voltage V_P, which is the necessary condition to enable soft-switching operation.

VI. Conclusion

An adaptive multi-loop regulated power transfer using tunable matching networks for resonant capacitive wireless systems has been detailed, analyzed and experimentally validated. The controller comprises of three main control loops, which effectively disengage the power transfer capabilities of CPT systems from any drift or variations, and further enables spatial freedom of the transferred energy from transmitter to the receiver. The control algorithm, signal flow and the functional relationships of the multi mixed-signal controller have been addressed. This study also introduced a variable inductor realization that enables continuous self-tuned impedance matching. To demonstrate closed-loop operation under system variations, an experiential resonant *LC* CPT prototype in the MHz range has been constructed. The new controller concept establishes the foundations for better power delivery in capacitive-based WPT systems.

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