# Multilevel High-Voltage Modular Rapid Capacitor Charger

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***Abstract*— This paper introduces a multilevel high-voltage modular capacitor charger. The unique architecture allows a single front-end to charge several capacitors connected in series with actively balanced voltages. Charge redistribution between the capacitors is carried out using a switched-capacitor balancing circuits. The system's multilevel structure, and modularity that stems from isolated design, enables charging of a distributed energy storage to very high voltages, while the component ratings and stresses are only a fraction of the total voltage. Using this approach, the designer is free to choose optimal energy storage and switching components, rather than using bulky, limited in options high voltage components. The architecture has been validated by simulations as well as on an experimental prototype of 1kW that has been constructed, validating capacitor charging to 1.2kV per module from a 12V input.**

**Keywords – charger, balancer, charging time, resonant converter, capacitor equalizer.**

## I. INTRODUCTION

Pulsed power applications are mostly implemented in a structure where high voltage, high power energy storage is discharged to the load [1]-[7]. The best candidate for high power energy storage is a capacitor, or bank of capacitors. The common implementation approach of these systems is selecting a high voltage single capacitor which is then charged to the voltage proportional to the amplitude of the pulse. Some obvious drawbacks of this approach include the fact that high voltage capacitors are large and bulky, rendering the design to be bulky as well. Another drawback is a complex high voltage capacitor charging power converter, required to charge the energy storage. To mitigate two of these down sides, a new multilevel high voltage modular capacitor charger architecture is introduced in this study (Fig. 1). Multilevel architecture enables the designer to select lower voltage capacitors and charging converter components, which are superior in size and power density comparing to their higher voltage counterparts, reducing the overall size and volume of the system. The modularity of the system enables to extend the voltage of the energy storage to much higher amplitudes than a single module, while still maintaining the advantage of the very low stress per component. The unique architecture utilizes cell equalization approach to keep the capacitors in the chain equally charged [8]-[23]. Additional advantage of the multilevel architecture is the ability to design multisource discharge pattern to accommodate multistage loads such as a

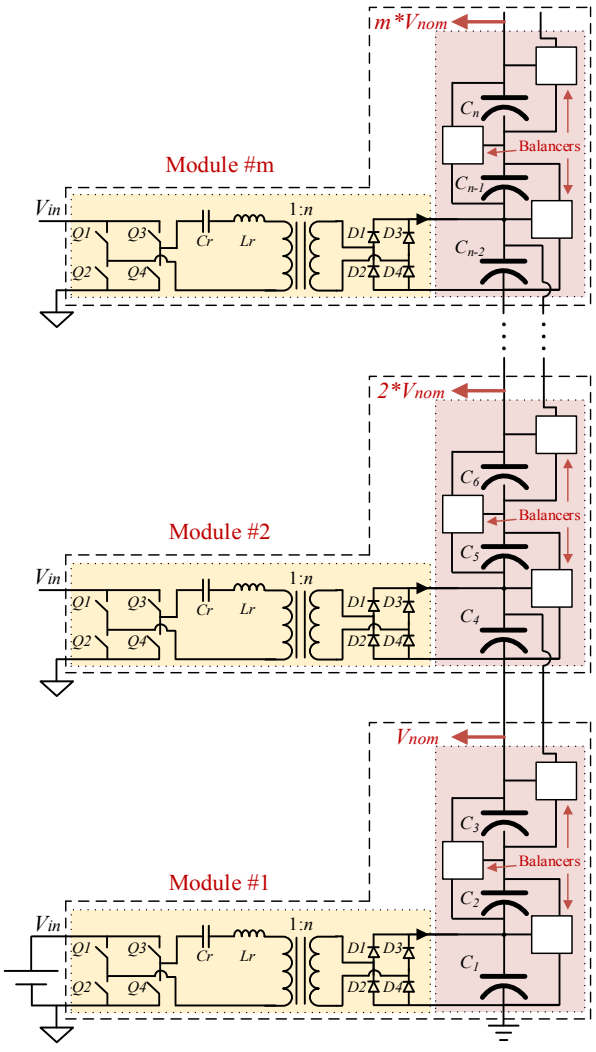


Fig. 1: Multilevel high voltage modular capacitor charger

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multi-winding magnetic acceleration device targeted in this study. The rest of the paper is organized as follows: section II describes system architecture, section III presents design and optimization considerations, section IV presents some validation results, and section V concludes the paper.

## II. System Architecture

### A. System overview

The system is built around *m* modules on top of each other, where each module has a number of serially connected storage capacitors, three in this study. The module consists of an isolated charging converter that is connected to a bottom storage cell out of a chain of serially connected energy storage cells. Storage cells employed in this study are capacitors to sustain high voltages, but from a topological perspective can be replaced by either supercapacitors or battery cells. The charging converter is programmed to transfer charge from the source to the bottom capacitor, limited by the maximum converter power. The chain of serially connected capacitors is interconnected with balancing circuits that are responsible to redistribute the charge from the bottom cell, receiving capacitor, to the rest of the cells in the chain. In this architecture, the charge from the source arrives to each of the serially connected capacitors, and is distributed between them. One extra balancing circuit per module is added to maintain equalization between the modules.

### B. Capacitor charger

There are several options to implement a capacitor charger [24]-[28]. As can be seen in Fig. 2, in this study the capacitor charger is built around a double bridge series resonant converter, where the input bridge is active (comprises of transistors), and the output rectifier is realized with diodes. Within the context of a capacitor charger, a resonant converter is preferred over a PWM type converter because of several factors: (a) regulation of charge transfer to the load; (b) operation in ZCS; and (c) the output impedance characteristics it presents to the output capacitor. A step-up transformer is used for both isolation and step up of the input voltage. The resonant tank consists of a resonant capacitor *Cr* and resonant inductor *Lr*, while leakage inductance of the isolation transformer can function as a resonant inductor [22], [29]. Capacitor charger operation is similar to a conventional resonant converter operated in DCM. The switching frequency, $f_s$, is set to be lower than the resonant frequency, $f_r$, i.e. $f_s < f_r$, to maintain DCM operation. An additional switch $Q_5$ is introduced to enable DCM operation at all time, and to avoid current back flow to the source. Current back flow takes place due to the large voltage difference between the input voltage and the output voltage mirrored to the primary during the charging operation of the system. Due to the high quality factor the resonant tank charges up and develops resonant capacitor voltage that exceeds the input voltage. High resonant capacitor voltage flips the direction of the resonant current during the dead time, forcing the body diodes of the active bridge MOSFETs to conduct. This condition results in energy loss and

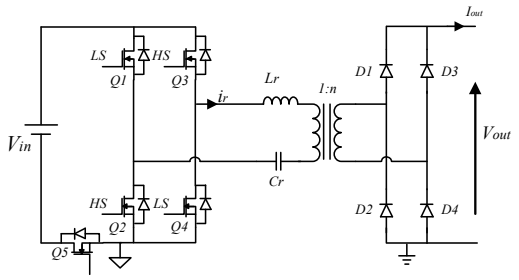


Fig. 2: Full bridge isolated capacitor charger

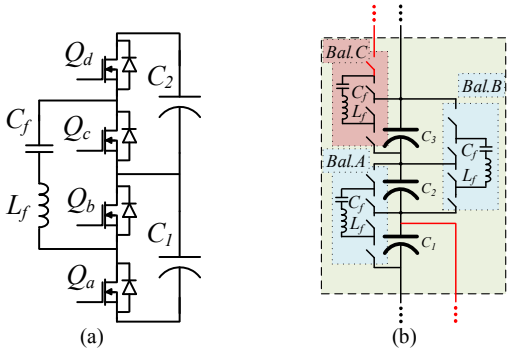


Fig. 3: Balancing circuits: (a) A single balancer schematic; (b) Balancers extra hardware for multimodule compatibility (balancer *C* and traces highlighted in bold red).

unnecessary current circulation that is overcome with additional switch $Q_5$, which is turned on and off under ZCS conditions.

### C. Balancing Circuit

To enable charge flow between the bottom capacitor, charged by the capacitor charger and the rest of the storage capacitors, a network of charge redistribution converters is used, the balancing circuits [8]-[23]. Each balancing circuit is built around a resonant switched-capacitor converter and designed to support two adjacent capacitors. Each balancer consists of two half bridges each in parallel to the storage capacitors, and a resonant tank, which is the switched capacitor cell. Each pair of storage capacitors has balancing circuit attached to it as can be seen in Fig. 3a. Running the switches at the resonant frequency of the switched capacitor cell with approximately 50% duty cycle enables voltage equalization of adjacent energy storage cells [9]-[13].

### D. Extension to m Modules

The multilevel capacitor charger employed in this study is compatible to be extended serially to increase the maximum voltage of the energy storage. Each unit that includes the charger and balancer is treated as a single independent module rated for a nominal voltage of $V_{nom}$ (Fig. 1). It becomes possible due to the isolation transformer used in between the primary and the secondary bridges of the double bridge charging converter, and independent operation of each of the modules, where balancing circuits equalize the cells within each module. Connecting in series *m* of these modules enables to extend the voltage rating of the energy storage. The primary side of each charger is connected in parallel to the voltage source, while the output part is connected in series to each other, (Fig 1), stacking the storage

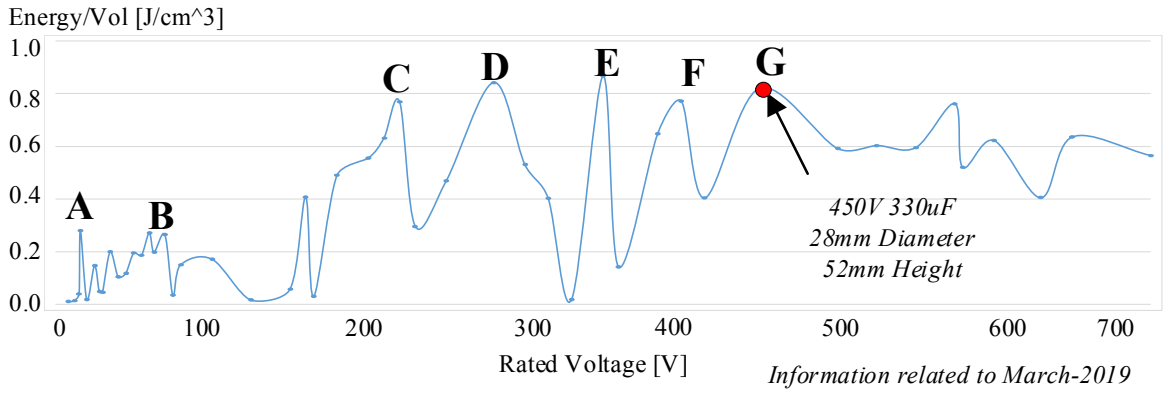


Fig. 4: Capacitor's energy density vs. maximum voltage rating

capacitor chains on top of each other. An extra balancing circuit, Balancer C, (Fig. 3b), is added to each module for serial connection compatibility. The extra balancer is in charge to equalize between the last storage cell of its own module and the first storage cell of the module above in the chain, maintaining continuous balancing along the whole serial stack of storage capacitors.

## III. Design and Optimization Considerations

### A. Industry inclined system optimization

Technology development in the modern world is majorly incremental, with rare exceptions that bring a break through and push us to a new technological level. In this environment, freshly invented technology becomes mature in a period of several years to a decade, and it is commercialized to support new or improved product. Commercialization process doesn't necessarily treat equally every application. Some applications are favored by higher consumer demand, or governmental legislation and standards. As a result, favored products get an increased interest and see increased incremental development over their peers from the same technology, until the next break through arrives.

An example of component selection based on industry inclined optimization related to this study, would be a selection of an energy storage, a capacitor, that occupies minimum space and supports maximum charge storage rated for 1.2kV. Fig. 4 demonstrates commercially available aluminum electrolytic capacitors spread, where the energy per unit volume is the performance metric, while rated capacitor voltage is the parameter. Several maximum performance points are outlined, which coincide with industry interest voltage ratings in the fields of automotive (12-24V point A in Fig. 4), data centers (48V point B in Fig. 4), and grid connected applications (250V for US points C and D in Fig. 4, and 350-400V for EU points E, F and G in Fig. 4). Examining Fig. 4, the capacitor at point G has been selected to achieve the best energy per volume for the maximum voltage of a 1.2kV. The approach is to connect in series 3 capacitors rated for 450V each that are optimized for the EU grid, to achieve 1.2kV. The common practice of selecting a single bulky capacitor rated for the maximum required voltage is the least favorable approach in terms of energy per volume. The same industry inclined optimization is true in regards to switching elements. Switches rated for 500V for example, are better in terms of power density than the switches for 1.2kV. To achieve the benefit of industry inclined optimization a unique multilevel modular architecture is required, similar to the one introduced in this study. Three serially connected capacitors constitute the energy storage of each module, to provide output of 1.2kV.

### B. Design considerations

The regulation approach of the charging converter used in this study is the Pulse-Frequency Modulation (PFM). Input voltage source is connected to provide current for a predefined time frame, the half resonant frequency period of the tank and the width of the pulse, $T_r/2$. Regulation parameter in this case is the switching frequency, which controls the density of the pulses and the amount of the processed energy. The ratio between the pulse width and the switching cycle length, $T_s$, is defined as $D = T_r / T_s$, where $T_r$ is always smaller or equal to $T_s$.

Next to the voltage considered as the full charge, and capacity of the energy storage, which are dictated by the application, the major parameter to be considered by a designer is the time available to charge the capacitor, $T_{chrg}$, which sets the nominal power and physical volume of the charger. To calculate $T_{chrg}$ for presented topology we make an assumption that the balancing circuits are lossless, and shuttle the charge instantaneously between storage capacitors, which is a reasonable assumption as long as the balancers are sized according to the required power level. As a result, the total output capacitance of the charging stage equals the sum of all the storage capacitors in the module, three times the capacitance in the case presented here. Averaging the net amount of charge provided by the charger to the output each **half** of its switching cycle, we calculate output voltage increment that took place from the end of the previous cycle. The increment, $\Delta V_{out}$ is a function of switching period and the average current:

$$\Delta V_{out} = \frac{I_{avg}}{C_{out}} \frac{T_s}{2}, \qquad (1)$$

substituting the expression for average current $I_{avg}$ into (1), voltage increment takes the form of:

$$\Delta V_{out} = \frac{2}{\pi} \cdot I_{r\_pk} \cdot D \cdot \frac{T_s}{2C_{out}} = \frac{2}{\pi} \cdot \left( \frac{V_{in} - \frac{V_{out}}{N}}{R} \frac{1}{N} \right) D \frac{T_s}{2C_{out}}, \qquad (2)$$

where $N$ is transformer's turn ratio. Finally rearranging (2) into (3) results in a straightforward expression.

$$\Delta V_{out} = \frac{D \cdot T_S}{N \cdot R \cdot C_{out} \cdot \pi} \cdot \left( V_{in} - \frac{V_{out}}{N} \right) \quad (3)$$

The voltage in $n$-th half-cycle can be calculated by adding the voltage at the previous half-cycle, i.e. $V_{out}[n\text{-}1]$, plus the voltage increment developed in (3):

$$V_{out}[n] = V_{out}[n-1] + K \left( V_{in} - \frac{V_{out}[n-1]}{N} \right) \quad (4)$$

where $K$ is the ratio between the output time constant and the switching period $K = DT_s / (NRC_{out}\pi)$ and $R$ is the total loop resistance including stray resistance, capacitor ESR, MOSFETs $R_{ds\_on}$ and inductor resistance. Applying (4) for each of the half cycles preceding $n$-th half cycle, an equation for the voltage $V_{out}[n]$ could be written, where a first member is the initial capacitor voltage $V_{out}[0]$:

$$V_{out}[n] = K \cdot V_{in} \left[ 1 + \left(1 - \frac{K}{N}\right) + \left(1 - \frac{K}{N}\right)^2 + \cdots + \left(1 - \frac{K}{N}\right)^{M-1} \right] + \left(1 - \frac{K}{N}\right) V_{out}[0]. \quad (5)$$

The expression in the square brackets in (5) is a geometric series, which can be rearranged to express the target charge voltage $V_T$ as a function of the number of half cycles $M$:

$$V_T = V_{out}[M] = K V_{in} \sum_{n=0}^{M-1} \left(1 - \frac{K}{N}\right)^n, \quad (6)$$

where $V_{out}[0]$ is assumed to be 0 volts, i.e. a charge from completely discharged capacitors. The sum of (6) has a finite expression:

$$V_T = N V_{in} \left[ 1 - \left(1 - \frac{K}{N}\right)^M \right]. \quad (7)$$

Rearranging (7) for $M$, the number of **half** switching cycles to charge the output capacitor to targeted voltage, $V_T$, can be summarized as:

$$M = \frac{\log\left(1 - \frac{V_T}{N V_{in}}\right)}{\log\left(1 - \frac{K}{N}\right)}. \quad (8)$$

Multiplying (8) by the switching **half** period and dividing by the duty cycle, the charging time to reach a target output voltage can be expressed as:

$$T_{chrg}(V_T) = \frac{\log\left(1 - \frac{V_T}{N V_{in}}\right)}{\log\left(1 - \frac{K}{DN}\right)} \frac{T_r}{2} \frac{1}{D} \quad (9)$$

where the resonant time is defined as: $T_r = 2\pi\sqrt{L_r C_r}$ . Equation (9) presents a finite and closed solution for the time required to achieve a certain final capacitor voltage, taking into account the changes in the charging conditions along the process.

To estimate the heat dissipation an efficiency calculation is carried out. The calculation considers conduction losses only. Since capacitor charging involves extremely wide variation in the output voltage the efficiency constantly changes with the rise of the output voltage. The efficiency of these systems lies in the range of a converter that operates in constant transient mode rather than a converter that operates in steady state, and expected numbers are hover around 30% or sometimes go even lower.

A calculation of an average efficiency of the charging process is based on per cycle efficiency calculation, and averaging of the results. The basic efficiency equation used is shown in (10):

$$\eta_{AVG} = 1 - \frac{P_{loss}}{P_{in}} \quad (10)$$

Input power and the losses are calculated in the similar way as described for $V_T$ in (6), using the finite sum of the geometric series. The number of switching cycles is $M/2$ as calculated in (8):

$$1 - \frac{P_{loss}}{P_{in}} = 1 - \frac{\frac{DV_{in}^2}{2R} \sum_{n=0}^{M} \left(1 - \frac{K}{N}\right)^{2n}}{\frac{2DV_{in}^2}{\pi R} \sum_{n=0}^{M} \left(1 - \frac{K}{N}\right)^{n}} \quad (11)$$

Rearranging (11) the average efficiency to charge the capacitors to the target voltage $V_{out}=V_T$ can be summarized as:

$$\eta_{AVG} = 1 - \frac{\pi}{4} \frac{1+q^{(M+1)}}{1+q} * 100\ [\%] \quad (12)$$

where $q = 1 - \frac{K}{N}$.

## IV. Simulations and Experimental Validation

To validate the theoretical concepts and operation of the system introduced in this study, a multilevel modular capacitor charger unit has been designed and fabricated. The validation of the concepts using numerical simulation is carried out and three modules of the multilevel modular capacitor charger are built and evaluated in numerical simulator PSIM. The schematic of the system follows the structure of Fig. 1, where three modules are stacked on top of each other, in parallel at the input, and in series at the output. Table I summarizes the main parameters of the system including the storage capacitors.

Basic charging operation waveforms are presented in Fig. 5 where a 90% duty cycle and 50% duty cycles are demonstrated.

Transformer resonant currents are shown in Fig. 6. Simulation results are presented in Fig. 6a, and experimental results are shown in Fig. 6b. Converter operation includes a main high peak sinusoidal current followed by a smaller resonant shape immediately after it. The second resonant

TABLE I – SYSTEM'S PARAMETERS

| ***Parameter*** | ***Symbol*** | ***Value/Type*** |
|---|---|---|
| *Input voltage* | $V_{in}$ | 12V |
| *Transformer ratio* | $N$ | 1:50 |
| *Resonant inductor* | $L_r$ | 1µH |
| *Resonant capacitor* | $C_r$ | 1µF |
| *Resonant frequency (charger)* | $f_{r1}$ | 160kHz |
| *Flying capacitor* | $C_f$ | 0.1µF |
| *Flying inductor* | $L_f$ | 1µH |
| *Resonant frequency (balancer)* | $f_{r2}$ | 500kHz |
| *Storage Capacitor* | $C_{out}$ | *330µF* |
| *DC Voltage rating* | $V_{DC}$ | *450V* |
| *Equivalent series resistance* | *ESR* | *1m*Ω |

shape is induced due to the high quality factor resonant tank that results in resonant capacitor voltage exceeding the input voltage during some time at the beginning of the charging process when the difference between the input and the output voltages is high. Since the gating of the charger allows some extra time to ensure zero voltage switching in the presence of resonant tank component variation, a reverse current flow from the capacitor is developed and creates a lower amplitude sinusoidal follow up. This follow up however, doesn't impacts efficiency, since it is rectified by the passive rectifier at the secondary side, and adds to the total converter energy transfer to the output. A good agreement between the simulation and experimental results as demonstrated in Fig. 6 was obtained.

A resonant tank voltage generated by the full bridge rectifier is presented in Fig. 7. Simulation results are shown in Fig. 7a, the current in the resonant tank is shown in red, and the voltage across it is shown in blue. Experimental results are presented in Fig. 7b. The waveforms in both simulation and experimental evaluations are within a close fit to each other.

The voltage and the current of the resonant capacitor, $V_{Cr}$, and $I_{Cr}$ at the begging of the charging process and at the middle of the charging process are presented in Figs. 8 and 9, respectively. The simulation results of $V_{Cr}$ are shown in Fig. 8a and Fig. 9a while the experimental results of $V_{Cr}$ are shown in Fig. 8b and Fig. 9b.

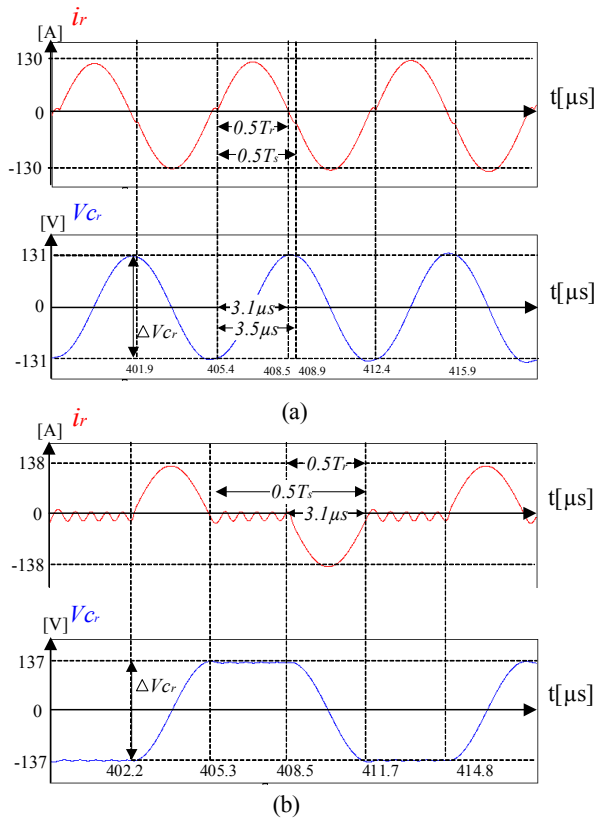


Fig. 5: Simulation of charging operation with: (a) $D$=0.9; (b) $D$=0.5.

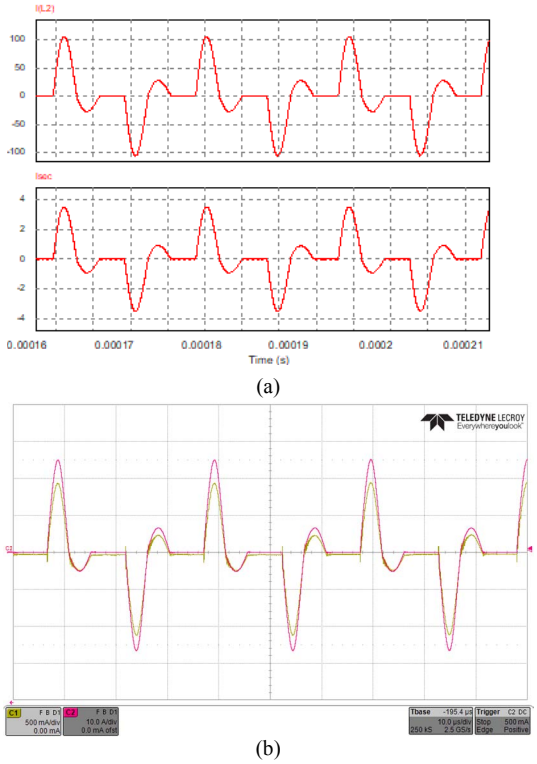


Fig. 6: Transformer resonant currents experimental vs. simulation results. (a) Simulation: primary current (top) 50A/div., secondary current (bottom) 2A/div.; (b) Experimental results: primary current (pink) 10A/div., secondary current (yellow) 0.5A/div.

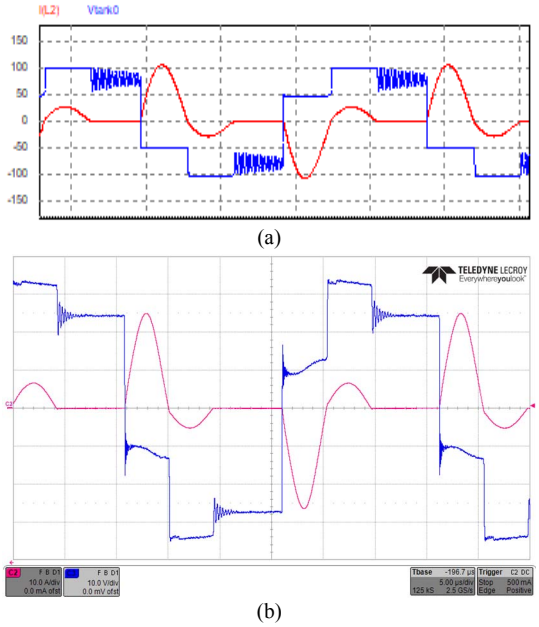


Fig. 7: Resonant tank voltage. Experimental vs. simulation results. (a) simulation results: transformer primary resonant current (red) 50A/div., resonant tank voltage (blue) 50V/div., (b) Experimental results: transformer primary resonant current (pink) 10A/div., resonant tank voltage (blue) 10V/div.

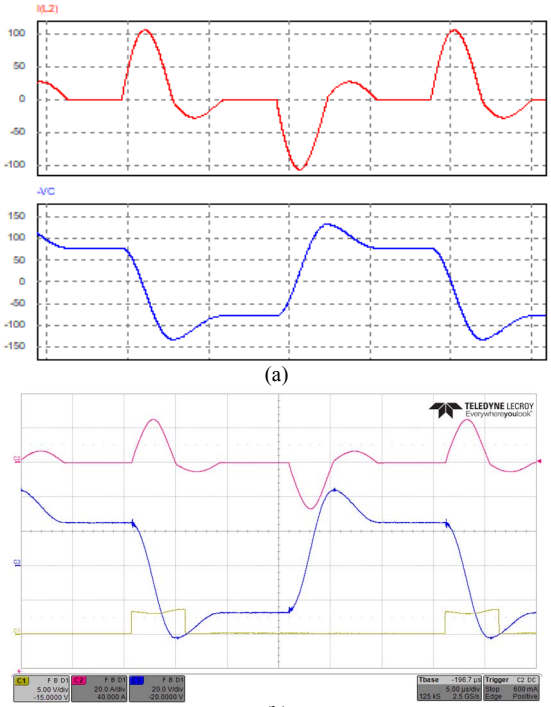


Fig 8: Resonant capacitor $C_r$ voltage and current at the beginning of the charging process: (a) Simulation results: from top to bottom: transformer primary resonant current 50A/div., $V_{Cr}$ 50V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 20A/div., $V_{Cr}$ (blue) 20V/div., gate signal ($Q_2$) (yellow) 5V/div.

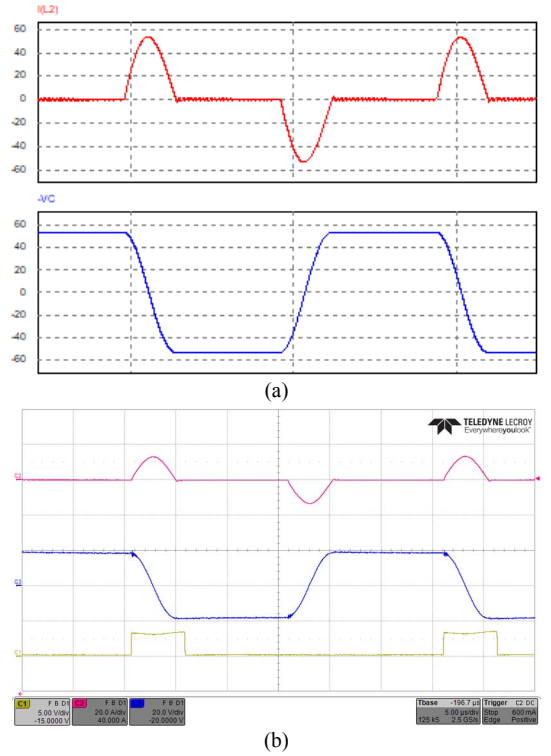


Fig. 9: Resonant capacitor $C_r$ voltage and current in the middle of the charging process, at 60% point to target voltage: (a) Simulation results: from top to bottom: transformer primary resonant current 20A/div., $V_{Cr}$ 20V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 20A/div., $V_{Cr}$ (blue) 20V/div., gate signal ($Q_2$) (yellow) 5V/div.

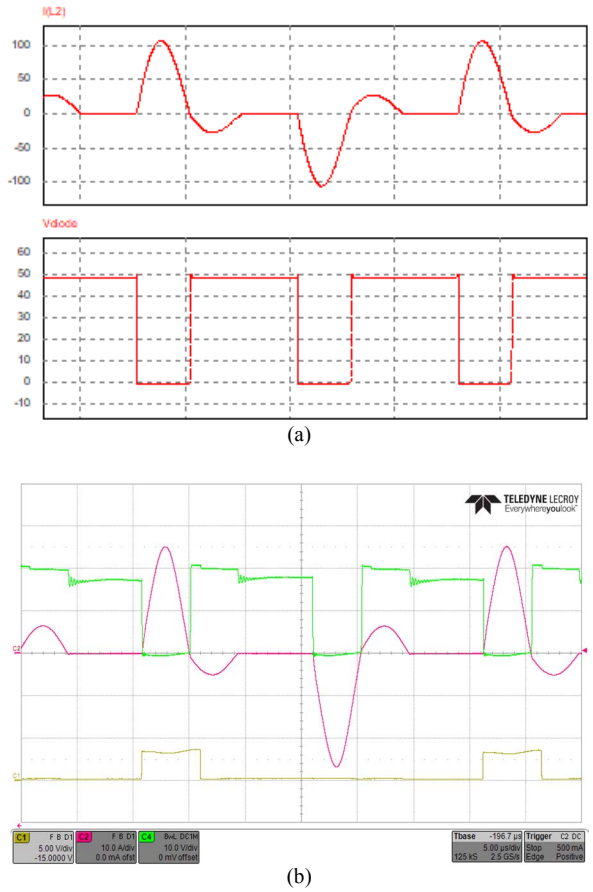


Fig. 10: Switch $Q_5$ (keeping DCM operation) drain-source voltage. Experimental vs. simulation results. (a) Simulation results. From top to bottom: transformer primary resonant current 50A/div., $V_{DS\_Q5}$ 10V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 10A/div., $V_{DS\_Q5}$ (green) 10V/div., gate signal ($Q_2$) (yellow) 5V/div.

The voltage stress across the switch $Q_5$ (see section II.a) is presented in Fig. 10. Simulation results are shown in Fig. 10a, and experimental results are shown in Fig. 10b. A good agreement is shown between simulation and experimental results. Full charging process experimental results were carried out with a prototype board as shown in Fig. 13. A storage electrolytic output capacitor of $C_{out}$=330$\mu$F is charged to $V_T$=300V off an input voltage source of $V_{in}$=12V with an average charging power of 25W and peak instantaneous power of approximately 70W. The charging current and output voltage are shown in Fig. 11a. A charge with an average charging power of 45W and peak instantaneous power of approximately 140W is demonstrated in Fig. 11b. A shorter charging time can be observed in Fig. 11b. Validation of charging time (9) using cycle-by-cycle simulation is shown in Fig. 12. Blue trace presents the target charge voltage and the time required to reach it as calculated by equation (9), while the stars represent cycle-by-cycle simulation results as were aquired in PSIM simulator. The minor discrepancy between the theoretical trace and simulation results is due to the assumption that the balancers are lossless.

## V. CONCLUSION

In this study a new architecture of multilevel high voltage modular capacitor charger is presented. The architecture is based on a double bridge resonant converter operated in DCM as a charger that is connected to a series of energy storage cells equalized with switched capacitor balancers. The unique architecture enables the designer to spread the stresses across several components and select optimal components as dictated by the industry, i.e. carry out an industry inclined optimization, and to avoid the common solution where full rating bulk components are chosen. Industry inclined optimization is discussed along with design considerations such as regulation, charging time and charging efficiency. An experimental prototype has been built and evaluated experimentally. The validation of system operation has been carried out using PSIM numerical simulation and experimental trials and found to be in an excellent agreement with theoretical premises.

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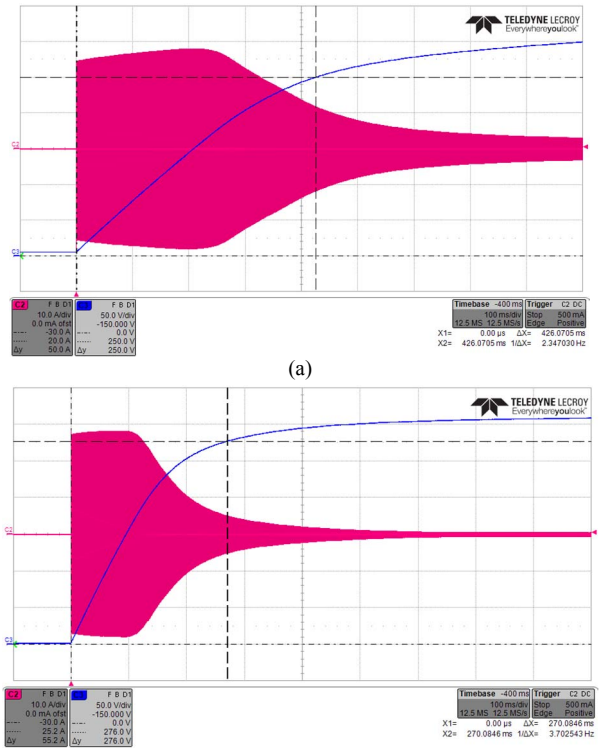


Fig. 11: Experimental results: full charge of output capacitor with $C_{out}$=330µF, $V_{in}$=12V, Transformer primary resonant current (pink) 10A/div., $V_{out}$ on $C_{out}$ (blue) 50V/div. with time scale: 100ms/div. (a) $D$=0.3, $P_{out\_avg}$=25W, $P_{out\_max}$=70W , (b) $D$=0.6, $P_{out\_avg}$=45W, $P_{out\_max}$=140W

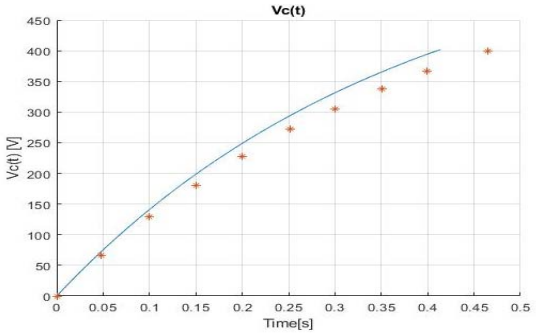


Fig. 12: Theoretical results of a single module charging times versus targeted output voltage with 3 capacitors in series, 330µF each. Blue trace is a model calculation, and discrete stars in red are the PSIM numerical simulation. Parameters are: $V_{in}$=12V, N=50, $D$=0.9, $C_{out}$=990µF, $R$=96mΩ

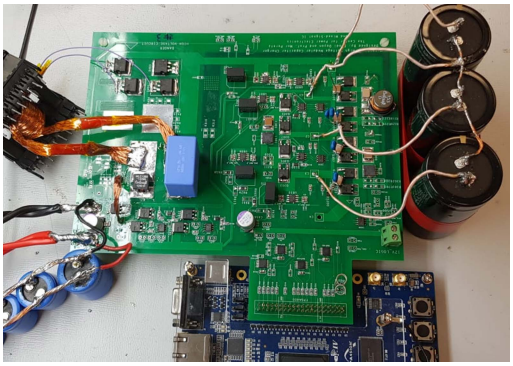

Fig. 13: Prototype board, including charger and balancer.

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