Digital Controller for High-Performance Multiphase VRM with Current Balancing and Near-Ideal Transient Response

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***Abstract* - This paper introduces a digital current-programmed control for multiphase buck VRM for high-performance loads that regulates the output voltage with high accuracy, maintains current sharing of all phases for the entire operation range, and achieves optimal transient recovery for load transients. These are enabled by hybrid controller architecture that facilitates per-phase average current control (ACM) for steady-state operation and a state-space based transient oriented controller that executes time-optimal or minimum-deviation recovery for loading and unloading transients. Active voltage positioning (AVP) as well as current sharing algorithms are embedded, covering all the required features to supply modern high-end loads. In addition to the high-end analog interface developed for accurate acquisition of the control signals, the digital core IP blocks (compensation, sharing, droop, etc.) and peripheral units (HRDPWM, ADC) are realized by combinatorial asynchronous logic, all with standard cells using HDL toward direct synthesis for IC implementation. The resultant compact controller (implemented on FPGA with total logic element count of 1700 elements for 4 phases) has been tested and successfully validated experimentally on Intel-certified hardware. The experimental prototype featured a 4-phase 12V to 1.xV buck VRM that drives an array of 7 DDR4 load modules, accommodating 100A load transients with transition rate of 1000A/µs, and demonstrating time-optimal recovery.**

Keywords – Digital control, hybrid control, multiphase, buck, VRM, controller, DDR

I. Introduction

With the proliferation of cloud computing, power consumption of datacenters has grown significantly [1]. Datacenters typically use a large number of CPUs and DDR memory modules, each requires a well-regulated dc voltage, under extremely strict requirements and specifications. Formed by the OCP standardization in recent years [2], the power processing chain of datacenters applications has a 48Vdc unregulated bus as the main source, which is then down-streamed to the load in two-stage converter architecture. The first stage is a 48V-to-12Vconverter to provide a 12V bus. The second stage is the high-performance 12V-to-1.xV voltage regulator module (VRM) back-end converter, which is typically implemented using a multiphase buck architecture. This is done to satisfy the load in terms of power quality requirements and in particular to assure a tightly regulated supply under intensive, rapid and consecutive load transients.

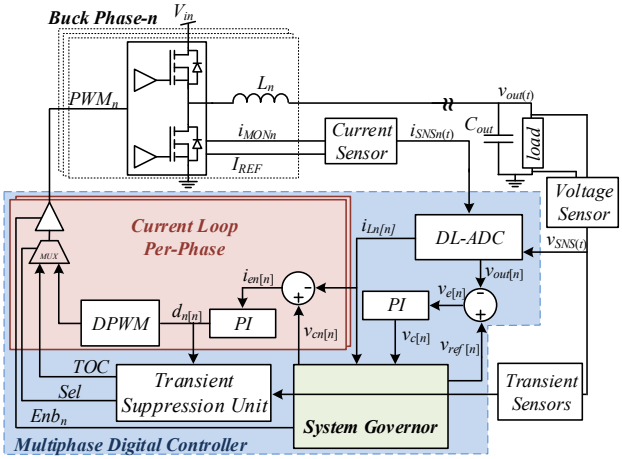

Fig. 1. Simplified schematic diagram of a multiphase buck system.

Multiphase interleaved buck VRM (MPVRM) enables low-voltage high-current operation [3]-[5], featuring high power density, high conversion efficiency [6]-[11] and fast dynamic response [12]-[16]. MPVRM can be ultimately used to relax the passive components requirements or to further increase the computing power. The conventional setup of a multiphase interleaved buck converter paralleling several phases to power the load. Typically, a single controller IC is employed to oversee the operation of all power stages. This allows better synchronization of the signals, data acquisition with higher signal-to-noise ratio, and saves PCB area.

Single-phase controllers are predominantly realized using analog implementation due to cost-performance tradeoff.

In applications of multiphase and in particular for VRM, digital control has taken the leading role and established its standing. This is primarily due to the fact that modern controllers require not only performance characteristics, but also flexibility, plug-and-play and programmability capabilities, several housekeeping, communication and telemetry features. Still however, the added penalty of implementing a digital controller

core is a non-negligible factor that stems from extreme hardware requirements to achieve the performance goals such as high base clock frequency, overall silicon area and power consumption, acquisition and control resolutions and more. These can be the result of the control architecture, implementation of the internal control blocks, peripheral units etc.

In the vast majority of MPVRMs voltage-mode control scheme with linear compensation is applied to facilitate regulation [17]-[22]. Paralleling and voltage positioning is achieved by droop control method [23]-[29], and per-phase current information is typically used for either sharing purposes or data collection [30]-[32]. Acceleration of the control bandwidth is facilitated by switching or transitioning between linear controllers, i.e., by adjustments of the compensator's coefficients according to the loading conditions [33]-[39]. Although a version of the per-phase current information is available to the controller, current-programmed mode control approach has been avoided from commercial applications hitherto.

Parallel connection of multiple power stages, operating in and out of phase, can form several challenges ranging from current and thermal distribution to producing different voltages for the same control as a result of different physical layout. Furthermore, since the phases are distributed over a sizeable portion of the PCB, meticulous tracing and interfacing are essential to carry on the power as well as the control signals from the individual phases to the centralized controller and back. In utilization like this, regulation of the per-phase current, as a concept, considerably reduces the complexity of the system. However, capture the instantaneous inductor current and manipulate the phase operation accordingly may be practically prohibitive from both sensing and control aspects. Here, the advantages of average current-mode (ACM) control approach are becoming more apparent [40]-[43]. Especially, in the case that it can be realized without additional hardware penalty. In ACM approach, some of the building blocks are identical for both the voltage and current loops, and therefore by using the same hardware, a significant reduction of the resources is achievable.

The objective of this study is therefore to introduce a new all-digital controller for high-performance multiphase buck VRM as shown in Fig. 1. The new controller includes current balancing modules that enable even load distribution between the phases. The outer voltage regulation loop encompasses a linear compensation for steady-state and small deviations, along with a large-signal transient suppression unit to mitigate large change in the load. In addition, a higher-level system governor overseas tasks of phase balancing, synchronization, load sharing and phase shedding. It is a further objective of this study to present in detail a new controller implementation that enables time-optimal transient recovery in multiphase regulators.

The rest of the paper is organized as follows, Section II describes the new controller architecture and its principle of operation, Section III delineates the large-signal compensation scheme. Practical implementation aspects and details of the system governor are provided in section IV. Experimental validation is carried out in section V. Section VI concludes the paper.

II. Controller Architecture and Principle of Operation

The multiphase buck VRM controller that has been developed in this study and illustratively presented in Fig. 1 consists of two main control units, a small-signal ACM controller and a large-signal transient suppression unit (TSU) incorporated together into a hybrid controller architecture [44]-[53]. Each controller is designed for superior performance within its control law operation. The TSU is designed to accommodate large load changes and utilizes a nonlinear, state-variable based recovery pattern to accomplish the best possible transitioning from one loading condition to another. The small-signal controller is structured around a current-programmed linear compensation scheme and operates in fixed-frequency PWM. By doing so, it enables simpler design of the power stage, and more importantly high steady-state accuracy can be achieved as well as high static efficiency, and good thermal distribution between the phases, which is important in the context of multiphase converters. Forming this type of hybrid controller structure provides flexibility, where the tasks are separated between the compensators. Load transients are remedied with time-optimal or minimum-deviation patterns, utilizing the advantage of paralleling phases to expedite the recovery process. The design of small signal linear compensator, encompasses minimum dc error, accuracy, and current sharing. This arrangement provides simplification of the design, and at the same time steady state features are retained and significant improvement in transient mitigation is achieved by the TSU. It should be noted that by defining the task of the transient controller to bring the state variables from the old state to the vicinity of the new state, while the task of the linear control remains regulation, the issue of the controller stability is inherently resolved and can be examined by conventional tools, such as Nyquist, or phase margin test [53]-[56].

Sensing diagram that is required to facilitate the hybrid controller is schematically detailed in Fig. 2. This is an important interface for any high-performance VRM and particularly in multiphase applications, since reliable acquisition of circuit parameters is pivotal for issues of accuracy, rapid timing, sensitivity to changes, and accommodating noise and other disturbances.

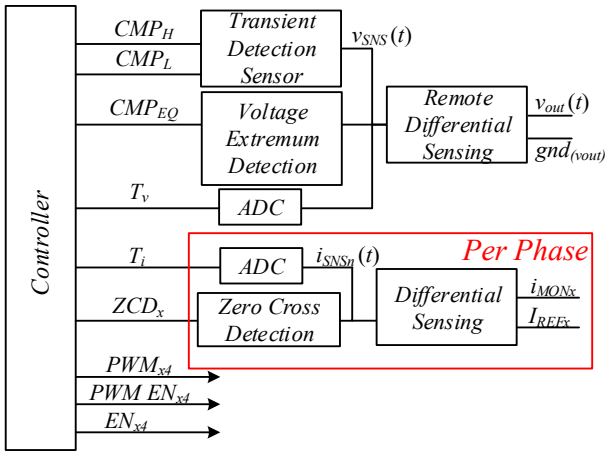

Fig. 2. Schematic illustration of the sensing scheme for multiphase controller operation.

The practice employed in this study, as can be seen from Fig. 2, is to employ a differential-type acquisition of the state-variable signals. By doing so, the distance from the measurement point to the controller front-end is compensated. Once the signal is obtained, it is further manipulated according to the required task (regulation, detection, information, etc.). Average value readings, i.e. one sample per cycle readings, such as information of the output voltage and the current of each phase, are processed by the steady-state controller. Continuous signal information of the output voltage is further manipulated by the TSU.

A fundamental challenge of multiphase architectures is the parallel connectivity of multiple power stages and the need to adequately distribute the efforts between them while maintaining a well-regulated voltage at the output. This mandates some form of current or load sharing protocol. In this study, average current-programmed mode (ACM) control for the operation of the steady-state compensation scheme has been pursued as can be seen in Fig. 3(a). Under the assumption that the control bandwidth of the current loop is sufficiently wider than that of the output voltage, the individual power stages that feed the output capacitance can be treated as controlled current sources as in Fig. 3(b). This enables multiple converter phase paralleling, simple adjustment of the phase currents, and therefore current sharing. Equal currents eventually result in even thermal distribution between the phases at no additional cost, which is important to multiphase applications.

Additional important feature of multiphase controllers required by the load due to the thermal restrictions when operating at high current [57], is active voltage positioning (AVP). A typical droop curve that represents the target v_{out}(t) level as a function of the load current i_{load}(t) is shown in Fig. 4. The output voltage level reduces as a linear function of the load current where V_{VID} defines the nominal output voltage at no-load conditions, and V_{min} is the required voltage at I_{max}. Droop control is implemented by shifting down the target reference voltage with load increase, and can be expressed as:

$$v_{ref}[n] = V_{VID} - R_{VID} \cdot i_{sum}[n]\,; \qquad (1)$$

where $v_{ref}[n]$ is the voltage loop reference, V_{VID} and R_{VID} are the user selected AVP parameters to fit the desired V_{VID} curve, and $i_{sum}[n]$ is the digital value of the total converter current. It should be noted that in order to avoid oscillations at the output and since the droop relates to the steady-state voltage level only, its bandwidth is significantly lower than the response of the voltage control loop.

The principle of operation of the ACM controller is described with the aid of Fig. 5 and Fig. 6, which show the conceptual block diagram of the ACM controller and its timing sequence diagram during steady-state operation respectively. Since this study focuses on all-digital implementation of the controller, the description is carried out with sample-data domain notations. The voltage loop creates a digital reference $v_c[n]$ for the inner current loops based upon the error signal $v_e[n]$ as given in (2):

$$v_e[n] = v_{ref}[n] - v_{out}[n]\,, \qquad (2)$$

where $v_{ref}[n]$ is the AVP generated reference and $v_{out}[n]$ is the sampled output voltage.

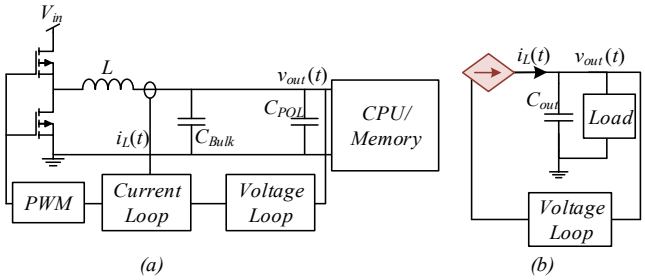

Fig. 3. Dual loop ACM buck VRM (a) current-controlled buck converter (b) equivalent diagram.

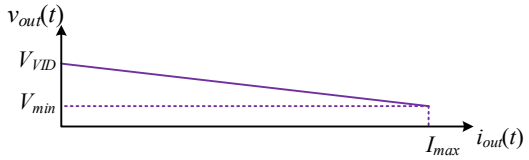

Fig. 4. Active voltage positioning VID curve required in high-end loads.

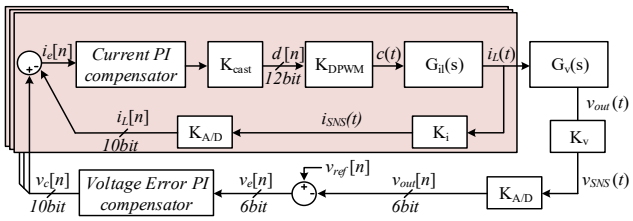

Fig. 5. Conceptual block diagram of the multiphase buck ACM control system.

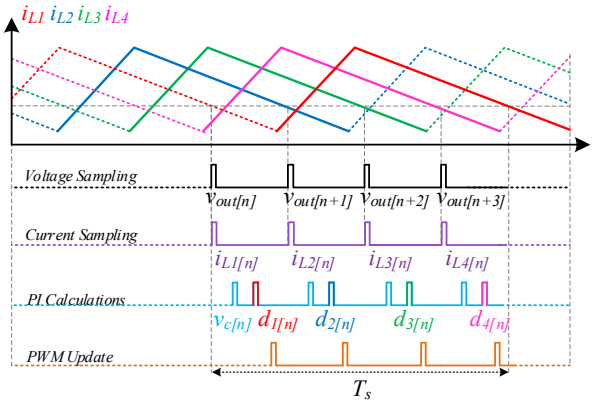

Fig. 6. Multiphase ACM controller timing sequence diagram of key blocks, during steady-state operation

The current error $i_e[n]$ is then calculated per-phase using the sampled average inductor current $i_L[n]$ of each phase. The current error $i_e[n]$ used as the input for the current loop compensator, which generates the duty command for the DPWM module $d[n]$, and a pulse width modulated signal $c(t)$ is formed.

In the classic approach for ACM control, the samples of $v_{out}[n]$ and $i_L[n]$ (Fig. 5), are sampled in a successive manner so that the resources of high-performance hardware such as ADC units can be shared, to save on power consumption and area. Furthermore, it is a common practice to position the sampling events away from switching actions to increase the measurement

signal-to-noise ratio. In interleaved multiphase systems however, switching events are scattered along virtually the entire switching cycle T_s and become more frequent with the number of phases, resulting in limited time slots suitable for data acquisition. To overcome this obstacle, this study formulates a unified data acquisition sequence that synchronizes per-phase measurements and gains the benefit of increasing the number of allowed interleaved phases to be limited by the acquisition time alone. Since the realization of the ADCs hardware in this study is carried out by delay-lines and combinatorial circuits as previously described in [58], the hardware penalty per phase is negligibly small.

A timing sequence diagram for the ACM controller is presented in Fig. 6, where $v_{out}[n]$ and $i_L[n]$ are both sampled at the same time. To utilize the enhanced bandwidth option of multiphase operation, the reference $v_c[n]$ signal is updated by the voltage loop compensator, the relevant phase duty command $d_n[n]$ is generated by the individual current loops and updated to its DPWM port at the beginning of each phase. By sampling $v_{out}[n]$ and $i_L[n]$ simultaneously at a fixed location within T_s, the timing logic in Fig. 6 can be duplicated and applied to accommodate any number of phases, limited by the data acquisition capabilities of the controller hardware.

Small load changes, defined within the range of the inductor current ripple (approximately 30% of the rated current) do not trigger the operation of the TSU and are accommodated through the steady-state compensation. Fig. 7 shows a typical response of the linear controller to a loading transient with four-phase operation (results obtained from PSIM simulation). Prior to the point t_{step} the controller is in steady-state, where each phase provides I_{low} to the output, sharing the load equally. At t_{step} the load changes so that each phase is required to carry I_{high}. Zoomed-in frame in Fig. 7 shows that the load step takes place between switching cycles of two adjacent phases. The small-signal compensator responds to the transient event immediately as the next closest phase cycle begins, at t_{update}. This is a much quicker response than the conventional practice, where the controller waits for a full switching cycle to complete. During the transient period, and under any transient conditions the ACM architecture of the small-signal compensator maintains current sharing between the phases, reducing the current sharing convergence time to zero, and the output current is fully shared when the system is back to the steady-state operation.

III. Large-Signal Compensation Scheme

Hybrid controller architecture facilitates a large-signal recovery pattern to suppress extreme transient events which exceed the regulation capabilities of the linear, small-signal compensator. Effectively, the limitations of the transient-oriented controller are the slew-rate imposed by the passive components, and the delays of the system (detection, calculation etc.) [48],[59]-[62]. Typical waveforms of transient recovery are depicted in Fig. 8 (obtained by PSIM simulation), demonstrating a loading transient event, followed by an unloading transient event as the load changes between the values of I_{low} and I_{high} respectively. The details of the transient and extremum detection sensors as used in this study are shown in Fig. 9 [43].

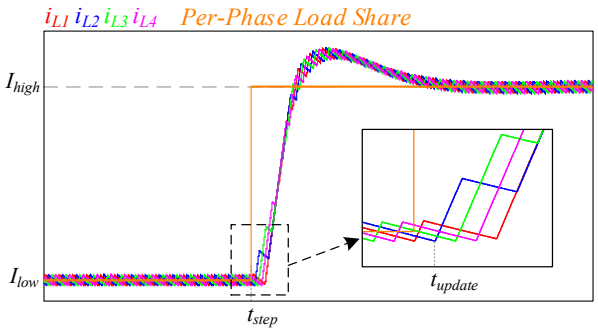

Fig. 7. Loading transient recovery of four phases interleaved buck converter controlled by linear compensation scheme.

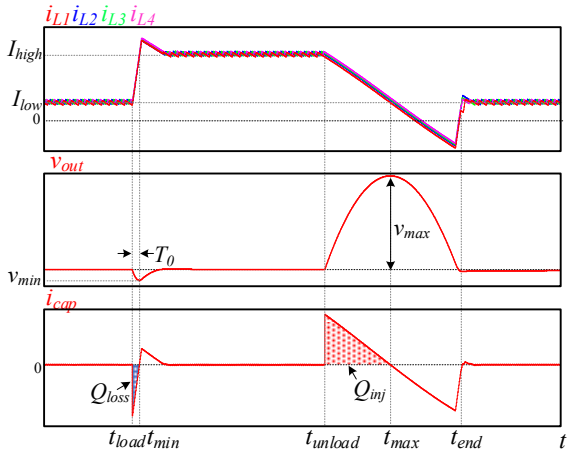

Fig. 8. Large-signal compensation waveform during loading and unloading transient events.

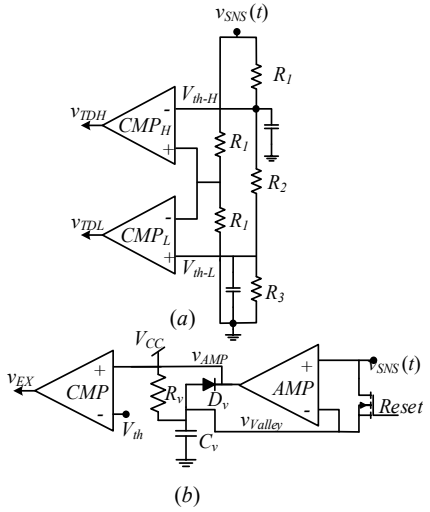

Fig. 9. Large-signal compensation sensors (a) transient detection sensor (b) output voltage extremum point detector (minimum).

Prior to the first transient event, the output voltage is within the steady-state window defined by V_{th-H} and V_{th-L} (Fig. 9 (a)) and controlled by the steady-state controller. At the time of t_{load} the load increases to I_{high} and the output voltage decreases, which triggers CMP_L. Past this point, the operation of the steady-state controller has been halted, the large-signal compensator takes over the control of the gating outputs and forces all available

phases to turn on. The time duration (T_0) between transient beginning and the point of output charge balance, is measured using a counter. The charge balance point manifested at the output voltage as an extremum point. Given that T_0 is attained by the controller the rest of the operation can be completed with a single on-off switching cycle as demonstrated in [44]-[49], to fully recover the output voltage back to its nominal value. In the unique case of loading transient, where the small inductors greatly increase the total system current slew rate producing faster transient response and virtually no voltage drop at the output, a minimum deviation approach can be implemented instead of the full TOC operation. Beyond this point, the control is returned back to the steady-state controller that maintains the operation at the new steady-state conditions.

In opposite to the loading transient event, the case of unloading transient present a more challenging task due to the low current slew rate which prolongs the transient recovery time. The result of the current slew rate mismatch is shown in Fig. 8 as the voltage overshoot caused by the unloading transient v_{max} is far greater than the voltage undershoot v_{min}, therefore a longer off time is required to bring the output voltage back to its nominal value. In some cases, the output capacitor is actively discharged by the multiphase VRM as the inductor currents turn negative to further induce the transient mitigation process. The output capacitor current i_{cap} shown in Fig. 8 can also demonstrate the differences between the two transients as the charge loss during loading transient Q_{loss} is recovered quickly in comparison to the injected charge Q_{inj} in the unloading transient.

The current ramp up/down phase in the large-signal compensation can be implemented with different levels of phase synchronization during transient. Fig. 10 shows three options for ramp-up initiation with and without phase synchronization, each with its pros and cons. The first option in Fig. 10 (a) maintains phase synchronization while also addressing the transient with the closest phase available upon detection, in this case the dashed line phase continues its ON state immediately upon transient detection. The second option in Fig. 10 (b) is to maintain full phase synchronization during transient when each phase is turned on at the beginning of its next cycle respectively. The third option is to turn all available phases as soon as transient event is detected, as a result, this method presents the poorest phase synchronization, nevertheless the transient performance is superior in comparison to the first two methods. When looking into the current sharing attribute during transient time the latter option maintains good current sharing, while the worst current mismatch possible is the size of the current ripple.

In this study the method described in Fig. 10 (c) is chosen due to the fastest transient performance as well as current sharing attributes. Another advantage of this method is that during a transient event, the system can be treated as a one single phase buck, with effectively increased bandwidth and with effective inductance of L_{eq}, given by $L_{eq}=L_{ind}/N$ (N represents the number of active phases).

IV. Practical Implementation Aspects and System Governor

In addition to the regulation requirements carried out by the hybrid architecture, and described in previous sections, state-of-the-art multiphase controllers are required to accommodate

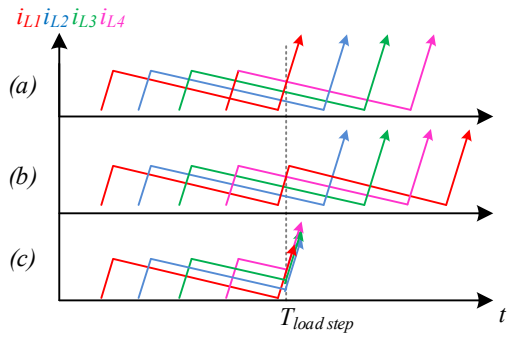

Fig. 10. Phase synchronization during transient current ramp up.

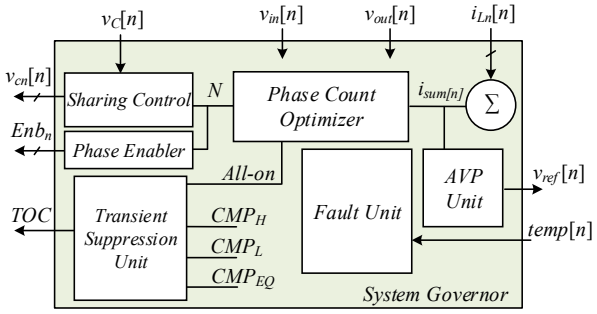

Fig. 11. System governor block diagram.

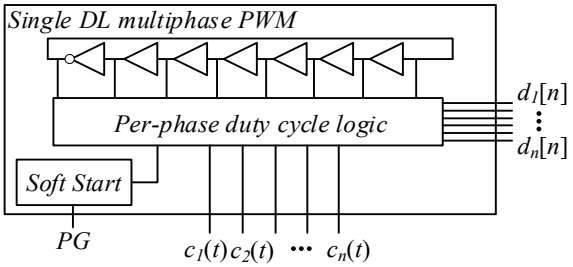

Fig. 12. Single DL multiphase DPWM module with built-in soft start unit.

high-performance loads with additional features like AVP and Fault management. In this study, the additional features are carried out by the system governor unit shown in Fig. 11. The system governor collects information of the following system variables: input voltage $v_{in}[n]$, output voltage $v_{out}[n]$, temperature $temp[n]$, and inductor currents $i_{Ln}[n]$. Using currents $i_{Ln}[n]$ the total inductors current $i_{sum}[n]$ is calculated every cycle. The AVP function, presented in section II, can be calculated using the total inductor current to dynamically adjust the voltage loop reference $v_{ref}[n]$ (Fig. 11). It is done to reduce the converter output voltage in high-currents operation.

An additional important feature carried out by the system governor is dynamic phase shedding. By changing the number of active phases during steady-state operation according to the loading condition, the overall converter efficiency can be further increased. The dynamic phase shedding is performed using the phase count optimizer (PCO), sharing control, and phase enabler are shown in Fig. 11. During a long steady-state operation, the PCO compares $i_{sum}[n]$ with a user-selected thresholds table to decide the N value, number of active phases, to the existing loading condition. In high output current operation, more phases are needed, so N is increased, the phase enabler determines the

relevant phase to be turned on by controlling the phase tristate output buffer (Fig. 1). After the phase has been enabled, the sharing control adjusts the relevant phase duty command to integrate the phase. This is done in a slow controlled fashion to prevent the system from going into transient during phase insertion. In low current operation, the phase is shed out by the sharing control unit before it is disabled by the phase enabler when the phase current reaches zero. During the transient event the phase shedding feature is disabled by the *All-on* signal form the TSU and force N to be changed to its maximal value, this is done to use all the available phases during transient assuring the best transient response.

Practical implementation of multiphase systems suffers from any imbalance between the different phases impacting the current sharing quality. A DPWM model based on multiple DL realization, especially on an FPGA custom designed modules, can introduce non-identical PWM signals for two different phases under the same duty command. The signal DL multiphase DPWM realized in this study as shown in Fig. 12 is based on a single DL ring oscillator to generate the PWM signal to all the phases. Given a duty command $d_n[n]$ a $c_n(t)$ signal is generated using the DL ring oscillator and the duty cycle logic. The single DL design cancels out the system sensitivity to both synthesis and silicon level differences between multiple modules. In the presence of very small inductors and very large output capacitance in multiphase systems, a soft start unit is essential to prevent any startup current or voltage overshoots and bring the system into the steady-state thresholds. The soft-start unit is incorporated into the DPWM module (Fig. 12) and provides a power good indication after soft start completion.

V. Experimental Validation on Multiphase Buck Converter

The multiphase buck VRM controller operation has been validated using a 12V-to-1.xV four-phase multiphase buck converter, an experimental prototype with all the analog front-end peripherals has been built and tested. The converter parameters are shown in Table I. Fig. 13 shows the experimental prototype setup, which comprises a specifically designed PCB to supply DDR memory, digital controller realized on FPGA, and an Intel-certified DDR4 load emulation modules. Each DDR4 module capable of sourcing or sinking up to 14A and the gating signal pattern is generated by a signal generator, asynchronous to the controller operation. The load slew-rate utilized in the experiments is 1000A/µs. The digital hybrid controller architecture, system governor, and custom-made peripherals such as the DL-ADC and single delay-line multiphase PWM has been entirely implemented on a Cyclone V FPGA.

Fig. 14 shows the transient response handled by the small-signal compensator of a loading transient event from 16A to 88A. i_{L1} and i_{L2} represent the inductor currents of phase 1 and phase 2 respectively, stepping up from the average current of 4A each to 22A each as the load changes. The output voltage at the load point is denoted as v_{out} and shows a maximal voltage deviation of 350mV and a full recovery period after 220µs. The small-signal controller maintains current sharing between the phases for the entire transient mitigation period.

In Fig. 15 the large-signal compensation scheme is activated to mitigate a loading transient event from 16A to 88A. Here, the controller realizes minimum-deviation recovery profile with output voltage v_{out} deviation of 30mV and recovery to steady-state within 12µs. TSU operation demonstrates excellent current sharing during transient and during the transition back to the steady-state controller.

The unloading transient case is demonstrated with an 88A to 24A load step as shown in Fig. 16 (small-signal compensation) and Fig. 17 (TSU). While the overshoot obtained by the linear compensation scheme is measured at 360mV and recovery within 300µs, the transient-oriented recovery resulted in 43mV with recovery time of 7µs.

TABLE I – Experimental Prototype Parameters

Parameter	*Value/Type*
Input voltage V_{in}	12V
Power Stage	SiC820, 70A
Inductor	120nH
Output capacitance, C_{out}	5mF
Switching frequency, f_{sw}	900KHz

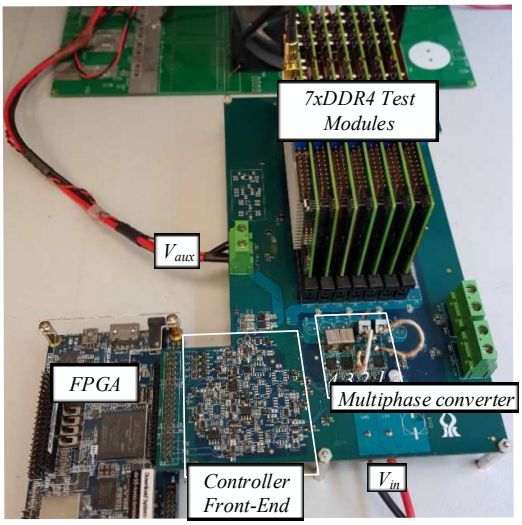

Fig. 13. Four-phase multiphase buck VRM experimental setup, including all the front-end peripherals and seven DDR4 test modules.

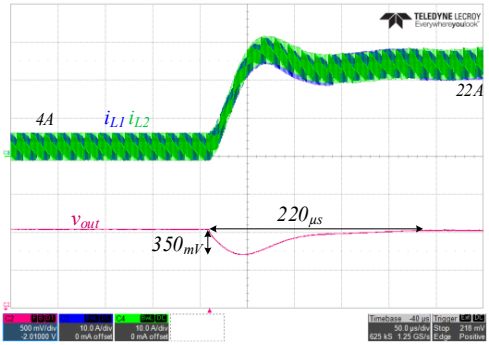

Fig. 14. Small-signal compensator operation during a 16A → 88A loading transient event.

VI. Conclusion

A digital hybrid controller for high-performance multiphase buck VRM has been demonstrated using a four-phase experimental prototype and a DDR4 emulation test modules. The hybrid controller architecture incorporates two main control laws, a per-phase ACM controller with current sharing capabilities for steady-state and minimized steady-state error, and a TSU for optimal load transient response. Control features such as phase shedding and AVP are implemented in the system governor to facilitate the efficiency and regulation requirements of high-performance loads like CPUs and DDR memories.

The experimental 12V-to-1.xV prototype has been validated using Intel-certified load emulator and demonstrated optimal transient mitigation capabilities of the TSU under extreme transient conditions. Both the ACM steady-state controller and the TSU show excellent current sharing attributes during the entire operation of the controller.

Acknowledgments

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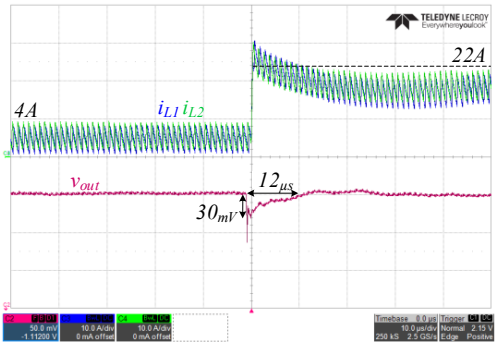

Fig. 15. Large-signal compensator operation during a 16A → 88A loading transient event.

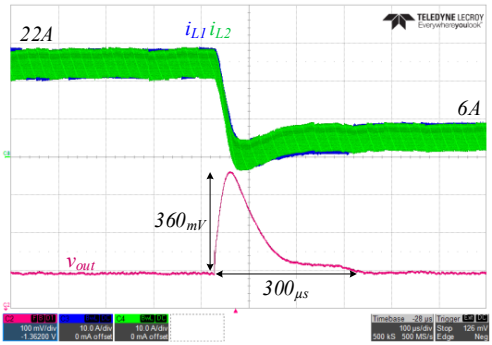

Fig. 16. Small-signal compensator operation during an 88A → 24A unloading transient event.

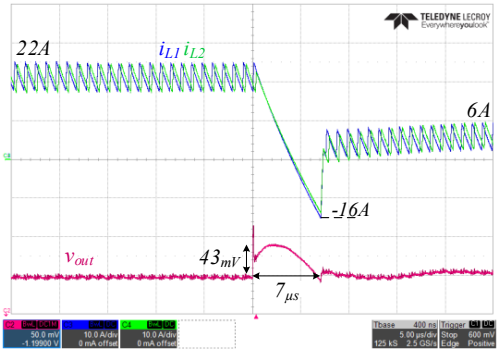

Fig. 17. Large-signal compensator operation during an 88A → 24A unloading transient event.

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