# Digital Lock-In Controller IC for Optimized Operation of Resonant SCC

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***Abstract* – This paper introduces a lock-in integrated controller for resonant SCC. The controller identifies the resonant period of each sub-circuit on-the-fly and locks-in to the correct switching time to fully utilize the charge transfer rate for each flying capacitor. The various modules of the controller are detailed, including the auto-tuner and sequencer which accommodate any mismatch, variations or drifts of component values or circuit configuration. The IC has been designed and fabricated on a 0.18$\mu$m 5V process resulting in effective silicon area of 0.64mm$^2$. Post-layout results of the controller IC operating in closed-loop are provided, demonstrating accurate lock-in for two resonators with individual independent resonant characteristics. A full-scale hardware prototype of 650W 4:1 switched-tank-converter is used to validate the controller's operation prior to IC fabrication, demonstrating excellent lock-in capabilities resulting in high efficiency of up to 98.6%.**

**Keywords – switched capacitor, ZCS, resonant converter, soft switching, integrated circuit**

## I. Introduction

Switched-Capacitor Converters (SCC) which have been rigorously explored over the last two decades [1]-[10] have established a dominant role in power management in datacenters and other cloud computing related applications. In light of the acceleration of the standardization of the power delivery structure that has been heavily affected by the trend-leading open-computing-project consortium (OCP) [11], the necessity to step the 48V rail down to 12V with extremely high efficiency and very high power density has established an application stand point at which SCC technology and its derivatives is highly superior over the inductor-based alternatives.

Power density and conversion efficiency are of key importance in datacenters applications (to maximize the amount of computing power per volume). This translates onto extremely strict conversion performance requirements at the 48V-to-12V level so that it would not further deteriorate the attractiveness of the overall solution. Since this application calls for a fixed conversion ratio, SCC technology renders a very attractive candidate. At medium power levels, SCCs have widely demonstrated peak efficiency over 98% [12]-[13].

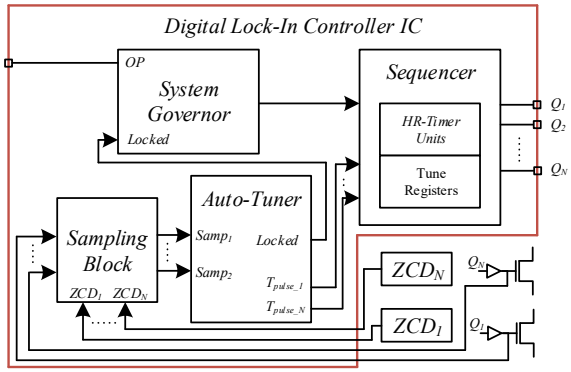


Fig. 1. Simplified schematic diagram of the digital lock-in controller IC.

Results of resonant SCC (RSCC) based power converters for datacenters applications, demonstrating peak efficiency of 98.5% around 200W have been recently presented [14]-[16].

The primary factor that facilitates efficient power conversion for the general case of RSCC is the accuracy of the switching frequency with respect to the resonant conditions of the converter. Optimal charge transfer is achieved in the case that the conduction time of each switching state matches exactly half of the resonator's period, and that deadtime between switching states is minimized [17]-[18]. In this way, the charge of the flying capacitor is fully utilized every cycle. Converter topologies with more frequent charge transfer of the output such as [19] inherently feature lower equivalent resistance, and as a result potentially more efficient than topologies with the basic charge-discharge pattern [20].

In topologies that comprise multiple switching states to complete a charge cycle [21], or in configurations with multiple resonators, full utilization of the charge out of each flying capacitor, every cycle, introduces complexity to the circuit controller. This mandate accurate zero-crossing information of the flying capacitor current and specific timing settings per switching state (and in some applications, per individual switch). This is since the conduction path is different for every state, which changes the resonant period. The resonant parameters per sub-circuit vary as a function of the stresses on the component, loading conditions, the physical layout of the design, and drifts with temperature and over time. In addition, the timing parameters need to account for variations and the accuracy of the current zero-crossing

detection circuit (ZCD). It would be extremely advantageous to utilize a controller which obtains the ZCD information, identifies on-the-fly the resonant period for each sub-circuit, locks-in to the correct switching time, and is capable of automatically compensate to any variation of the circuit – This has been pursued in this study.

The objective of this study is therefore to introduce a lock-in integrated controller architecture that facilitates accurate switching timing to fully utilize the charge transfer for each flying capacitor at every switching state as schematically illustrated in Fig. 1. The controller adjusts to accommodate any mismatch, variations or drifts at component values or the circuit configuration. It is a further objective of this study to present an all-digital IC implementation of the lock-in switching governor and detail the fundamental building blocks. Two lock-in architectures are presented and described in detail. One based on synchronized digital hardware and suitable for medium frequency range applications (in the range of several hundred kHz) whereas the second method is based on asynchronous combinatorial logic and features very high frequency resolution which qualifies to the MHz range. The control method is demonstrated for two resonators, with individual independent tuning per sub-circuit and switching state.

The rest of the paper is organized as follows: Section II describes the controller architecture and details its operation and the specific structure of the integrated units. Section III details a case study on a 4:1 switched-tank converter, covering the full circuit details, operation of the controller on the specific converter as well as the details of the ZCD acquisition method. System level and performance challenges are discussed in Section IV. Section V provides experimental validation on a discrete prototype and post-layout analysis carried out on the IC sent for fabrication. Section VI concludes the paper.

## II. Digital Lock-In Controller

The digital lock-in controller illustrated in Fig. 1 is described in this section in a general form and can be applied to various types of RSCC-based single or multi-stage converters topologies. The controller comprises the following modules as depicted in Fig. 1 (described in-detail in the subsections below): a) a system governor to manage, synchronize and dictate the operation mode; b) auto-tuner unit to adjust and calibrate the conduction time of the switches to achieve ZCS operation in all resonant tanks; c) switching sequencer to generate the required drive signals to the power switches; and d) a sampling block for accurate reading of the zero-current-detection (ZCD) sensors' outputs.

One possibility for tuning the drive frequency to the resonant characteristics can be performed by immediate response to the information from the zero-crossing point sensor [22]-[23]. This method may be problematic for some cases due to latencies and delays in the system. An alternative approach that is utilized for high switching frequency applications [24] performs delay-locked-loop convergence of the switching frequency to the resonant one. Such utilization, as employed in this study, locks in to the desired running frequency and compensates for any variations or mismatches in the system. This operation suits well resonant conversion, in particular at high-Q, since the response of the system to variations is rather slow and carries on over several switching cycles. In the specific case on-hand, as described in this study, the main motivation of the tuning comes from thermal considerations, to achieve optimal transfer conditions which result in the highest efficiency conditions in the system, is a relatively slow-varying objective that can be fulfilled well with a lock-in tuning architecture.

The tuning process is performed by the relatively slow internal clock of the controller IC, resulting in a simple and straightforward realization of the *Sequencer* and the *Sampling* blocks. For converters operating at higher frequencies, the frequency detection and generation units have been realized through asynchronous combinatorial logic to enable operation with higher resolution than of the one obtained by the internal synchronous clock.

### A. System Governor

The governor module dictates the desired operation mode of the converter, based on auxiliary configuration (OP in Fig. 1). In the private case for a conventional RSCC, the governor decisions include light-load operation of the converter, start-up and turn-off sequences as well as the applied dead-time. For more complex topologies, the system governor may dictate various switching schemes to minimize on-board periphery such as ZCD sensors in multi-stage converters, and even to determine the voltage conversion ratio. In this study, all synchronization actions performed by the system governor are based on an internal clock (in the specific case is 20MHz). A feedback from the auto-tuner block (*Locked* in Fig. 1) provides the governor with the required information regarding the tuning process. To support wide range of resonant converters, start-up and turn-off sequences can be re-programmed with no hardware modifications.

### B. Auto-Tuner

The auto-tuning module consists of several internal units, as shown in Fig. 2a. A digital compensation unit evaluates the sampled ZCD signals and determines whether the resonator current is zero when the transistor turns off. Non-zero resonant current at transistor turn off will occur in case of 'early' or 'late' switching as illustrated in Fig. 3. Based on the information of the polarity of the current at turn-off, the compensator modifies the on-time for each resonant tank separately ($T_x$ in Fig. 2a). The on-time of the next switching cycle is increased in case the sampled ZCD signal indicates 'early' switching and decreased in case of 'late' switching indication. Once the sampled signal of the ZCD indicates ZCS, the on-time remains unchanged. The initial values that the unit start the process with can be programmed in advance, or can be used as default, depending on the length of the start-up tuning procedure that is allowed.

The compensator block is followed by a digital LPF to smooth any noise variations, and it also functions as a possible degree of compensation network in cases where additional lagging or leading phase is required. In this study, filtering is performed by comparing a configurable number of compensator outputs, as shown in Fig. 2b. At the beginning of

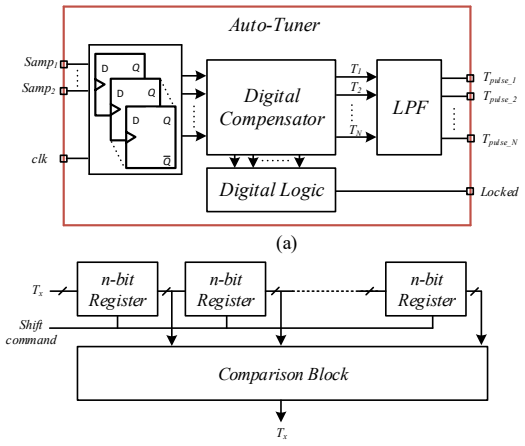


Fig. 2. (a) Internal block-diagram of the auto-tuner module. (b) Simplified block-diagram of the LPF.

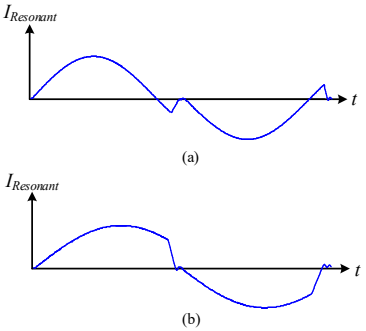


Fig. 3. Current waveform of a resonant circuit switched-off at: (a) Late switching. (b) Early switching.

each switching cycle a shift operation is performed on the register structure and the output of the LPF filter is calculated ($T_{pulse\_x}$ in Fig. 2a). The tune-registers are updated only when all registers hold the same value, which completely eliminates the effect of singular non-ZCS events or inaccurate indications of the ZCD sensors on the converter's operation.

The auto-tuning module allows flexible choice of the resonant tank values which determine the operating frequency of the converter. At power-up a lock-in routine is initiated in which the auto-tuner locates the resonance frequency of each tank. During normal running mode, the module observes the operation of the power-stage and provides fine-tuning to ensure ZCS in case the passive components drift from their values upon start-up.

### C. Sequencer

The *sequencer* module executes the gating signals to the power stage based on the information from the preceding modules. It incorporates a multi-phase high-resolution timer to ensure correct and precise pulse-length for single or multi-stage converter topologies. The gating signals are set independently per resonator (or sub-circuit) of the converter so that ZCS operation can be separately realized per all resonant tanks or stages of a converter, regardless of component mismatches or variations.

The conventional approach to implement a high-resolution timer is by a fast-clock counter-comparator scheme [25]-[27]. In this way, $n$-bit resolution at a switching frequency of $f_s$ requires a reference clock frequency of $2^n f_s$ which translates to increased power consumption. In this study, the high-resolution pulse-width drive signals for the power switches are produced by incorporating a coarse-counting block followed by a fine-tuning delay-line based module, as shown in Fig. 4. This allows a design that is based on standard cells, and enables direct synthesis with low power consumption. As can be seen, a counter-based signal is generated independently for each resonant tank by the information provided from the auto-tuner block. This signal is then delayed by the delay-line to achieve the exact on-time for ZCS operation of all resonant tanks by setting the input of each multiplexer unit according to its *sel* command, which is supplied by the auto-tuner. Protection logic and other gating-related features are also incorporated in this module to allow full completion of a sequence and to avoid overlapping of signals in case the resonant tanks operate with different drive sequences.

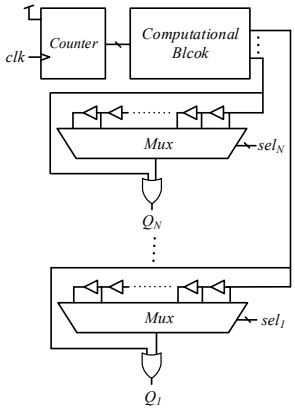


Fig. 4. Simplified block diagram of the sequencer module.

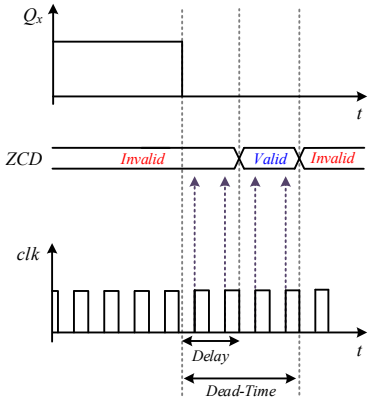


Fig. 5. Continuous-sampling based approach of the ZCD sensors.

### D. Sampling Block

Inherent delay between the generated gating signals in the controller and the actual conduction of the transistors is quite common for all switch-mode applications. This delay, from a controller point of view, is generally unknown and may significantly vary as a function of the operating point or the passive components, driving circuitry and power transistors used [28]-[31]. The information regarding the polarity of the resonant current at transistor turn-off, which is the indicator for early or late switching of the transistors, is only valid in proximity to the switching event. Sampling the ZCD sensors

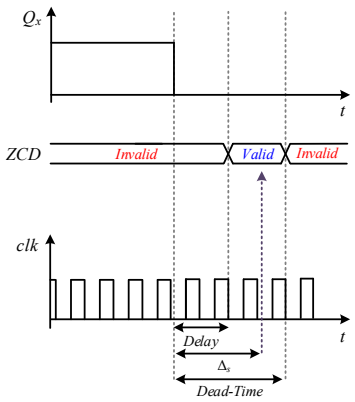


Fig. 6. Single-sample based approach of the ZCD sensors.

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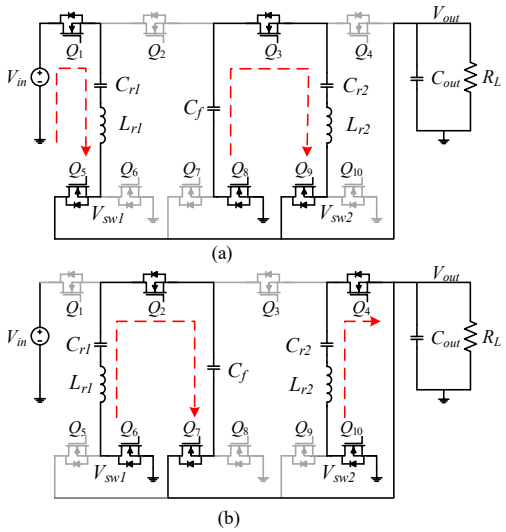



Fig. 7. Equivalent circuits of the 4:1 STC: (a) Charging operation of the resonant tank. (b) Discharging operation of the resonant tanks.

must be able to compensate, or at least consider this inherent delay so that an accurate status information is obtained, i.e. early or late switching.

In this study, two completely synthesizable approaches have been realized to acquire the information from the ZCD sensors while accounting for the above-mentioned delay. The first is based on continuous sampling of the ZCD sensors at the internal clock's frequency from the turn-off command by the controller until the end of the applied dead-time period, as shown in Fig. 5. Here, the ZCD sensor is sampled at the beginning of each clock cycle and the acquired result is processed according to a state-machine algorithm to acquire the converter's switching-state. Once the dead-time period is over, the sampling block provides the auto-tuner with the valid readings for further processing and tuning operations.

The second approach requires less computational efforts during the sampling process, yet still allows sampling with greater proximity to the switching action to further minimize charge losses due to late or early switching of the transistors. This is performed by incorporating a *delay-estimation logic* (detailed in V) which accurately estimates the inherent delay upon start-up, illustrated as $\Delta_s$ in Fig. 6, in addition to a delay-line based structure which generates a sampling signal with a resolution of a single delay-element. Once the ZCD sensors have been sampled, the sampling block provides the auto-tuner with the acquired readings for further processing and tuning operations.

## III. 4:1 STC Control and Simulation Case-Study

As described earlier, the on-time for each resonant tank is modified by the auto-tuner to achieve ZCS operation based on the polarity of the resonant current at turn-off. The operation of the controller is demonstrated for a 4:1 switched-tank-converter (STC) [14] which comprises two resonators, independently tuned to achieve full ZCS operation, as shown in Fig. 7. The operation of the STC can be divided into two states – charging or discharging of the resonators, as shown in Fig. 7a and Fig. 7b, respectively, with a short dead-time period between them. The flying capacitor (intermediate element in Fig. 7) connects to a different resonator at each active sub-circuit, resulting in charge transfer from the input to the output. Soft-charging is achieved for all capacitors in the system, and soft-switching of all switches can be achieved allowing the correct timing which is the task of the controller. For the case of 4:1conversion ratio STC illustrated in Fig. 7, the voltages at $V_{sw1}$ and $V_{sw2}$ are a direct indicator to the current polarity at turn-off. In case of early switching, the resonant current is flowing towards $V_{sw1}$ or $V_{sw2}$ (as shown in Fig. 7a) and the voltages are clamped to $V_{out}+V_F$ (where $V_F$ is the forward voltage of the transistor diode). The same applies to the case of late switching where the current is flowing from $V_{sw1}$ or $V_{sw2}$ (as shown in Fig. 7b), here the voltages will be equal to-$V_F$. Therefore, the ZCD inputs to the controller are obtained from $V_{sw1}$ or $V_{sw2}$.

The ZCD sensor produces a *2-bit* result indicating late-switching (2'*b*00), early-switching (2'*b*11) or ZCS operation (2'*b*01) which is the input to the auto-tuner block, as shown in Fig. 1. The controller observes the status of the ZCD sensors after transistor turn-off and the on-time for each tank is modified accordingly by the compensator.

The verification of the controller operation has been carried out on a 48V-12V STC converter by a set of simulations conducted in PSIM (PowerSim, Inc.); the parameters of the nominal values of the passive components are: $C_{r1}$=2.35$\mu$F, $L_{r1}$=70nH, $C_{r2}$=2.1$\mu$F, $L_{r2}$=63nH, $R_L$=0.26Ω. Results of the lock-in tuning process are shown in Fig. 8a-e, demonstrating convergence onto tuned conditions from off-tune starting points of both resonators, where Fig. 8c, Fig. 8d and Fig. 8e are a zoom-in of the area marked C,D and E in Fig. 8a, respectively. It can be seen that the output voltage increases to approximately 12V, which is the no-load target voltage, indicating that in the context of optimal charge transfer, the controller adequately fulfills its task.

## IV. System-Level and Performance Challenges

### A. Single-Pin Configuration

In complex controller ICs where pin-count is an important asset and it is required to provide access to a large number of operating modes, a single-pin setup is essential. This implies that programming, mode selection, or values setting is carried out according to the voltage level that is imposed on the input pin. The amount of levels that can be utilized in this approach

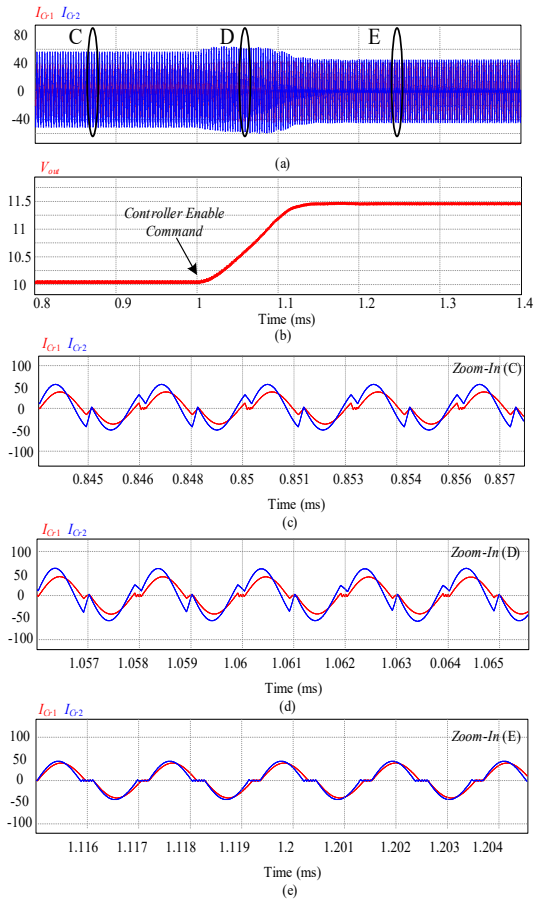



Fig. 8. Closed-loop operation of the controller for a 4:1 STC converter: (a) Resonant currents. (b) Output voltage. (c) Zoom-in on the resonant currents before controller enable command. (d) Zoom-in on the resonant currents during the convergence period. (e) Zoom-in on the resonant currents at steady-state.

depends on the voltage span allowed on the input, resolution and accuracy of the detection unit. The single-pin configuration is facilitated in this study by a Sigma-Delta (SD) modulator and digital logic as shown schematically in Fig. 9.

The SD modulator has been realized with simplified hardware to reduce complexity and the effective area. This may come at the cost of performance or conversion speed, but since the objective of this ADC is to acquire static, or semi-static, voltage levels, the solution fits well within the specifications. As can be seen in Fig. 9, the modulator front-end is realized by a digital inverter, with $V_{op}$ as the high logic level (supply). The integrator is realized by a simple RC network with a corner frequency of at least one order of magnitude lower than the clock frequency. Quantizer is realized by another digital inverter or buffer. The result is then held by a D-flipflop to facilitate a clocked bit-stream and to generate the oversampling frequency of the ADC. The resultant SD-based ADC is a hardware-efficient voltage level translator, the average voltage at node $S_o(t)$ can be expressed as:

$$\overline{S_o(t)} = V_{ref} = V_{op}\frac{CNTR_n}{2^n}, \quad (1)$$

where $V_{ref}$ is the reference value for the modulation process (the threshold voltage of the inverter-based comparator) and $CNTR_n$

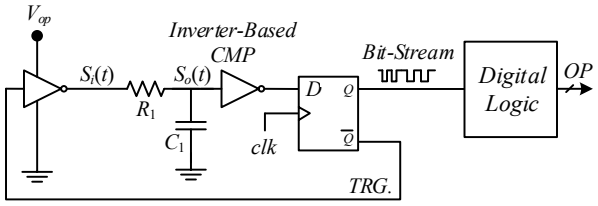



Fig. 9. Simplified architecture of the single-pin configuration hardware.

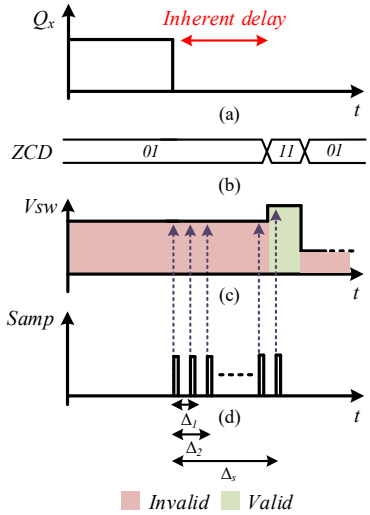



Fig. 10. Waveforms during the inherent delay calculation procedure: (a) Controller gating signal. (b) ZCD sensor. (c) Switching node. (d) Sampling signals.

is the number of logic-high occurrences in the bit stream for $2^n$ clock cycles.

The bit-stream is the input to the computational logic which counts the amount of 'ones' (equals to $CNTR_n$) with a dedicated counter which acts as a sinc LPF, and resets at pre-defined intervals to perform decimation. In this study, the voltage applied on the front-end inverter is translated to a digital representation every 1024 clock cycles, which results in a 10-bit representation of the desired operating mode of the controller.

### B. Inherent Delay Calculation

Estimation of the inherent delay between the gating signals of the controller and the actual turn-off of the power transistors is performed upon start-up and every *Nest* STC switching cycles to account for variations of the passive components (*Nest* is set by the configurable inputs of the controller, OP in Fig. 1). Upon initiation of the delay estimation procedure, a pre-defined switching frequency is applied on both tanks so that early-switching operation is ensured. As a result, the voltage at the switching nodes, $V_{sw1}$ and $V_{sw2}$, is clamped to $V_{out}+V_F$ when the power stage transistors are turned-off, as shown in Fig. 11. To estimate the inherent delay, sampling the ZCD sensor is performed once every switching cycle in different locations ($\Delta_x$ in Fig. 10) until the early-switching reading from the ZCD sensor is acquired (2'*b*11), as shown in Fig. 10b-d. The inherent delay, $\Delta_s$, is estimated to be the minimum delay between the controller gating signals and a sampling command that acquires a valid reading from the sensor.

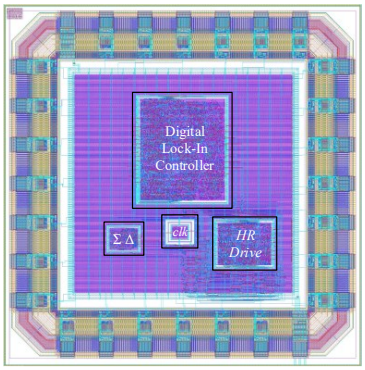



Fig. 11. Layout of the fabricated RSCC controller IC.

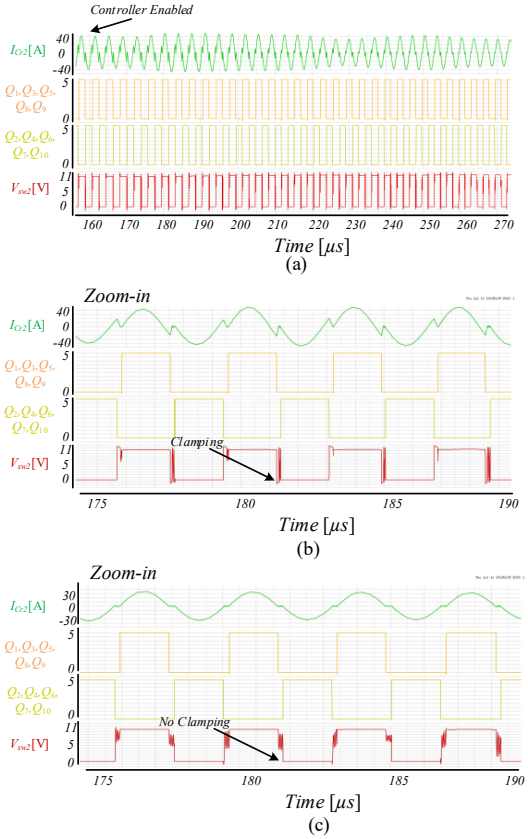



Fig. 12. Post-layout simulations controller IC for a 4:1 STC: (a) Transition from late-switching to ZCS. (b) Zoom-in during open-loop operation. (c) Zoom-in after convergence to ZCS operation.

## V. Experimental Verification

A digital controller IC for RSCC has been designed and fabricated in 0.18$\mu$m 5V process. The IC layout micrograph is depicted in Fig. 11 with overall die area that is pad-limited at 4mm$^2$, while the effective silicon used is 0.64mm$^2$. The operation of the controller IC has been verified with post-layout simulations using Cadence Virtuoso, where the IC connects to a 4:1 STC converter with a 48V input voltage feeding a resistive load of 0.3Ω. The power stage as well as all peripheral circuitry (ZCD sensors, sigma-delta modulator, etc.) have been added to the simulation based on the components used in the experimental setup (discussed next). A transition from late-switching open-loop operation to closed-loop ZCS operation is simulated and verified as shown in Fig. 12. The zoomed-in view of Fig. 12b indicates that in the case of late-switching the voltage at the switching node, $V_{sw2}$, is clamped as discussed in IV and accurately indicates the polarity of the resonant current at turn-off. The zoomed-in view of Fig. 12c shows that once the closed-loop operation is enabled, ZCS is achieved within several cycles.

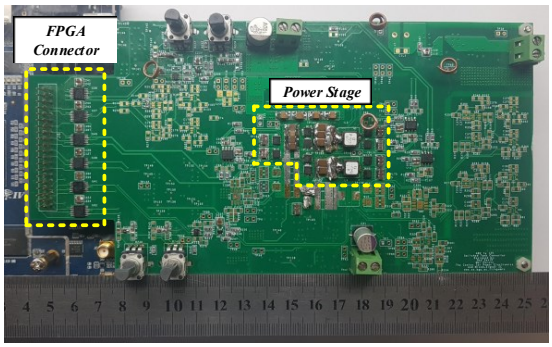



Fig. 13. Experimental prototype of a 4:1 STC for evaluation of the control algorithm on FPGA.

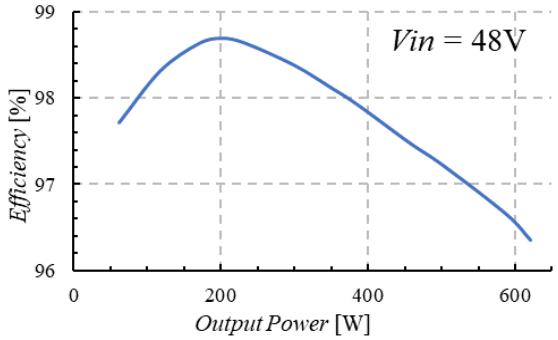
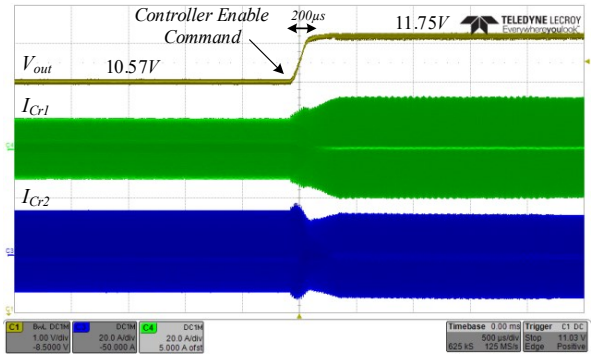


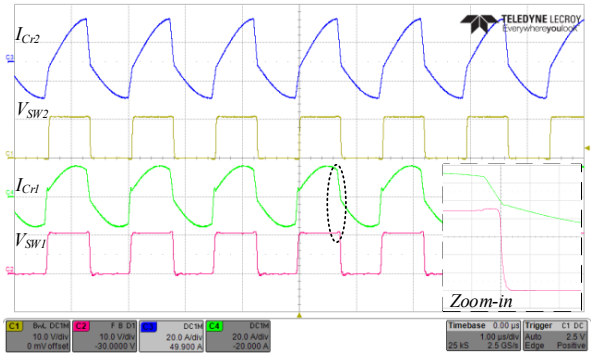

Fig. 14. STC efficiency under tuned conditions.

To validate the core of the controller prior to IC fabrication, and to further investigate the capabilities of the main control units developed in this study in real environment, a full-scale hardware prototype of a 650W 4:1 STC (48V-12V) converter as well as all required peripherals for the controller operation have been designed, built and tested. Shown in Fig. 13 are the full experimental setup, PCB with the power stage and connection to FPGA platform. The control algorithm has been fully coded in Verilog and implemented on a Cyclone IV FPGA using Quartus environment. The experimental STC hardware has been designed on a 14-layer PCB and it is rated for 650W. The effective board area of the 4:1 power stage is 5cmX2cm. The resonators have been designed symmetrically with equal resonant frequency and the following component values: $C_{r1}$=2.35$\mu$F, $L_{r1}$=70nH, $C_{r2}$=2.35$\mu$F, $L_{r2}$=70nH.

Fig. 14 shows the efficiency curve as a function of the load under tuned conditions that have been obtained by the controller operation. Experimental waveforms, depicted in Fig. 15, for closed-loop operation of the system with deliberate mismatch between the resonant tanks component values ($C_{r1}$=2.62$\mu$F, $L_{r1}$=70nH, $C_{r2}$=2.35$\mu$F, $L_{r2}$=50nH). Fig. 15a shows smooth transition from open-loop early-switching operation to ZCS of both resonant tanks. A zoomed-in view of the resonant currents as well as the switching nodes is shown in Fig. 15b-c.




(a)

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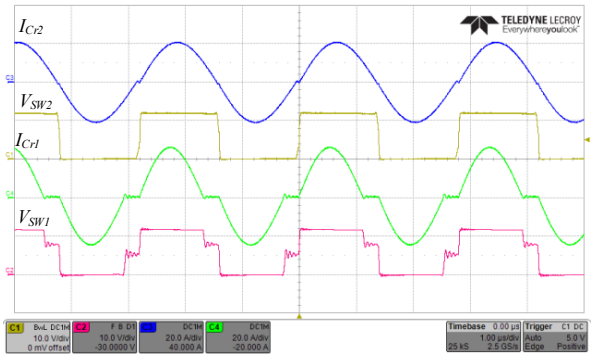


(c)

Fig. 15. Experimental results of a 4:1 STC's transition from open-loop early-switching to ZCS by the digital lock-in controller: (a) Full view of the tanks' currents and the output voltage. (b) Zoom-in view during open-loop operation on the tanks' currents (top-blue, middle-green) 20A/div, switching nodes (middle-yellow, bottom-red) 10V/div, time scale 1$\mu$s/div. (c) Zoom-in view during ZCS closed-loop operation on the tanks' currents (top-blue, middle-green) 20A/div, switching nodes (middle-yellow, bottom-red) 10V/div, time scale 1$\mu$s/div.

## VI. Conclusion

A lock-in integrated controller architecture that facilitates accurate switching timing for single or multi-stage RSCC based topologies has been presented. The controller adjusts to accommodate any mismatch, variations or drifts of component values or circuit configuration, and performs tuning for each resonator independently to fully utilize the charge transfer for each flying capacitor in the system. A full-scale hardware prototype of 650W 4:1 switched-tank-converter has been used to validate the controller's operation prior to IC fabrication, demonstrating excellent lock-in capabilities and high efficiency of up to 98.6%. The fully-digital controller IC has been designed and fabricated on a 0.18$\mu$m 5V process by pure digital means, resulting in effective silicon area of 0.64mm$^2$. The post-layout results of the closed-loop operation demonstrated accurate tuning for two resonators with individual independent resonant characteristics.

## Acknowledgment

This research was supported by THE ISRAEL SCIENCE FOUNDATION grant number 2186/19.
This research was supported by Vishay Ltd., Siliconix IC division.

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