

Adaptive Self-Tuned Mixed-Signal Controller IC for Resonant Wireless Power Transfer

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Abstract — This paper introduces an adaptive self-tuned controller IC for resonant wireless power transfer (RWPT) systems. The new controller IC comprises an on-the-fly very-high-frequency tracking hardware with high-resolution and an independent high-resolution digital PWM-based (HR-DPWM) current programmed control. These facilitate precise frequency generation as well as adaptive tuning of the reactive components in the matching network, which translate into tight current/power regulation capabilities while retaining optimized power transfer conditions. This enables to effectively disengage the power delivery capabilities from the variations of the resonators, electrical circuits and wireless medium. A fully synthesizable digital two-loop controller has been realized through HDL tools, and several new IP blocks have been developed and described in-detail: a delay-line (DL) based phase detector, high-resolution digital controlled oscillator (DCO), HR-DPWM. To fully exploit the benefits of digital electronics, reduce power consumption and save area, the digital core of the controller has been designed through asynchronous architecture, eliminating the need of high-speed clock and its related architecture. The mixed-signal controller IC has been designed and implemented in 0.18 μm , resulting in total effective silicon area of 1.44 mm^2 . Post-layout results of the fabricated IC operating in closed-loop are provided, demonstrating the performance and benefits of the new controller for meeting the requirements of resonant-based WPT systems. In addition, to validate and verify the controller core prior to IC fabrication, the control algorithm has been implemented on FPGA. To demonstrate closed-loop operation of a wireless power system, an experimental LC resonant capacitive-based WPT system has been constructed. The effectiveness of the controller is well demonstrated and evaluated at the MHz range up to an air-gap of 200 mm, validating adaptive self-tuned system.

Keywords — adaptive controller IC, closed-loop wireless system, impedance matching, resonant power transfer, self-tuned system, variable inductance.

I. INTRODUCTION

Over that last decade, there has been an increasing interest in the rapidly growing field of wireless power transfer (WPT) technology, which developing into a standard feature in many daily-used applications [1]-[7]. WPT technology is the main enabler to cut the last cord, and to reduce the significant dependency of volume-sensitive portable applications on embedded bulky batteries as a reliable main source of energy [1]-[3]. Inductive power transfer (IPT) is a well-known near-field WPT method, and it is the most adopted technique in commercial WPT applications due to its simplicity, reliability and safety [1], [3]-[5]. Another near-field method is capacitive

power transfer (CPT), that is potentially with better efficiency characteristics, lower volume and construction complexity [6]-[8]. To achieve better power transfer characteristics, resonant high-frequency operation, typically in the range of several MHz, is utilized in WPT systems [9]-[16]. This is essential to compensate for the relatively low coupling of the wireless medium, enhance the transmission range, and achieve reasonable efficiency. In addition to improved spatial freedom, resonant wireless power transfer (RWPT) systems can to provide energy to multiple devices with different power requirements simultaneously [11], [16].

Several methods to achieve resonant frequency control for RWPT have been reported in the literature [17]-[29]; Tunable impedance matching techniques have been widely adopted in RWPT to adjust the resonant characteristics to a target fixed frequency [17]-[21]. To obtain fine tuning of the matching networks, in particular at high frequencies, considerable amount of passive components and bi-directional switches is required, thus, the overall system is quite complex and bulky [18]-[20]. Automated frequency tracking method has been also utilized in RWPT [21]-[29]. Several works employed frequency tuning by maximum power point tracking [21]-[24], there, the controller seeks for the peak power which obtained at resonance, and tunes the operating frequency accordingly. The latter provides flexibility in power regulation, but comes at the cost of potential slow dynamics of the system and potential degradation of the overall efficiency. Another technique for automated frequency tuning has been utilized based on phase angle detection [25]-[29]. Although reasonable dynamics can be obtained, this approach introduces a major tradeoff between

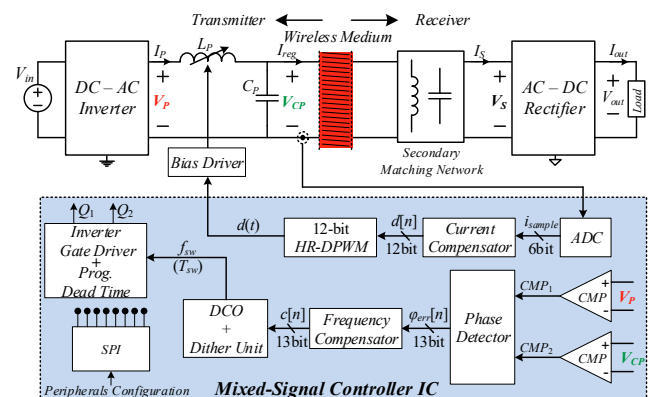


Fig. 1. Simplified schematic diagram of a double-sided LC capacitive WPT system with an adaptive multi-loop controller.

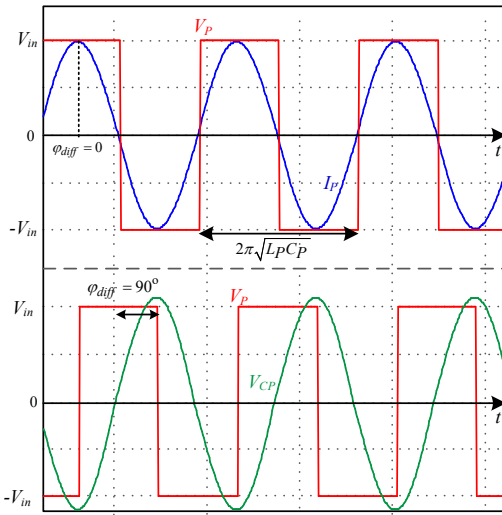


Fig. 2. Typical waveforms of the primary side at resonance in a L-type WPT configuration operating at resonance.

frequency resolution and operation range. This can be improved by using custom designed analog-oriented architectures IC, however, the design efforts, die area and overall power consumption will significantly increase. On the other hand, digital-oriented architectures can be found very attractive in terms of design efforts and integration [30], [31]. The main limiting factor of digital-based frequency synthesizers is that commonly used FPGAs, microcontrollers and other digital platforms provide time-resolution on the order of several hundreds of pico-seconds [31]-[33]. Therefore, to obtain wide range high-frequency operation while maintaining a high-resolution, without significant penalty on power consumption and silicon area, *dedicated ASIC with specifically tailored hardware that can be realized through a simple design flow is required* - this has been pursued in this study.

The objective of this study is therefore to introduce an adaptive high-frequency high-resolution self-tuned controller IC for resonant-based WPT systems as detailed in Fig. 1. The new controller IC relies on continuous tuning of the operating frequency to the resonant one, regardless of system variations and components drifts. It is a further objective of this study to present a tuned network realization that enables a power regulation on the transmitter by controlling a continuous self-tuned variable inductor that is not based on relays or semiconductor switches. The mixed-signal IC architecture is based on two independent control loops that include the following key building blocks: wide-range high-resolution phase detector, high-resolution digital controlled oscillator (DCO), programmable dead-time unit, digital PWM for basing the variable inductor, custom designed sigma-delta ADC and a serial communication interface (SPI).

The rest of the paper is organized as follows: Following a brief survey of L-type resonator, Section II describes the principle of operation of the mixed-signal controller IC and details its algorithm. Section III details the architectures for the main units of the mixed-signal controller IC. System level considerations with emphasis on limit-cycles oscillations and frequency resolution are delineated in Section IV. Experimental and post-layout verification of the controller IC are provided in Section V. Section VI concludes the paper.

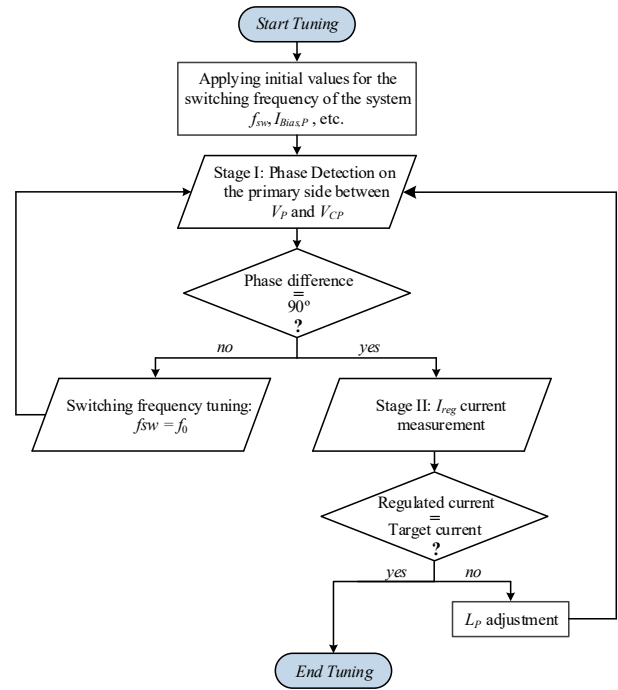


Fig. 3. Flowchart of the resonant WPT controller IC tuning procedure.

II. CONTROL FOR RESONANT WPT SYSTEMS

A. Review of L-type based WPT System

The principle of operation of the adaptive resonant WPT controller IC is described here through a L-type series-parallel (LC) matching network [7], [34] as delineated in Fig. 1. It should be emphasized, however, that the core of the control algorithm is applicable for any near-field resonant-based WPT approach. Assuming loosely-coupled operation [7], [9], [35], the drive frequency, f_{sw} , is near the matching networks' resonant frequency (i.e., $f_0 = 1/(2\pi\sqrt{L_P C_P})$), then the currents as well as voltages of the passive components are virtually sinusoidal [36]. This is since high-Q operation is naturally facilitated as the output impedance of the LC matching network in the primary side is relatively high. Typical waveforms of the primary side in this WPT system are shown in Fig. 2. Assuming that a full-bridge inverter is used at the front-end, the primary voltage, V_P , toggles between V_{in} to $-V_{in}$, and the sinusoidal primary current, I_P , is in phase with V_P . It can be also seen, that in resonance the phase difference between V_P and the voltage across the matching capacitor, V_{CP} , is exactly 90° .

B. Controller Operation

The new mixed-signal controller IC that has been realized in this study, is described with the aid of a high-level flowchart of the tuning procedure (Fig. 3). Since the controller IC should function as a stand-alone module, the hardware architecture includes a small volatile memory, as a part of the serial communication interface (custom designed SPI) that is preprogrammed with a set of default values for the main parameters of the controller. On startup, the default values can be used or a new set can be loaded to the controller through the SPI. Then, the SPI internally communicates with the main units and loads the set of values per block. A benefit of this embedded

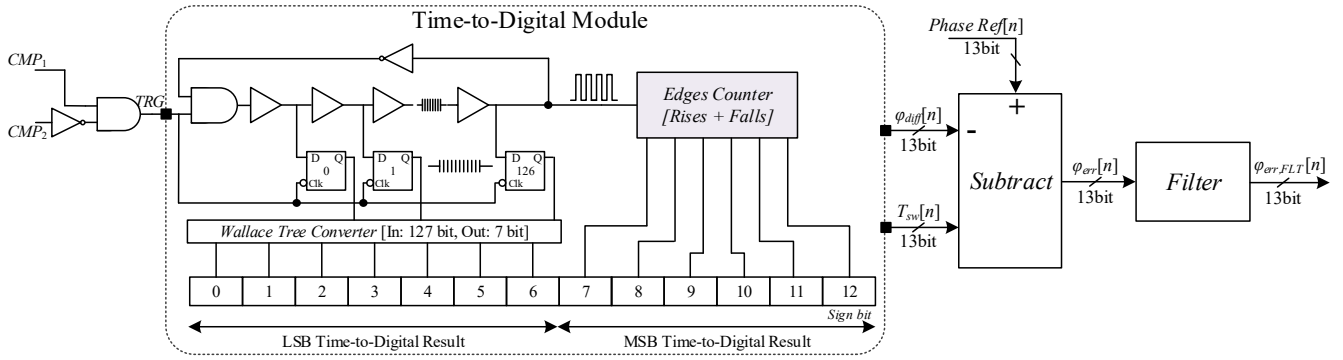


Fig. 4. Simplified schematic diagram of the high-resolution wide-range phase detector.

feature is that the same controller hardware can be used with different power-stages, matching network configurations and parameters.

Upon initiation of the tuning procedure (Fig. 3), a default set of pre-loaded values are used to determine the switching frequency, f_{sw} , variable inductor, compensators parameters, etc. The inner feedback which is the fastest loop applies frequency tuning. There, the switching frequency, f_{sw} , to drive the DC-AC inverter (full-bridge in this study) is being varied by the DPLL unit to match the resonant frequency of the circuit f_0 . This is facilitated by measuring the voltages V_P and V_{CP} (Fig. 1), extracting the phase difference between them, and adjusting f_{sw} until the phase difference between the signals reaches 90° . In the case that the detected phase difference between the signals is not 90° , an error signal is generated to the DCO, which in turn synthesizes new switching frequency until $f_{sw} = f_0$. In the next stage of the tuning operation, the current flowing to the coupler, I_{reg} , from the primary circuit (Fig. 1) is sensed and compared to a target/reference one, which is pre-defined by the SPI unit. The correction signal that is generated is used to vary the inductance L_P through a bias winding until the required current is achieved. This variation of the inductor value is realized by a buck converter current driver that applies dc bias to non-gapped side windings of the inductor as previously described in [37]-[39]. Due to the variation of the inductance value, the resonant characteristics of the system change, and potentially move the system out of its optimized transfer conditions. As a result, the frequency tracking loop needs to search again and lock the switching frequency into the resonant frequency.

III. ADAPTIVE RESONANT WPT CONTROLLER IC ARCHITECTURE

The realization of the adaptive mixed-signal controller IC, relies on three key enabling blocks: 1) a high-resolution wide-range phase detector. 2) a 13-bit Enhanced dither-based high-resolution digital controlled oscillator. 3) a 12-bit high-resolution digital PWM (HR-DPWM) that generates gate drive signals for the bias current driver of the variable inductor. Each of the fundamental units has been implemented as an asynchronous hardware, using delay-lines (DL) [40] and combinatorial circuits. By doing so, a significant portion of complex and power-hungry hardware for timing and high-speed synchronization is eliminated. Since some of the units are still based on a synchronized process, a system governor is employed to provide time-base to the switching cycle and

trigger the sequential operation of the functional blocks within the switching cycle.

A. Phase Detector

Accurate wide-range phase detection is one of the key factors to achieve high-performance frequency control in resonant WPT systems. Thus, conventional methods for phase detection which consists of type-I detection circuit, i.e., comparators as digitizers and an exclusive-or (XOR) phase comparator [41], are not sufficient since they have narrow dynamic range of operation, additionally, there is no direct information whether the phase difference is positive or negative.

The phase detector in this study is based on a time-to-digital conversion (TDC) using a DL string built of digital buffers with fixed propagation time [31], [40], as shown in Fig. 4. The phase difference is translated by the time difference between the signals CMP_1 and CMP_2 (which are the digitized representations of V_P and V_{CP}), and obtained by combination of few basic operators (Fig. 4). The signal, TRG , triggers the DL string and starts the conversion process, such that seven LSBs of the output registers are a direct Wallace-Tree translation [31] of the DL. A counter, triggered both at rising and falling edges, is connected to the end of the string to count the repetitions of full DL string propagations, the result is conjugated as the six MSBs of the output register. Once TRG returns to low logic level, the counter holds the number of cycles that the DL propagates throughout the pulse width of TRG , while the DL holds the residual time difference with higher time resolution, due to the partial propagation of the last run. A 13-bit result of the phase difference, $\phi_{diff}[n]$, is generated together with $T_{sw}[n]$ which represents the switching period (time representation of 360° phase range) with respect to the operating frequency of the system. This is essential, since the phase difference and the phase reference must be normalized to the time base due to the operating frequency. The phase error, $\phi_{err}[n]$, is obtained by subtraction between the phase reference and $\phi_{diff}[n]$, where the MSB of $\phi_{err}[n]$ is the sign bit. Finally, to obtain noise-clean phase error signal as much as possible, $\phi_{err}[n]$ is filtered.

It should be further noted that, since the voltages of the resonator can be significantly higher than the operation voltage levels of the controller and other electronics periphery, the voltages V_P and V_{CP} are scaled down using high-impedance attenuation circuit to voltage levels suitable for logic gates input such as the phase detector unit. From practical implementation perspective, if a simple resistive divider is used, the input

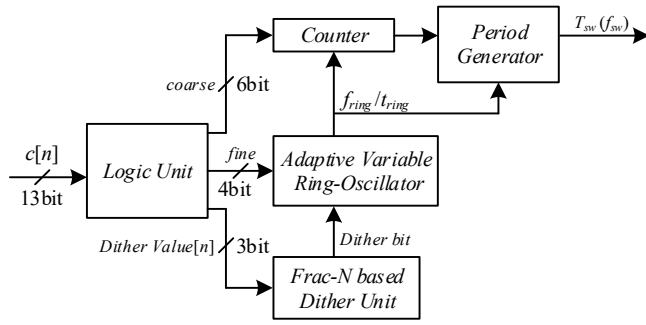


Fig. 5. Block diagram of the digital controlled oscillator.

capacitance of the logic gate introduces phase delay between the actual zero-crossing point and the digital signal transition. In the case that the phase shifts of the two measured signals are different (due to different resistive path), a systematical offset exist, and should be calibrated out. This has been solved by setting the phase reference slightly higher (or lower) than the target one, compensating for undesired offsets due to the voltages sensing paths.

B. High-Resolution Digital Controlled Oscillator

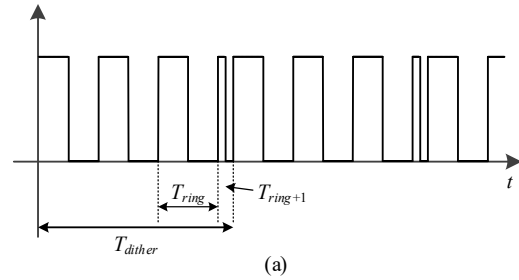
The core of the DCO in this work is based on a clocked counter-comparator scheme [42], and is able to generate frequencies between approximately 1-to-10 MHz. Where the general frequency relationships of the DCO are expressed as follows

$$f_{ring} = \frac{1}{Nt_{DE}} \Rightarrow f_{sw} = \frac{f_{ring}}{CNT_{per}} = \frac{1}{CNT_{per}t_{ring}}, \quad (1)$$

where f_{ring} is the frequency of the ring-oscillator, t_{DE} is the delay of a single delay element within the ring-oscillator, N is number of elements in the string, and CNT_{per} is an integer represents the value of the counter for generating the target frequency (period). It should be noted that, due to possible process, voltage, and temperature (PVT) variations, and other potential post-fabrication mismatches, t_{ring} can be manually calibrated by adding/removing delay elements within the ring-oscillator (by the SPI). From (1), it can be observed that f_{sw} can be varied by adjusting t_{ring} and CNT_{per} , therefore, an adaptive ring-oscillator has been realized. In order to achieve high-resolution frequency tuning, without the penalty of increased power consumption, the DCO in this study, has been realized based on a combined coarse-fine tuning concept [31].

The correction signal from the frequency compensator, $c[n]$, is passed through a logic unit which distributes $c[n]$ to the main units of the module (Fig. 5) after employing some mathematical manipulations. The coarse-tuning of the output frequency, f_{sw} , is generated by 6-bit counter which divides the frequency band into 64 time slots of t_{ring} , where change of a single bit results in a different time slot. Next, fine-tuning is employed by varying t_{ring} in real-time by adjusting the number of the delay elements, N , within the adaptive ring-oscillator, which enables a single cell resolution.

The frequency resolution of the DCO, f_{res} , can be calculated as the LSB change in CNT_{per}



(a)

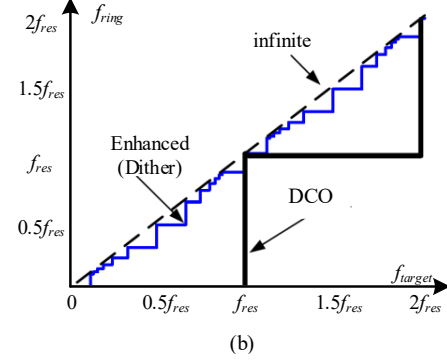


Fig. 6. (a) Dithered output signal with frequency fraction of $0.25f_{res}$; (b) Output frequency versus desired frequency for typical DCO and 3-bit resolution enhancement.

$$f_{res} = \Delta f_{sw} = \frac{1}{CNT_{per}t_{ring}} - \frac{1}{(CNT_{per} + 1)t_{ring}} \approx \frac{1}{CNT_{per}^2 t_{ring}} = t_{ring} f_{sw}^2 \quad (2)$$

From (2), it can be well observed that the frequency steps of the DCO are limited by the module's base frequency, and increase as the square of the operating frequency, i.e., at lower operating frequency, the frequency resolution would be finer than what can be achieved at a higher frequency. Since finer resolution is desired for the entire operating range, an effective, fast dynamics and low distortion, frequency enhancement dithering procedure has been employed [43]. Adaptive Frac-N dithering method is facilitated by dithering the DCO between CNT_{per} and $CNT_{per}+1$ at a defined rate, varied by the required accuracy. The dither factor, n , is the number of DCO cycles needed to achieve the desired fractional frequency. Dithering is accomplished by keeping a constant period over $(n-1)$ DCO cycles (referred as base period) and then changing the last slot (n) to another period. For example, (Fig. 6a), for a frequency fraction of $0.25f_{res}$, the DCO will generate one $(CNT_{per}+1)$ period every 4th cycle. The resultant (average) frequency in this method can be calculated by a general expression as follows

$$f_{sw_dither} = \frac{1}{\left[(n-1)CNT_{per} + (CNT_{per} + 1) \right] / nt_{DE}} = \frac{1}{\left(CNT_{per} + \frac{1}{n} \right) t_{DE}} ; n=1,2,3... \quad (3)$$

and the enhanced frequency resolution

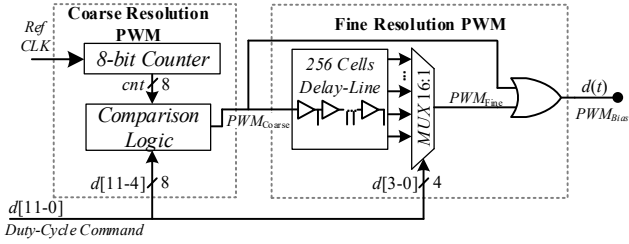


Fig. 7. Simplified architecture of the 12-bit HR DPWM.

$$f_{res_dither} = \frac{1}{\left(CNT_{per} + \frac{1}{n+1}\right)t_{DE}} - \frac{1}{\left(CNT_{per} + \frac{1}{n}\right)t_{DE}} \approx \frac{1}{n(n+1)CNT_{per}^2 t_{DE}} = \frac{t_{DE} f_{sw}^2}{n(n+1)} \quad (4)$$

Fig. 6b shows a comparison between ideal infinite frequency states, Frac-N dithering method for a 3-bit frequency resolution enhancement (i.e., eight additional frequency fractions between two base DCO values) and a typical DCO operation.

C. High-Resolution Digital Pulse Width Modulator

To accurately control the variable inductor and to avoid undesired oscillations, a high-resolution modulator is required. The conventional approach to implement HR-DPWM is by a fast-clocked counter-comparator scheme [42]. In this way, n -bit resolution at a switching frequency of f_{bias} requires a reference clock frequency of $2^n f_{bias}$. This translates to increased power consumption and more complex design to realize the high-speed circuitry. Another approach to realize a HR-DPWM is based on tapped DL scheme [40]. In this method, the power consumption is reduced, but the required silicon area of the design grows exponentially with the number of resolution bits.

The HR-DPWM in this study, has been realized similarly to a combined coarse-fine digital counter concept [31], Fig. 7 shows the conceptual architecture of the unit. As can be seen, it comprises two main functional units: counter-based coarse resolution PWM generator and fine-tuning delay chain combined with an OR operator. The 12-bit digital word for the duty-cycle command $d[11-0]$ is distributed within the units. The coarse Resolution PWM block is fed by a reference clock (generated by the system governor) which is being counted and compared with 8 upper bits of the duty-cycle command $d[11-4]$, the resulted signal PWM_{Coarse} can be expressed by

$$PWM_{Coarse} = \begin{cases} d[11-4] > cnt[7-0], & '1' \\ d[11-4] < cnt[7-0], & '0' \end{cases} \quad (5)$$

The fine resolution PWM unit generates a string of 4-bit long DL that finely adjusts PWM_{Coarse} by the number of delay elements as specified by $d[3-0]$. The latter combined with the OR operator generate the high-resolution PWM output signal, $d(t)$.

IV. LIMIT-CYCLE OSCILLATIONS IN DIGITALLY CONTROLLED RESONANT WPT

A major practical issue that should be considered when designing closed-loop resonant based WPT systems, and particularly digitally controlled RWPT are limit-cycle oscillations (LCO). As originally presented in [43], the primary cause for steady-state oscillations is resolution mismatch of the

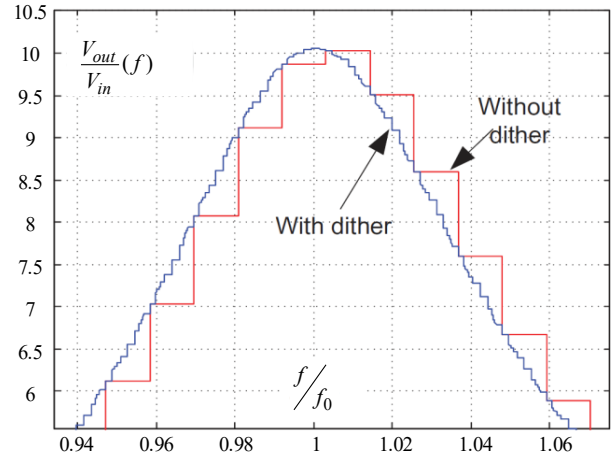


Fig. 8. Simulated frequency response (sweep) of L-type resonant network, comparison between typical DCO frequency steps and 3-bit resolution dithered-based DCO.

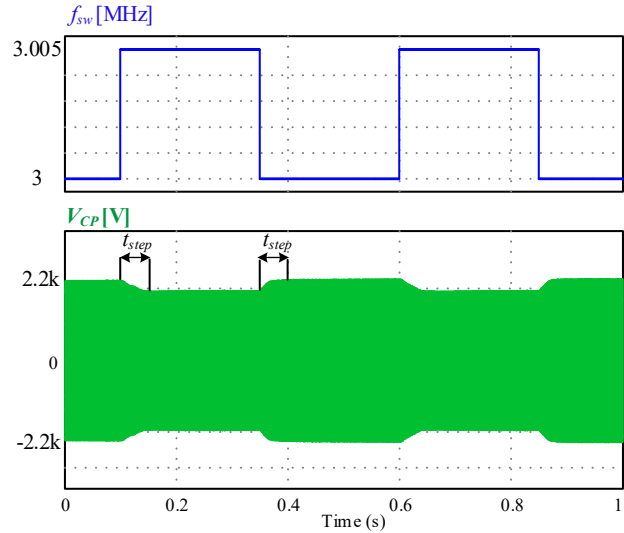
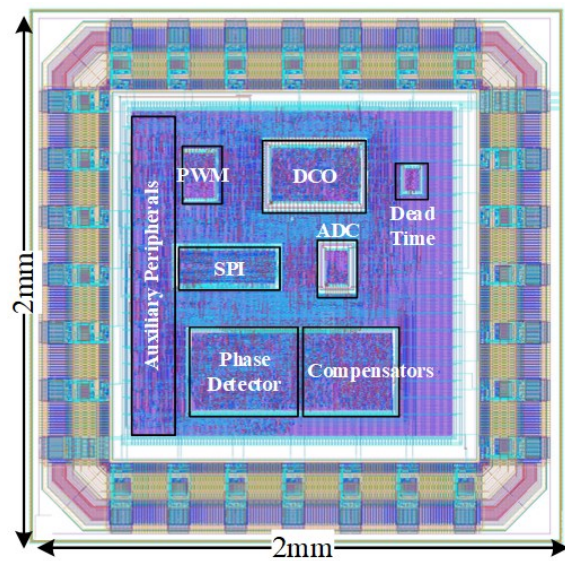
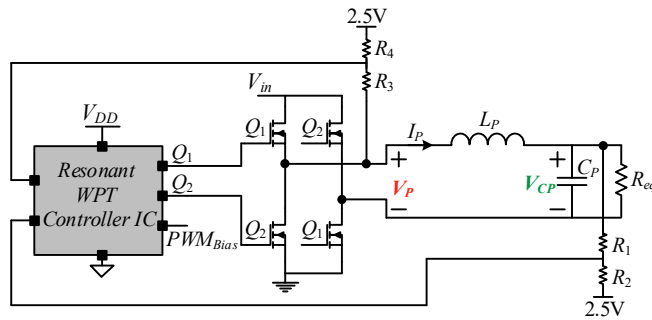


Fig. 9. Simulation results showing the convergence of the sinusoidal voltage V_{CP} to frequency steps of 5 kHz.

DCO (assuming the compensators does not add quantization error). In addition to the operating-point-dependent gain that exist in resonant converters, the highest sensitivity to gain variations is located around the resonant frequency, a condition that becomes even further emphasized in resonant-operating WPT systems that operate with very high-quality factors. Since the controller targets optimal transfer conditions which are obtained at resonance (aside from slight deviation from the exact target frequency to facilitate ZVS), this calls for extremely sensitive calibration, i.e., fine frequency resolution generator at MHz range to facilitate LCO-free operation. Therefore, to ensure smooth high-frequency drive throughout the operation range (taking into account the worst-case conditions of the highest quality factor), the DCO in this study have been designed to achieve the required effective acquisition as well as control resolution such that limit-cycle oscillations are remedied. As discussed in Section III, frequency dithering has been embedded to enhance the drive frequency, and to provide effective frequency (over few cycles) with finer resolution than the base value. The effect of frequency resolution in resonant converter drives is depicted in Fig. 8,



(a)



(b)

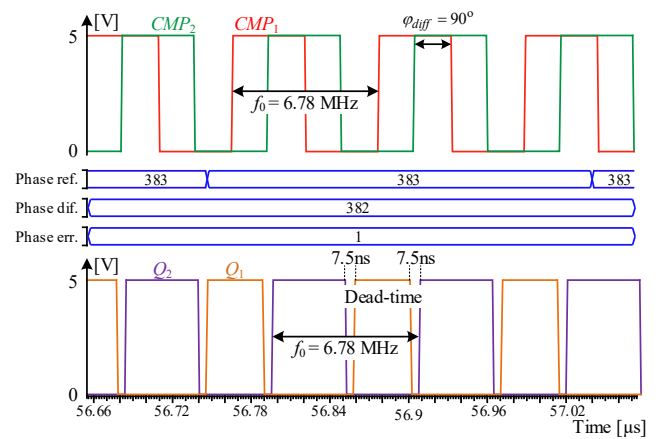
Fig. 10. (a) Layout of the fabricated resonant WPT controller IC; (b) Post-Layout simulation test-bench.

which is the simulated output response of a series-parallel resonator (L-type) driven by a typical 8-bit DCO and by the presented dithered-DCO with 3-bit resolution enhancement. In addition, the slow-response feature of the resonant network due to high-Q also aids with LCO in the context of resonant WPT systems, since it takes the resonator several cycles to react to changes in the drive frequency, it is utilized as an averaging action. To demonstrate this characteristic, a cycle-by-cycle simulation at a resonant frequency of 3 MHz with steps of 5 kHz has been utilized as illustrated in Fig. 9. There, the convergence time, t_{step} , to ± 5 kHz step was approximately hundred switching cycles.

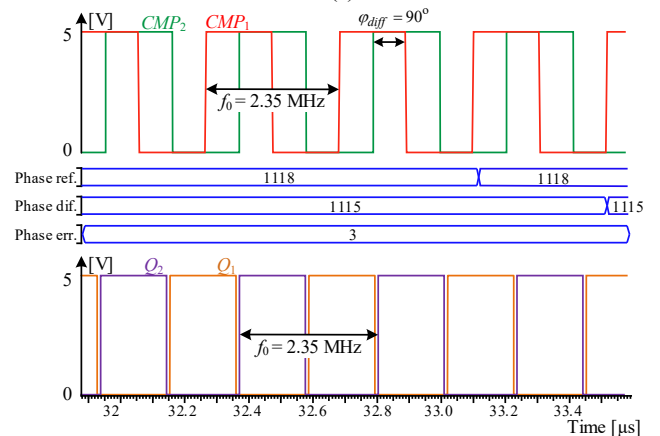
V. POST-LAYOUT AND EXPERIMENTAL VERIFICATION

A resonant WPT mixed-signal controller IC has been designed and implemented in 0.18- μm , the overall die area is 4 mm^2 (pad limited), with effective silicon areas of 1.44 mm^2 , the chip layout is shown in Fig. 10a. The operation of the controller IC has been verified with post-layout results using Cadence Virtuoso, where the IC connects to an external L-type resonator; $L_p=11 \mu\text{H}$ and $C_p=50 \text{ pF}$, with full-bridge inverter at the front-end (Fig. 10b).

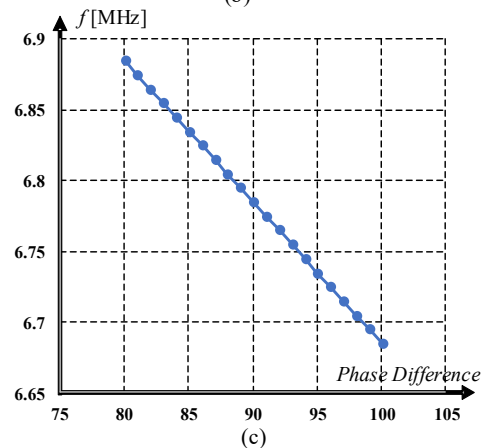
Using high-impedance resistive divider, the voltages V_p and V_{CP} are scaled down to voltage levels suitable for the chip operation. Fig. 11a depicts results for resonant operation at



(a)



(b)



(c)

Fig. 11. Post-layout results of the controller IC: (a) tuned operation at 6.78 MHz, (b) tuned operation at 2.35 MHz, (c) frequency resolution at the vicinity of resonant operation at 6.78 MHz.

ISM-band frequency 6.78 MHz for, as can be seen the target phase reference (90°) is translated to decimal representation of '383', phase difference is '382', thus, the error equals to '1' (with respect to 13-bit). The dead-time between the generated gate drive signals is ~ 7.5 ns. Fig. 11b demonstrates resonant operation at 2.35 MHz, it can be noticed that although phase difference of 90° is obtained, the values are translated to different decimal representations, since the values are normalized with respect to the switching period, as discussed in Section III-B. In addition, post-layout analysis shows that at

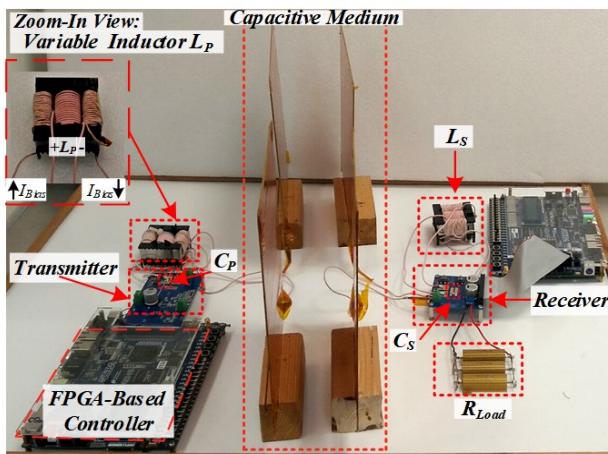


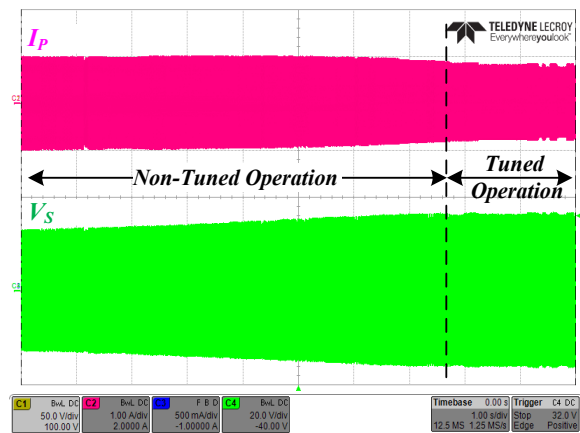
Fig. 12. Experimental prototype of a double-sided L-type capacitive WPT system for evaluation of the control algorithm on FPGA.

6.78 MHz in the vicinity of resonance, the effective frequency resolution is approximately ± 1.25 kHz, which satisfies the allocated frequency bandwidth according to alliance for wireless power consortium [39].

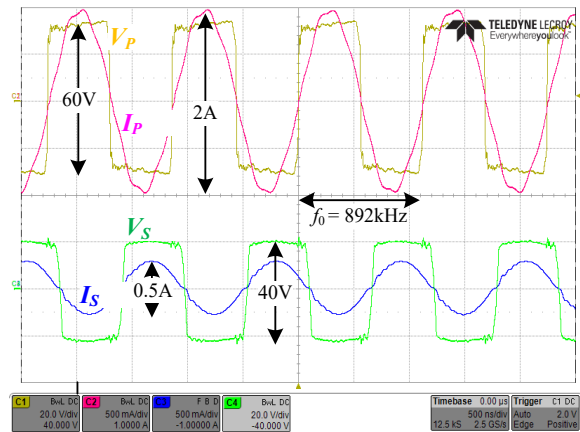
To verify the core of the controller prior to IC fabrication, the control algorithm has been fully coded in Verilog and implemented on FPGA with lowered operation frequency, and validated on an experimental double-sided L-type resonant operating capacitive WTP prototype with variable inductors as depicted in Fig. 12. The coupling plates have been designed symmetrically (30x30cm), and the L-type networks nominal parameters are: $L_p = L_s \approx 75$ μ H and $C_p = C_s = 250$ pF, $f_0 \approx 1.2$ MHz. The full-bridge inverter has been realized with high-frequency GaN power modules. Fig. 13a shows the behavior of the system during tuning for an input voltage $V_{in} = 30$ V and 100 Ω load for an air-gap of ~ 200 mm (with primary's current I_p and secondary's voltage V_s). Figs 13b and 13c show a zoomed-in views of the tuning process with the waveforms of the switching nodes voltages and resonant currents upon initialization (Fig. 13b) and the end (Fig. 13c) of the tuning process. It can be seen that the switching frequency increases from 892 kHz to 1.2 MHz, which is the resonant frequency of the system. The output parameters (I_s and V_s) also increase, delivering more energy to the load by more than 2.5 times, while the transfer efficiency has improved over four times.

VI. CONCLUSIONS

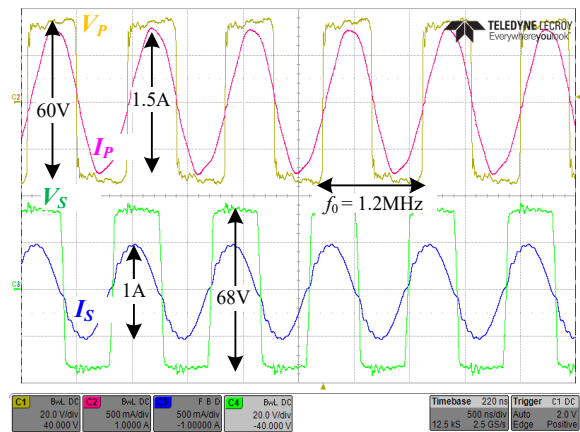
An adaptive self-tuned high-performance controller IC for resonant-based WPT systems has been detailed, analyzed and experimentally validated. The IC comprises of two main independent control loops, which effectively disengage the power transfer capabilities of RWPT from components variations any other potential drifts, and further enables spatial freedom. The control algorithm, signal flow and the functional relationships of the multi mixed-signal controller have been addressed, and all the intricate transfer functions of the key building blocks have been derived. The controller has been designed and fabricated in 0.18- μ m process, where the digital core has been realized by an automated synthesis process and place-and route tools, resulting in total effective silicone chip area of 1.44 mm². In the IC design, several main enabling key building blocks have been developed: DL-based phase detector,



(a)



(b)



(c)

Fig. 13. Experimental results of the tuning process: (a) Full view of the envelopes of I_p and V_s , (b) Zoom-in view on the initial stage, (c) Zoom-in view on the final stage. Voltage scale 20V/div; Current scale 500mA/div; Time scale 500ns/div.

high-resolution DCO, and DPWM. Post-layout analysis of the controller IC combined with L-type resonator, demonstrates high-performance self-tuned system. To further validate the controller core, an experiential resonant LC CPT prototype in the MHz range has been constructed, with the core of controller implemented on FPGA platform. The resultant dynamic performance of the closed-loop CPT system is well validated through experiments up to air-gap of 200 mm. The new mixed-signal controller IC concept may be found very beneficial in many resonant-based wireless technologies.

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