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Advanced Control Features of Hybrid Current-Programmed Digital Controller in Multiphase VRM Applications

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***Abstract*— This paper introduces advanced digital control features intended for high-end multiphase VRM controllers. These features are incorporated in state-of-the-art digital hybrid Average Current Mode (ACM) control architecture to facilitate a through and comprehensive solution required in voltage regulation of high-performance loads. Particularly, two main architectures are detailed. A phase shedding (and adding) scheme to determine the optimal phase-count according to the per-phase maximum efficiency region and the current provided to the load, and an Active Voltage Positioning (AVP) modifies the output voltage to limit instantaneous heat dissipation of the load according to a programmable piecewise linear load-line profile. In addition, the voltage regulation scheme is based on a control scheme that hybrids two control laws: a linear ACM and non-linear acceleration for optimized transient response. The hand-off procedure, presented in this study, achieves seamless transitioning between controller operations, reducing post-transient output voltage deviations and current spikes. The mixed-signal platform (digital controller, analog interfaces, acquisition periphery) have been tested and successfully validated experimentally on Intel-certified hardware and test protocols. The experimental prototype features a 4-phase 12V to 1.xV multiphase buck VRM that drives an array of 7 DDR4 load modules, accommodating 100A load transients with transition rate of 2000A/us, demonstrating minimum-deviation load recovery as well as ace steady-state target tracking.**

Keywords – Digital control, hybrid control, multiphase, buck, VRM, DDR.

I. INTRODUCTION

The growth of datacenters and computing power have expanded significantly over the last decade with the emerging data-intensive technologies such as artificial intelligence, autonomous vehicles and cloud computing [1]-[3]. The power processing architecture of datacenters applications typically applies a 48V unregulated bus as the main source, which is then stepped-down to the load voltage level in a two-stage conversion [4]. The first stage facilitates a 12V voltage rail, in either regulated or nonregulated configuration; the second stage is a 12V-to-1.xV voltage regulator module (VRM) back-end converter, tightly regulates the voltage of the high-performance load with high steady-state efficiency, voltage accuracy and tight regulation under wide and rapid load changes. Multiphase buck converter VRM (MPVRM) is the configuration of choice for datacenters and in the majority of high-performance load applications [5]-[6]. Cutting-edge MPVRMs obtain higher effective bandwidth, reduced output current ripple and components' stress [7]-[8]. This is achieved by paralleling multiple converters to supply the load, operating in synchronized operation either in-phase (for transient acceleration) or interleaved (to reduce ripple and enhance the steady-state efficiency) [9]-[10].

Digital control of MPVRM has emerged as the favorable approach for power management in high-end applications [11], offering design flexibility and combining tight voltage regulation along with advanced programmable features tailored to the power-stage and load requirements. The utilization of digital implementation has been augmented with the introduction of multi-mode, boundary and hybrid controllers since incorporation of multitude of configurable options and the transitioning between modes is quite straightforward, as opposed to analog realization. In the vast

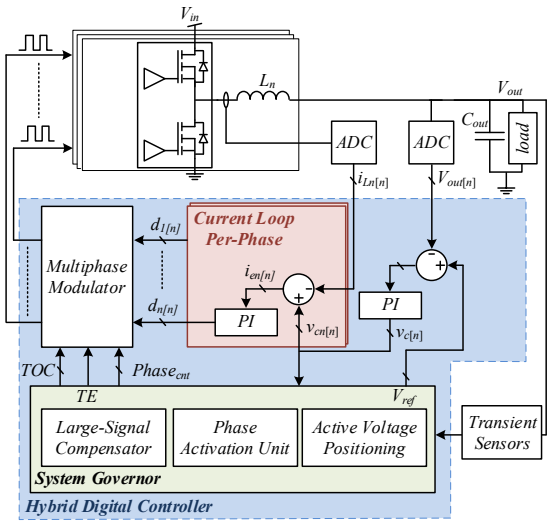

Fig. 1. Simplified block diagram of the multiphase buck controller.

majority of MPVRMs voltage-mode control scheme with linear compensation is applied to facilitate regulation due to its lean hardware requirements and relatively low design complexity [12]. Compared to the latter, Average Current Mode (ACM) control offers a good trade-off between inherent current sharing capabilities, reduced compensators' complexity, per-phase current-programming, and minor increase in hardware requirements [13]-[14]. While the ACM digital controller satisfies all steady-state requirements, transient performance due to large load perturbations is limited by the inner- and outer-loop dynamics, i.e. the system bandwidth. To satisfy transient requirements and accelerate the dynamic response of the VRM beyond its linear bandwidth limitation, transient-oriented non-linear control schemes [15]-[19], alongside the steady-state controller have been employed, realizing the hybrid controller architecture.

In addition to the core objective of voltage regulation, controllers are required to incorporate features to enhance the system's performance in both steady-state and transient conditions. Phase shedding procedure improves the overall system's efficiency by governing the number of active phases with respect to the loading condition [20]-[21]. By doing so, the system's performance is optimized so that each phase converter operates around its peak efficiency, resulting in overall improved efficiency for a wide range of output power [22]. Another essential feature of the controller is Active Voltage Positioning (AVP) procedure where the load voltage is adjusted on-the-fly according to the instantaneous load status [23]-[24]. By doing so, the heat dissipation of the load is adequately managed, allowing better utilization of the processor load, improves the allowed computing efforts. Implementation of these two prominent features is considerably eased when employing digital ACM control. Since both phase current information and the total current to the load is readily available on a cycle-by-cycle basis to the controller, programming of active phases and the target output voltage is a virtually inherent attribute of the controller and is facilitated efficiently with minor additions to the digital controller.

The objective of this study is therefore to introduce an all-digital realization of advanced control features for high-end MPVRM hybrid controllers, as shown in Fig. 1. The implemented features offer improvements in converter's efficiency without compromising on transient suppression capabilities, and provides programmable active voltage positioning as required by state-of-the-art high performance loads. The number of active phases is dynamically adjusted by the *Phase Activation Unit* (PAU) while maintaining minimal deviation of the state-variables. Transition between the steady-state ACM control schemes to transient acceleration is governed by an advanced hand-off procedure, ensuring smooth and seamless transition between the control laws. It is a further objective of this study to present in detail the practical effects of the measurement discretization on the controller design, its performance and limitations.

The rest of the paper is organized as follows: section II describes advanced key control features of MPVRM alongside the design considerations and realization details. Practical implementation issues of the hybrid digital controller are covered in section III. Experimental system implementation and validation are presented in section IV. Section V concludes the paper.

II. Important Features in MPVRM Controllers

A. Phase Shedding and Adding

The design of converters and selection of components are carried out to maximize efficiency for nominal load conditions but also to ensure proper operation under full-load in which all phases are active. For multiphase converters with equal phases, as the one shown in Fig. 1, the load requirements are satisfied by the active phases equally. Therefore, maximum efficiency is achieved where each phase delivers the nominal power to the output. For a multiphase converter with M possible active phases configurations, the efficiency curve can be extracted with M variations, having their maximum points at multiplications of the nominal power per phase. A conceptual efficiency graph for a 4-phase converter with 3 possible phase combinations (1,2 or 4 active phases) is shown in Fig. 2. As can be seen in Fig. 2, the efficiency of multiphase converters is a function of the load, as for single-phase converters, but also as a function of the number of active phases working in parallel. Since an accurate model of a multiphase converter's losses is a hard task to derive and may contain several degrees of freedom, the efficiency graphs are extracted based on experimental measurements. At light-loads, where the switching losses are more dominant, to maintain high efficiency a lower number of phases are activated. The controller modifies the number of active phases on-the-fly to maximize the converter's efficiency as a function of the load condition based on the information extracted from the efficiency graph. This procedure is referred to as "*Steady-State Operation*" in the flowchart of Fig. 3.

In this study, the load current information is extracted from the inner current loops reference, v_c, which is the product of the, outer voltage regulation loop (Fig. 1). Since this process is relatively slow compared to the cycle-by-cycle information, the value of v_c is fed into a digital LPF (implemented as a moving-average). This also avoids singular calculation or sampling errors from triggering the *Phase Activation Unit* (PAU). The resultant average value of

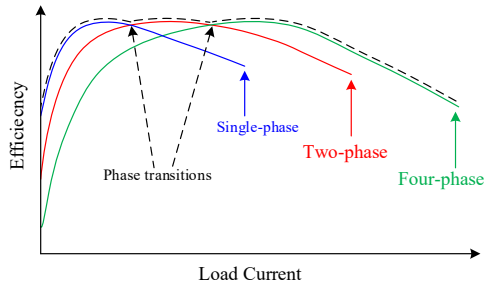

Fig. 2. Typical efficiency graph of a multiphase buck converter operating with one, two or four parallel phases.

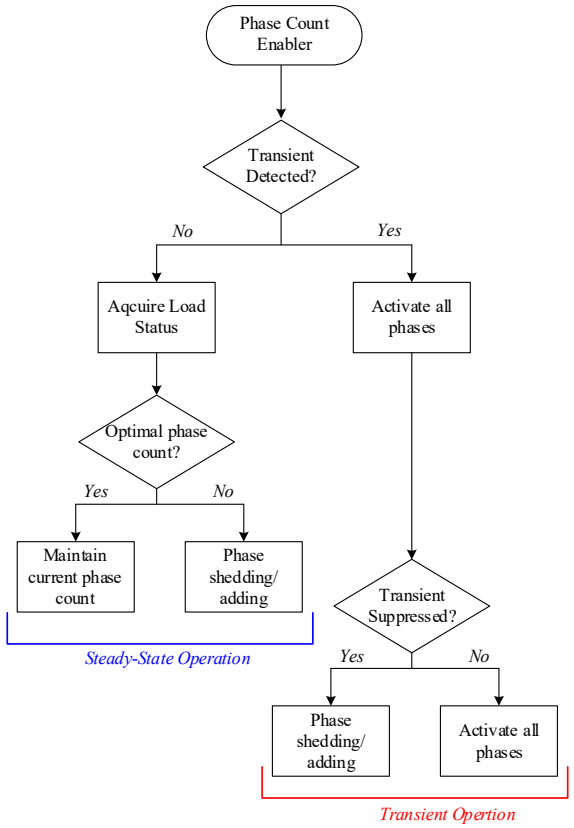

Fig. 3. High level flowchart of the PAU operation.

v_c is the input to a LUT which determines the number of active phases.

In case the load has dropped, phase shedding procedure carried by the PAU is initiated. For simplicity, the procedure is described, with the aid of Fig. 4 for a 2-to-1 transition but applies for any other phase shedding transitions. It should be noted that, prior to any change in the number of active phases, current balancing is enforced by the ACM control scheme, as shown in Fig. 4. The reference to the inner current loop of the shedded phase is bypassed with a value equals to $v_{c\_sh}[n]$, while the remaining phase operates in the original dual-loop configuration. Upon initialization, $v_{c\_sh}[n]$ equals to $v_c[n]$-1 and gradually decreased every N_{sh} switching cycles. Since the inner current loop of the shedded phase remains active, its inductor current tracks v_{c_sh} which allows supervised current ramp-down. The remaining phase, which its current is regulated by the ACM, ramps up its current to compensate for the shedded phase. This results in a gradual phase shedding scheme with no voltage deviations or current spikes. Once v_{c_sh} reaches zero, the shedded phase is completely turned-off by the controller. The duration of each step can be altered but must be sufficiently long to allow the remaining phase to ramp its current. For an increase in the load requirements, similar procedure takes place in which the added phase's inner loop reference is gradually ramped up every N_{sh} switching cycles. The phase adding procedure ends when v_{c_sh} equals v_c, which ensures that the currents of both phases are equal.

Another incentive to change the number of active phases is to enhance non-linear transient recovery patterns. Upon

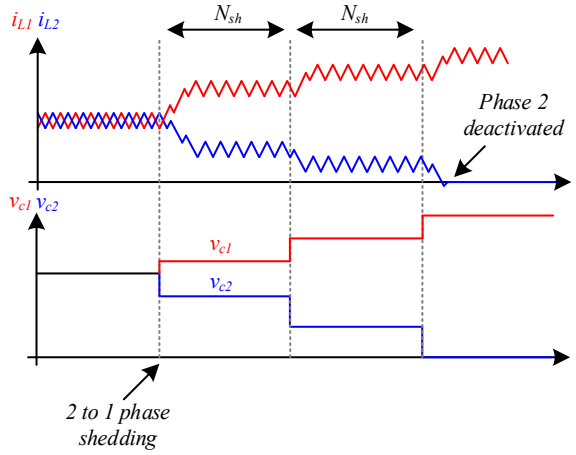

Fig. 4. Inductor currents and inner current loops reference values during a 2-to-1 phase-shedding procedure.

transient detection, the linear controller is bypassed and the drive signals to the power switches are produced by the non-linear controller (*Large-Signal Compensator* Fig. 1). In this study, minimum deviation control is executed to suppress extreme transient events which exceed the regulation capabilities of the linear controller [25]-[26]. For both loading and unloading transients, the current slew-rate sets a limit on the recovery duration [25]-[26]. Therefore, the PAU sets the maximal number of phases upon transient detection to shorten the transient duration by increasing the effective current slew rate. This procedure is referred to as "*Transient Operation*" in the flowchart of Fig. 3.

The current ramp up/down phase in the large-signal compensation can be implemented with different levels of phase synchronization during transient. Fig. 5 shows three options for ramp-up initiation with and without phase synchronization, each with its pros and cons. The first option in Fig. 5a maintains phase synchronization while also addressing the transient with the closest phase available upon detection, in this case the dashed line phase continues it ON state immediately upon transient detection. The second option in Fig. 5b is to maintains full phase synchronization during transient when each phase is turned on at the beginning of its next cycle respectively. The third option is to turn all available phases as soon as transient event is detected, as a result, this method presents the poorest phase synchronization, nevertheless the transient performance is superior in comparison to the first two methods. When looking into the current sharing attribute during transient time the latter option maintains good current sharing, while the worst current mismatch possible is the size of the current ripple. In this study, the method described in Fig. 5c is chosen due to the fastest transient performance as well as current sharing attributes. Another advantage of this method is that during a transient event, the system can be treated as a single-phase buck converter, with effectively increase bandwidth and with effective inductance, L_{eq}, is given by $L_{eq}=L/N$ (N is the number of phases, four in the example of Fig. 5). Once the transient event has been suppressed the PAU returns to

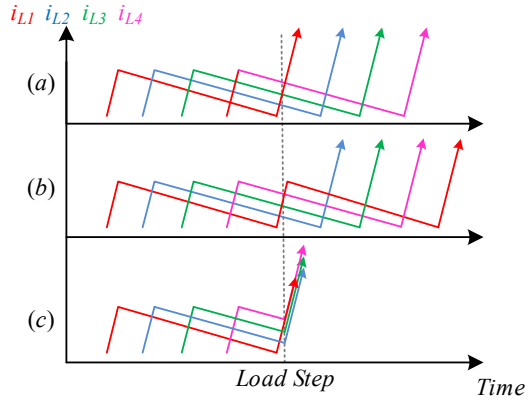

Fig. 5. Comparison between different phase adding methods during load transients.

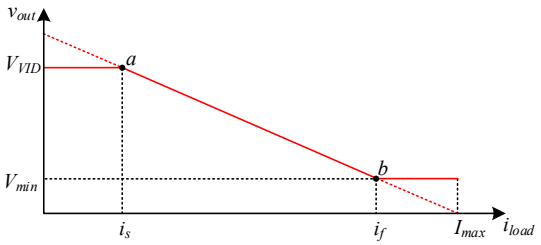

Fig. 6. Programmable piecewise linear load line function.

its steady-state operation, observes the new loading condition and adjusts the optimal number of active phases accordingly.

B. AVP

The core purpose of the AVP unit is to design the output resistance (R_o) of the MPVRM, in its most simplistic implementation the output voltage is dynamically adjusted according to the load current status. In the majority of systems a linear constant output impedance behavior is sufficient to address the load requirements, such linear AVP function dictates that output voltage decreases from its zero-load value (V_{VID}) as the load current grows, as expressed in (1). Using a straightforward differentiation, the dynamic range of the MPVRM output voltage can be derived from (1) and extracted in (2):

$$v_{out} = V_{VID} - R_o i_{load}\,, \tag{1}$$

$$\Delta v_{out} = -R_o \Delta i_{load}\,, \tag{2}$$

where Δi_{load} is the load current range and R_o is the desired output impedance.

Although the linear AVP function in (1) is realized in analog controllers with relatively moderate design efforts, the implementation of more complex functions like piecewise-linear or non-linear functions may increase the controller design complexity drastically. The digital control used in most state-of-the-art MPVRM controllers supports complex AVP functions as shown in Fig. 6, reduces design complexity and offers real-time calibration of the AVP function. In this study the digital AVP function is introduced in Fig. 6, at low loading conditions the output voltage remains constant until the load current surpasses the bottom threshold i_s, from this point and up to a load current of i_f the output voltage follows a constant output impedance function similar to (1). For load currents larger than i_f and up to I_{max} the load maximum current, the output voltage remains constant and equal V_{min}.

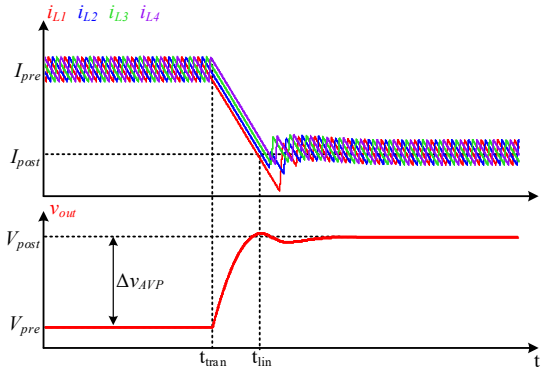

Fig. 7. AVP procedure after load transient event.

Traditional AVP operation is a relatively slower process than the voltage loop response, to prevent undesired voltage oscillations and assure tight voltage regulation at steady-state. In modern MPVRMs, however, the load is capable of having fast and large transients that require a non-linear solution to ensure the desired load-line constraints are kept at all times. Fig. 7 demonstrates the AVP unit non-linear operation during a large unloading transient event. Ideally, when the non-linear transient mitigation is complete at t_{lin}, the output voltage is then steered by the linear controller to its desired post-transient level (V_{post}), as prescribed by the AVP unit. Since transient events may be extremely short due to small inductor values used in high performance MPVRMs (resulting in high current slew), the duration of the non-linear mitigation operation t_{lin}-t_{tran} (acquired by the controller during transient) can be used to estimate the current step and change V_{ref} accordingly.

In comparison to an analog implemented AVP unit, the digital AVP unit may encounter resolution issues where the minimal output voltage quantization step is limited by the voltage ADC sampling resolution. Since the unity change in V_{ref} is translated to a small step in v_{out} the smooth load line profile of Fig. 6 is realized in a discrete manner. Enhancing the ADC resolution in order to solve the AVP profile discretization is limited by the system PWM resolution to prevent limit cycle oscillations. Filtering the AVP result improves noise immunity and profile discretization having minimal impact on the bandwidth of the AVP function.

C. Hand-off

The transition from the non-linear controller operation executing minimum deviation control to the small-signal based linear controller is referred to as *Hand-off*. It comprises a set of adjustments to the internal control signals as well as to the duty-cycle commands of the different phases. The hand-off procedure from non-linear control operation in a lossless converter can be executed by assigning the pre-transient values, while in practice if the post-transient control signals (both internal and external) are not modified to compensate for the losses in the system, additional settling

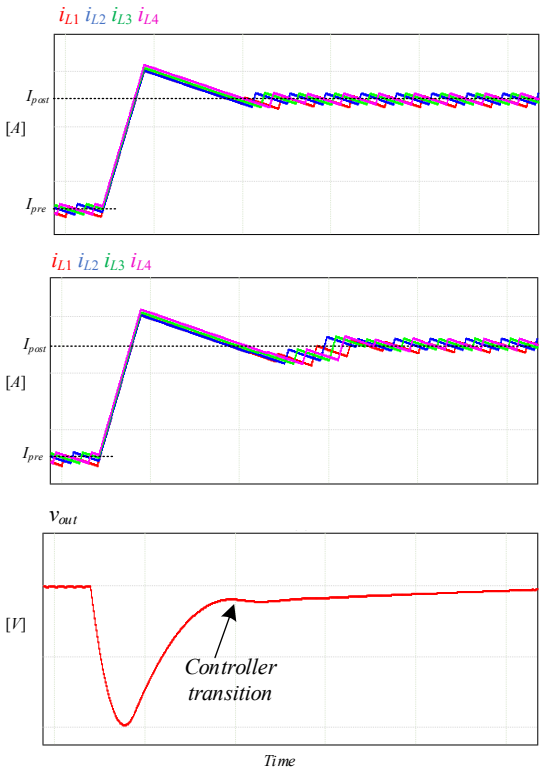

Fig. 8. Hand-off procedure after a loading event for a 4-phase converter. (a) Inductor currents in case the internal and external control signals are compensated. (b) Inductor current without post-transient modifications of the control signals. (c) Output voltage for the implemented hand-off procedure (red) and for the uncompensated procedure (blue).

transients may occur. In this study, ACM control scheme has been realized (Fig. 1) for the steady-state operation, therefore both the reference to the inner current loops, v_c, as well as all duty-cycle commands are modified based on the duration and the polarity of the transient event. Once the hand-off procedure is initiated, the controller operates in open-loop for a single switching cycle with the modified duty-cycle before closed-loop operation is resumed.

Upon transient detection, the duty-cycle of the leading phase, D_0[n], and the current loop reference, v_{co}[n] are sampled and stored in dedicated registers. For a loading transient, the modified duty-cycle, D_{tr}, is calculated by the following:

$$D_{tr} = D_0 + k \cdot t_o \frac{V_{in} - V_{out}}{L}, \quad (3)$$

while for an unloading transient the following is used:

$$D_{tr} = D_0 + k \cdot t_o \frac{V_{out}}{L}, \quad (4)$$

where k is a proportional constant derived during the design process and t_o[n] is the duration of the transient recovery period estimated by a counter-based module. By performing a current-sweep test of the multiphase converter, operation of the entire load range is validated and duty-cycle values are stored in the system for a wide range of loading conditions. Plotting these values as a function of the load current and extrapolating results in a linear curve with a slope equals to k. The inner current loops reference is also updated in a similar manner as in (3)-(4), taking into account the sampled v_{co} value and the load step information stored as t_o[n]. Once closed-loop operation is enabled, fine adjustments are performed by the steady-state controller to the duty-cycle commands to achieve accurate current matching.

A set of simulations has been conducted in PSIM (PowerSim, Inc.) to verify the effectiveness of the hand-off procedure and to validate the accuracy of the extracted value for k. Fig. 8a shows inductor currents for a 4-phase converter controlled by the hybrid controller during a loading transient. Upon transient detection the large-signal compensator (Fig. 1) takes over the task of producing the gating signals to the power switches as well as the calculation of the post-transient values for the duty-cycle and v_c. Once the transient is supressed, these values are assigned, resulting in a smooth transition with no current overshoots or output voltage deviations, as shown in the red curve of Fig. 8c. Fig. 8b illustrates a case where no adjustments are made to the internal control signals, resulting in prolong convergence time in addition to a small settling transient, as shown in the blue curve of Fig. 8c.

III. Practical Implementation

To successfully achieve the design goals, the realization of algorithms and control schemes must consider the practical limitations of the platform. Aspects such as quantisizers' resolutions and calculations complexity are detailed in the following, and provide design guidelines for choosing ADC resolutions and protection circuitry for dual-loop controllers.

A. ADC resolution limitations

The quantization effects are prominent contributors of oscillations in steady-state. For high performance VRMs, high steady-state accuracy is required but at the same time, caution must be exercised to avoid limit-cycle oscillations [27]-[28]. A no-limit-cycle condition must be kept to ensure high quality voltage regulation. This condition is derived from the resolution of the ADCs and DPWM units in the control loop. DPWM resolution is usually the limiting factor due to its dependency on hardware limitations. Increasing the DPWM resolution in counter-based modules translates to increased power consumption and more complex design to realize the high-speed circuitry.

For voltage mode control schemes based on a single loop configuration the no limit-cycle condition is determined by the relation between the DPWM resolution, q_{pwm}, and the voltage sampling ADC resolution, q_v. In current mode control schemes, such as ACM, the additional inner current loop independent operation results in a more complex no limit-cycle condition which considers the current ADC resolution, q_i, in addition to q_{pwm} and q_v. The first sub-condition is to prevent oscillations in the inner current loop. The minimal change to the output voltage which is defined by the product of the current sampling ADC resolution and

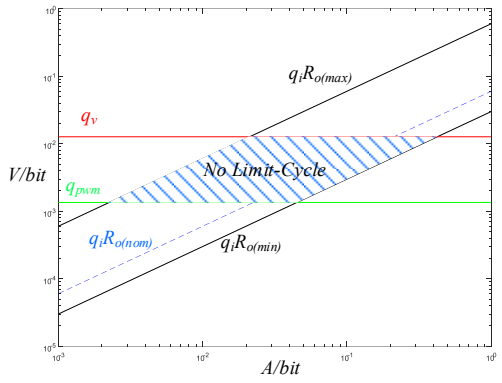

Fig. 9. Graphical representation of the MPVRM controller quantisizers' resolutions: voltage ADC resolution (red), DPWM resolution (green) and the upper- and lower-boundaries of the current resolution (black).

the equivalent output resistance, R_o, must be larger than the DPWM resolution. Due to the superior control bandwidth of the inner current loop, the quantization effect of the DPWM becomes transparent to the outer voltage loop. The second sub-condition is to prevent oscillations in the outer voltage loop. Assuming the inner current loop sub-condition is satisfied, it can be modeled as a controlled current source with resolution of q_i, therefore the fundamental output voltage resolution is $R_o q_i$. This dictates the voltage ADC resolution to be greater than $R_o q_i$. Taking into account both sub-conditions, a unified no limit-cycle condition can be expressed as:

$$q_{pwm} < q_i \cdot R_o < q_v \,, \tag{5}$$

where R_o is the output impedance of converter. The resolution of the PWM unit is calculated according to:

$$q_{pwm} = \Delta D \cdot V_{in} = \frac{T_\Delta}{T_s} \cdot V_{in} \,, \tag{6}$$

The dynamic response of STC with self-tuning control, has been verified by a set of simulations conducted in PSIM (PowerSim, Inc.). Among the simulated cases are convergence to ZCS of matched and mismatched tanks under various where T_Δ is the corresponding time difference due to a change in the LSB of the DPWM command, T_s is the switching-cycle duration and V_{in} is the input voltage of the converter. q_i and q_v values are derived from the analog-to-digital converter topology and can be adjusted to satisfy the no-limit-cycle condition for dual-loop based PWM converters, as shown in (5). As previously detailed in precursor of this study [28], the ADC of the controller is based on a fully-synthesizable delay-line based analog-to-digital converter topology has been utilized which ensures high sampling resolution with relatively low power and area requirements.

A graphical based solution of the no-limit-cycle condition of (5) is illustrated in Fig. 9. Here, the ADC resolutions are indicated for the general case by q_i and q_v, the maximum output impedance as $R_{o(max)}$ and the its minimum value as $R_{o(min)}$. The resolution of the current ADC is chosen to be greater than q_{pwm} to prevent limit-cycle oscillations in the inner current loop while the voltage ADC resolution is set to be higher than q_iR_o for the entire range of output impedances. Following these design guidelines result in a "*No Limit-Cycle*" region, as shown in Fig. 9.

The chosen resolution of q_i and q_v may become a limiting factor in the implementation of the control features detailed in II. For example, a trade-off exists between the q_v value determining the thickness of the "*No Limit-Cycle*" region and the discretization of the AVP profile.

IV. Experimental Results

The advanced VRM controller features introduced in this paper have been validated using a 12V-to-1.2V four-phase MPVRM. An experimental prototype with all the analog front-end peripherals required for the validation of the controller and its advanced features has been built and tested. The MPVRM parameters are shown in Table I. Fig. 10 shows the experimental prototype setup, which comprises a specifically designed PCB to supply DDR memory, digital controller realized on FPGA, and an Intel-certified DDR4 load emulation modules. Each DDR4 module capable of sourcing or sinking up to 14A and the gating signal pattern is generated by a signal generator, asynchronous to the controller operation. The digital core hybrid MPVRM controller combined with all the required features introduced in this paper and costume-made peripherals such as digital multiphase PWM and DL-ADC has been entirely implemented on a Cyclone V FPGA.

TABLE I – Experimental Prototype Parameters

Parameter	***Value/Type***
Input voltage V_{in}	12V
Nom. output voltage	1.2V
Power stage	SiC820, 70A
Inductor	120nH
Output capacitance, C_{out}	5mF
Switching frequency, f_{sw}	450KHz
AVP function slope	2mΩ

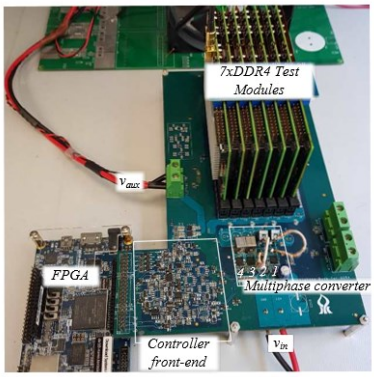

Fig. 10. Four-phase multiphase buck VRM experimental setup, including all the front-end peropherals and seven DDR4 test modules.

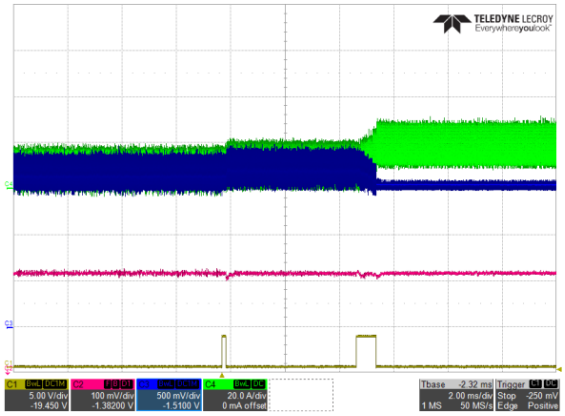

Fig. 11. 4-to-1 Phase shedding in low-power (20A) steady-state operation.

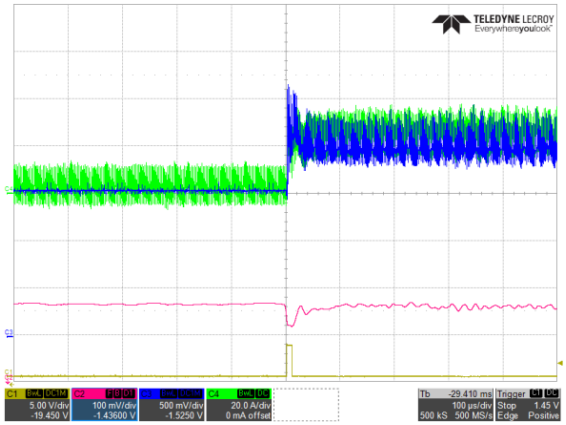

Fig. 12. 1-to-4 Phase adding during a loading transient event of 5A to 90A.

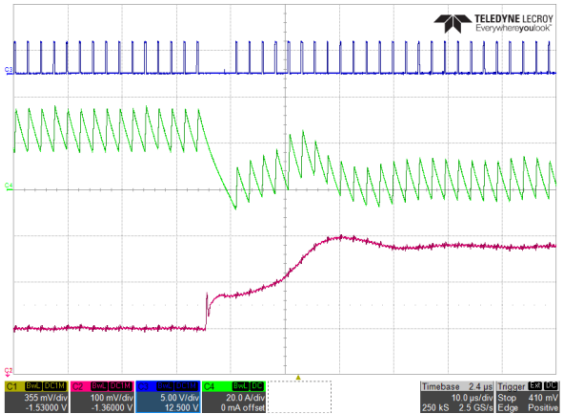

Fig. 13. Multiphase buck converter's response to a 90A-5A unloading transient with AVP function unit realizing a load line of 2mΩ.

Fig. 11 shows the MPVRM's operation during phase shedding operation carried out by the controller. Here phases are shaded out as a result of low required output power to further improve the overall VRM efficiency. As shown by the shedding indicator in Fig. 11 the full 4-phase operation is trimmed down to two-phase operation and eventually to single-phase operation. The impact of the shedding processes on the output voltage is neglectable, due to the governed

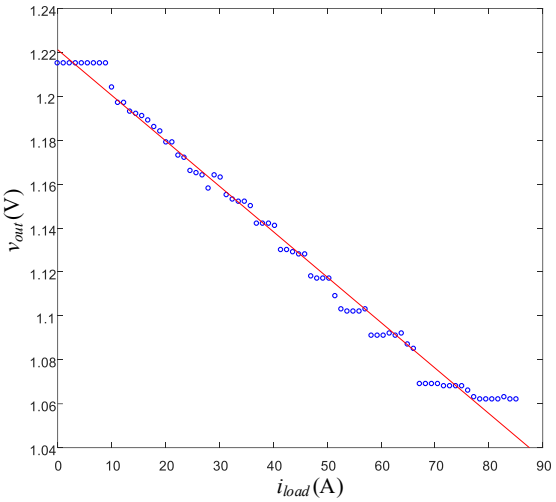

Fig. 14. Experimental results of the load-line function (blue markers) and the equivalent trendline of the results (red) indicating a 2mΩ slope.

shedding process described in II, the largest voltage deviation is measured to be less than 20mV.

Fig. 12 demonstrates the phase adding feature in a case of a loading transient event with a load step of 85A. Once the transient event has been detected by the controller, the phase activation unit ramps-up all the available phases to provide the best transient performance. As opposed to steady-state operation, the PAU enhances transient suppression by providing zero lag reaction to transient event detection, as detailed in II. The instantaneous phase adding also helps preventing high peak current stress on the single operating phase (i_{L1}) that otherwise would have supplied up to four times its peak value to accommodate the transient event.

The AVP unit operation during a 90A-5A unloading event of the load current is depicted at Fig. 13. During transient suppression the load voltage, v_{out}, rises by 70mV (Δv_M). Given a 2mΩ load-line profile, the output voltage has to change its value by another 90mV to complete its full 160mV swing of Δv_{AVP}. The additional elevation in v_{out} is carried out by the linear controller and settles at 160mV above the pre-transient output voltage value. The experimental validation of the AVP profile is depicted in Fig. 14 where the piecewise linear profile results are shown in blue. The AVP function slope is validated using extrapolation for the constant output impedance region shown in red and demonstrating a 2mΩ slope in accordance to the load requirements.

V. Conclusion

An all-digital implementation of advanced control features for high-end MPVRM has been introduced an demonstrated using a four-phase experimental prototype and DDR4 emulation test modules. The features are incorporated into a hybrid current programmed digital ACM controller architecture. Phase shedding feature facilitated by the all-digital PAU provides negligible voltage deviation during

shedding/adding process by taking advantage of the ACM controller architecture. Digital AVP function has been realized to support high-performance loads thermal restrictions by dynamically adjusting the output voltage in respect to the load current status. The transition between control laws within the hybrid controller is carried-out by a hand-off procedure, minimizing post-transient convergence to steady-state operation.

The experimental prototype featured a 4-phase 12V-to-1.xV buck VRM driving Intel-certified load emulator. A hybrid digital controller with all-digital AVP, phase shedding and hand-off functions has been realized, demonstrating excellent steady-state and transient operation for a wide range of load currents.

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