

Transient Suppression Scheme for Mitigation of High-Performance VRM Intricate Load Profiles

Bar Halivni, *Student Member, IEEE*, Tom Urkin, *Student Member, IEEE*,
and Mor Mordechai Peretz, *Member, IEEE*

The Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev, P.O. Box 653, Beer-Sheva, 8410501 Israel
barhal@post.bgu.ac.il, tomur@post.bgu.ac.il, morp@bgu.ac.il
<http://www.ee.bgu.ac.il/~pemic>

Abstract— This paper introduces a non-linear control scheme that supports near ideal transient recovery for high-frequency high-di/dt load-transients that exceed the control bandwidth in single-phase and multiphase buck converter VRMs. The new algorithm adapts the switching sequence for recovery using information obtained from a simple, plug-and-play, comparator-based observer of the output voltage. Detailed control algorithm is provided as well as implementation considerations for high-performance multiphase VRMs. The new control method is demonstrated via simulation on a multiphase VRM for complex load-profiles. Experimental verification has been carried out by intel certified-hardware of DDR4 emulation modules on a 12V-to-1.2V 120W multiphase buck VRM accommodating 80A load transients.

Keywords – Digital control, hybrid control, multiphase, buck, VRM, DDR.

I. INTRODUCTION

A target feature of high-power, high-performance, VRMs is the ability to maintain a well-regulated, virtually constant, output voltage under wide and rapid load changes. These VRMs can be found in state-of-the-art cloud computing, IoT, automotive and AI applications that facilitate a relatively large number of high-performance loads such as CPUs, FPGAs and DDR memories [1]-[3]. These loads present unique loading profiles that stem from their operating nature and introduce new challenges beyond single-step conventional load transients [4]-[5]. The complex loading patterns feature consecutive high step-repetition rate (SRR), variable slew-rate and magnitude load-transients. To minimize the output voltage deviation during load-transients, the common practice is to enhance the control bandwidth which results in fast ramp up/down of the current to the load so that minimal charge deficiency at the output capacitor is facilitated. In some cases, the load-transient frequency may exceed the controller's VRM maximal bandwidth, thus the output voltage is unable to fully recover between two adjacent load-transient events. This may result in extensive output voltage deviation beyond the allowed regulation boundaries, prolong recovery duration and may cause overall system failure.

Large-signal based control schemes such as minimum deviation or time-optimal control (TOC) [6]-[9] are commonly employed to achieve minimal output voltage deviation in buck derived converters. Such control schemes require dedicated sensing circuitry that identifies the output capacitor charge balance point based on output voltage information [6], [10]-[11]. Typically, these are complex circuitries that rely on either knowledge of the system parameters, or present calibration procedures to select the sensor's parameters for accurate results. Based on the information obtained from the sensors, TOC switching sequence is calculated according to [8]. Since the TOC recovery pattern relies solely on the information of the charge-balance point, any measurement inaccuracies or load changes past the charge balance instance will translate into an inadequate recovery pattern and increased output voltage deviation.

Non-linear control schemes for multiphase systems are designed to provide superior load-transient suppression for extreme load-changes in comparison to high-end linear controllers [12]-[14]. In order to become a viable solution non-linear control schemes must support additional control aspects, critical to multiphase VRMs such as current balancing, phase synchronization and interleaved operation [15]-[22]. One of the limiting factors for successful implementation of non-linear control methods in multiphase systems is the increased penalty due to any sensing

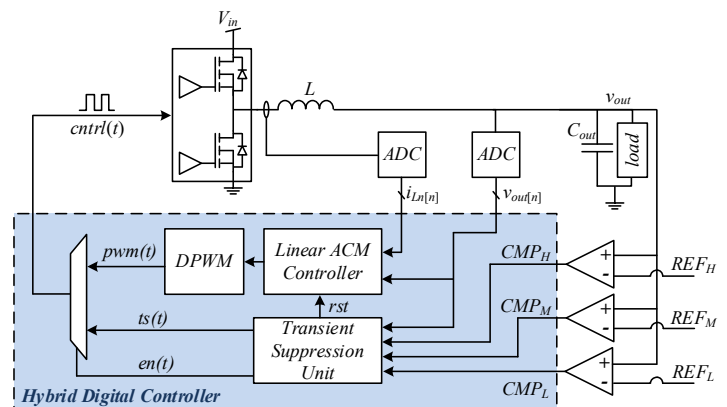


Fig. 1. Conceptual block diagram of the hybrid digital controller regulating a synchronous buck converter.

inaccuracies or calculation errors. This is since typical inductors' values of high-end multiphase converters are selected to provide high di/dt which translates any inaccuracy to large current errors. This is especially critical for high SRR applications, where TOC inability to react in real-time for rapid load-changes within its mitigation sequence results in state-variables divergence and ultimately overall system failure.

The objective of this paper is therefore to introduce a new control method for hybrid controllers to facilitate high Step Repetition Rate load transients and advanced loading patterns in high-performance VRMs, as can be seen in Fig. 1. The hybrid controller architecture comprises a steady-state controller and a transient suppression unit which realizes a state-space based non-linear switching sequence to facilitate a near-ideal transient mitigation of rapid and consecutive load profiles. The new controller doesn't require hardware modifications and is carried out through a classic dual-loop controller with conventional sensing and transient detection circuitry. In particular, the control approach is suitable for both single-phase and multiphase buck regulators in applications where the load transients' requirements are extremely stringent. High di/dt load transients as well as transient-within-a-transient events are handled by the TSU, carrying out a new mitigation sequence that relies solely on the converter's output voltage. A further objective of this paper is to discuss in detail implementation of the new controller in a high-performance multiphase VRM for DDR memories, covering transient suppression sequence and analog front-end adaptations.

The rest of the paper is organized as follows: Section II describes the high SRR transient suppression unit principle of operation. Section III covers implementation of the TSU in multiphase VRMs. Section IV provides the experimental verification. Section V concludes the paper.

II. HIGH SRR TRANSIENT SUPPRESSION UNIT PRINCIPLE OF OPERATION

High di/dt single-step load transients are frequently used to test and classify the dynamic performance of power supplies for the worst-case scenario in terms of output voltage deviation. TOC is the predominant method for single-step transient suppression by providing the minimum output voltage deviation within the minimum possible convergence time. Typical single-step load-transient recovery of the TOC method is demonstrated in Fig. 2 (blue). TOC employs a single on-off cycle and requires an indication of the load transient event (t_{step} in Fig. 2), its direction and the time duration from the start of transient until the point that charge balance is obtained, marked by t_{cb} [6], [10]. The switching sequence can be divided into two sections marked by the charge-balance instance. Prior to t_{cb} , the control sequence relies on the information from the extremum sensor to determine the exact location of the charge balance point and can respond to load changes that may occur without compromising transient performance. Beyond the charge balance point the gating signals to the converter are

calculated according to the time difference between t_{step} and t_{cb} , thus preventing the adaptation of the switching sequence timings to accommodate additional transient events [8].

In addition to single-step load-transients, modern high-performance loads such as DDRs and CPUs may exhibit more complex loading patterns such as high SRR and variable load-current slew-rate. Applying TOC on non-single-step loading transients may lead to extensive over compensation that results in output voltage deviations, as can be seen in the red curve of Fig. 2. Here, a case of high SRR is simulated in which an unloading transient event occurs after the charge-balance instance is reached (t_{unload}). As can be seen, the TOC sequence does not take into account the charge that is injected into the output capacitor due to the secondary unloading transient event, resulting in extensive output voltage overshoot. The TOC insensitivity to subsequent load changes with more complex loading patterns may result in overstepping the regulation boundaries of the VRM or lead to false re-triggering of the TOC sequence.

In state-of-the-art VRMs implementing TOC requires high-performance complex analog interface in order to detect the charge-balance instance with sufficient accuracy. The added penalty of implementing a high-end analog interface is a non-negligible factor that stems from extreme hardware requirements to achieve the performance goals such as overall silicon area, power consumption, accuracy and control resolutions. In addition, to obtain the correct on-off switching pattern, tedious and time-sensitive calculations are carried out in the TSU based on the information extracted from the extremum sensors. This translates into non-negligible computation resources and relatively high-frequency internal clock circuitry.

To support high SRR and complex load-transients, such as transient-within-a-transient, the TSU executes a new non-linear control scheme that utilizes simple comparator-based

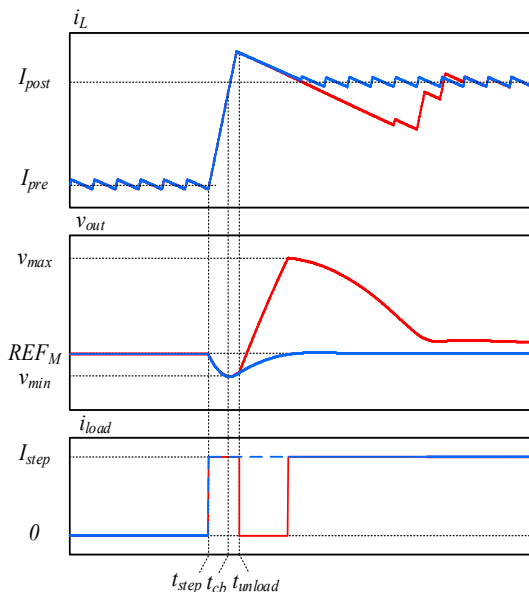


Fig. 2. Time-optimal control load-step transient recovery for (blue) single load-step and (red) complex dual-step loading pattern.

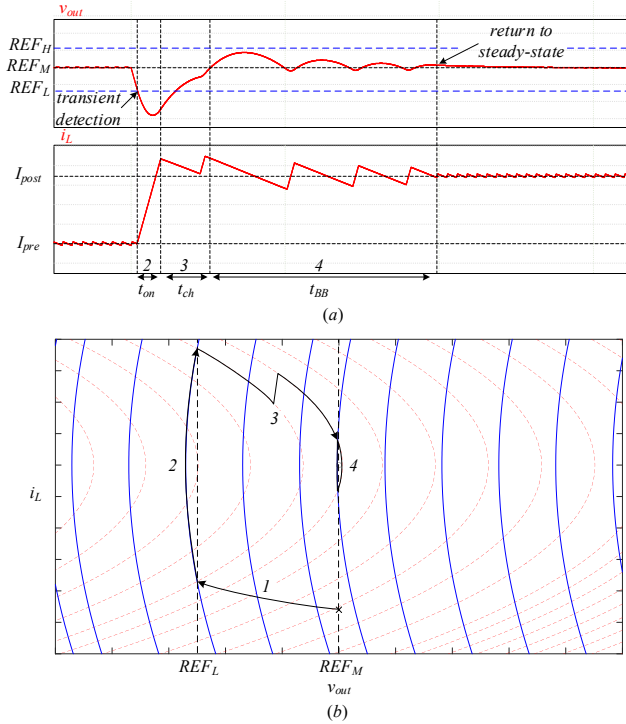


Fig. 3. Typical waveforms of the converter operation during a loading-transient event. (a) Output voltage (top) and inductor current (bottom). (b) State-plane representation of the output voltage and inductor current.

analog interface and requires low computational resources. The operation of the TSU during a loading-transient event is shown in Fig. 3 and is described with the aid of the flowchart of Fig. 4. Prior to the transient event the converter steady-state operation is handled by a dual-loop ACM controller [23]-[27] which performs the output voltage regulation for small load changes and keeps the output voltage confined within the steady-state window defined by REF_H and REF_L , as shown in Fig. 3a. As a result of a load-step the output voltage deviates due to the charge imbalance in the output capacitor, C_{out} , until the lower threshold is crossed as indicated in phase '1' of Fig. 3b.

Upon loading-transient detection the TSU bypasses the steady-state controller and produces pwm signals according to the loading branch in the flowchart of Fig. 4. First, the high-side transistor is turned-on to provide the best possible transient response until the output voltage returns to the steady-state window and the missing output capacitor charge is recovered. The duration of this phase is denoted as t_{on} in Fig. 3a and the state-variables movement across the state-plane is illustrated in phase '2' of Fig. 3b. At the end of the second phase, the remaining charge deficiency can be expressed as:

$$\Delta Q_{C_{out}} = C_{out} REF_M - C_{out} REF_L, \quad (1)$$

The remaining charge is recovered by a charge-injection on-off mitigation sequence that is initiated at the end of the second phase and ends when the output voltage reaches its nominal value, i.e. REF_M , as denoted in Fig. 4. During the charge-injection phase, the TSU employs pre-calculated

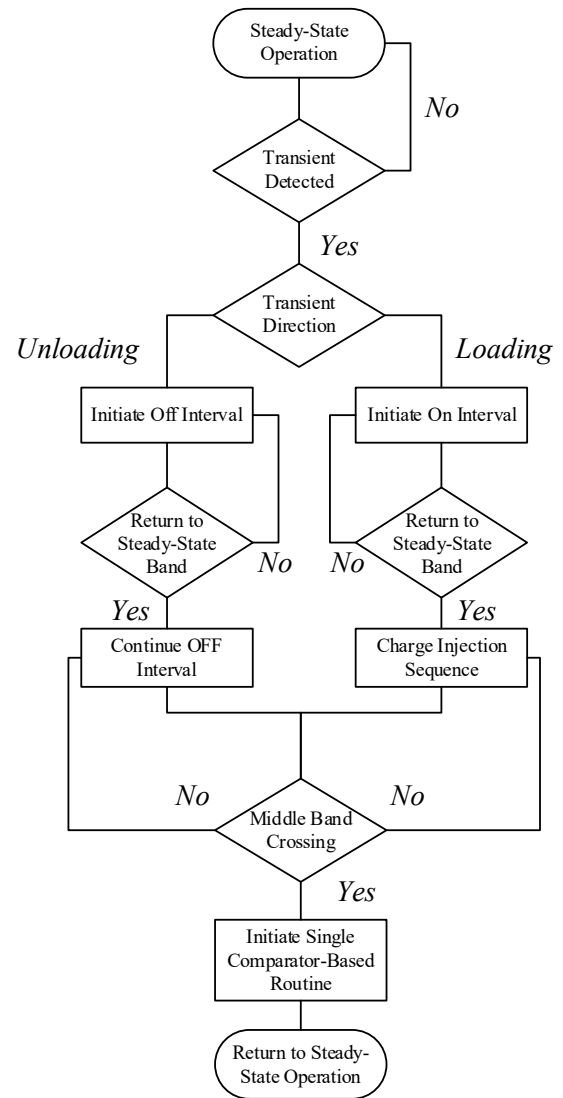


Fig. 4. Flowchart of the transient suppression unit's operation.

periodic on-off switching sequence that ensures movement of the state-variables toward the nominal output voltage, regardless of the inductor current value at the crossing point of REF_L . The amount of charge injected to the output capacitor during each on-off cycle is expressed as:

$$\Delta Q_{CB} = T_{on}^2 \cdot \frac{V_{in}(V_{in} - REF_M)}{2REF_M \cdot L}, \quad (2)$$

where the on and off times are calculated according to:

$$T_{on} = \sqrt{\frac{(C_{out} REF_M - C_{out} REF_L) \cdot 2REF_M \cdot L}{V_{in}(V_{in} - REF_M)}}, \quad (3)$$

$$T_{off} = \sqrt{\frac{(C_{out} REF_M - C_{out} REF_L) \cdot 2 \cdot REF_M \cdot L}{V_{in}(V_{in} - REF_M)}} \cdot \frac{V_{in} - REF_M}{REF_M}. \quad (4)$$

Typical operation of the TSU during the charge-injection phase for a loading-transient is illustrated in the timing diagram of Fig. 3a with the movement of the output voltage towards REF_M marked as '3' in the state-plane representation of Fig. 3b. The time duration of the charge-injection phase,

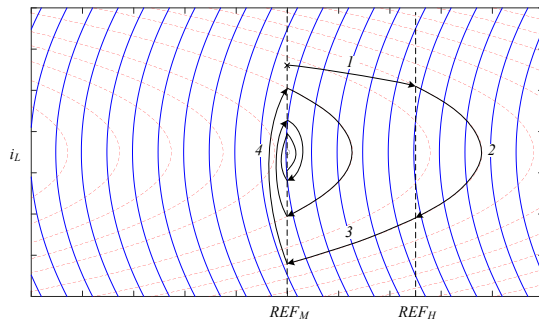


Fig. 5. State-plane representation of the output voltage and inductor current during an un-loading-transient event.

marked as t_{ch} in Fig. 3a, is a function of the output capacitor charge-imbalance at the end of phase 2 that is described by equation (1) and the load-status.

Once the nominal output voltage is reached, the TSU enters the final stage of the control algorithm, marked as ‘4’ in Fig. 3b. Previous phases of the TSU operation focused on converging the output voltage back to its steady-state value, REF_M . Therefore, the inductor current may not be positioned correctly for tight hand-off procedure that requires a good match between the load and the inductor currents [15]. During this step, the power-stage transistors are controlled by a single comparator for a pre-defined number of switching-cycles to ensure convergence of the inductor current to its new steady-state value. At the end of this phase, a hand-off procedure is carried out and the linear controller takes back control of the power-stage transistors.

The TSU operation during an unloading-transient event is shown in Fig. 5 and follows the ‘unloading’ branch in the flowchart of Fig. 4. Here, similar mitigation steps are executed with one significant modification where the charge-injection phase is replaced with constant conduction of the low-side transistor until the output voltage reaches its nominal value, REF_M . This is done to provide faster and tighter unloading-transient mitigation due to the differences in inductor slew rates during on- and off-times in buck-type converters and therefore the charge-injection phase can be omitted. Moreover, the TSU supports high SRR load transients by constantly monitoring the output voltage which allows real-time adjustments to the mitigation sequence regardless of the polarity of the loading-transient or its magnitude. In any case the output voltage triggers the steady-state window comparators the TSU returns to phase ‘2’. For small load-transients the duration of each phase will inherently adjust to accommodate any load changes.

III. IMPLEMENTATION OF THE TSU IN MULTIPHASE VRM

The load-transient recovery procedure discussed in Section II and executed by the TSU can be implemented in high-performance multiphase VRMs with minor adjustments to accommodate high phase-count operation. Since the TSU relies exclusively on the output voltage to generate the gating signals, a single shared analog interface is realized which results in reduced PCB area, power consumption and cost. Upon load-transient detection, the TSU takes control and

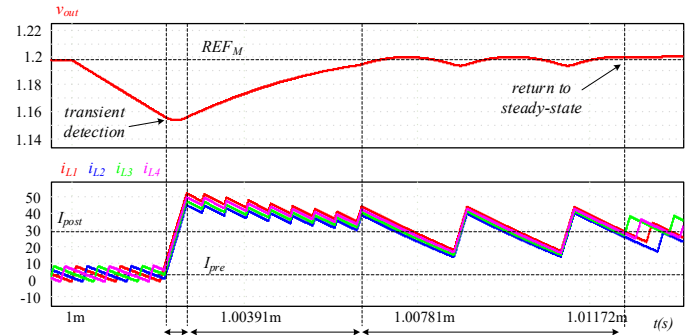


Fig. 6. Simulation results of a four-phase interleaved buck converter operation during 100A loading transient step.

applies the same switching commands for all available phases to provide the best possible transient suppression. This guarantees tight current sharing between all phases [16] and prevents divergence of the per-phase inductor currents during high SRR load transients. In addition, minimum on and off-time protection is implemented to prevent the power-stage from exceeding the maximal operation frequency. During TSU operation the multiphase converter can be modelled as a single-phase buck converter with effective inductor value of L/N , where N is the number of active phases. Therefore, the time-intervals of the charge-injection phase calculated according to (3)-(4) can be easily modified by replacing the per-phase inductor value with the effective inductance.

A set of simulations have been conducted using PSIM (PowerSim Inc.) to evaluate the TSU operation in a four-phase 12V-to-1.2V buck converter with output capacitor value of 5mF and per-phase inductor value of 120nH. The linear controller has been realized using dual-loop ACM architecture, as detailed in [16].

Fig. 6 demonstrates TSU operation for a 0A-100A transient event. As can be seen, once the loading-transient is detected by the comparator-based analog interface the TSU takes control and the interleaved operation of the linear controller is bypassed. The inductor currents are ramped-up with a slope of V_{in}/L until the output voltage returns to the steady-state window, marked as t_{on} in Fig. 6. Charge-injection phase is initiated and the modified on-off sequence is applied until the output voltage reaches its nominal value. In the case of Fig. 6, eight charge-injection cycles are required with total time-duration of t_{ch} . Prior to the hand-off procedure execution and return to steady-state, the TSU enters the single-threshold comparator-based stage (t_{BB}) as detailed in Section II.

The TSU operation for a 100A-0A unloading-transient is illustrated in Fig. 7. In a similar manner to the loading-transient case, the TSU takes control of the power-stage when the output voltage deviates outside the steady-state window. The low-side transistors are turned-on to ramp-down the inductors’ currents until the output voltage crosses REF_M , marked as t_{off} in Fig. 7. As can be seen, the TSU supports full synchronous mode operation where the inductors’ currents can turn negative to actively discharge the output capacitor to further induce the convergence time. As

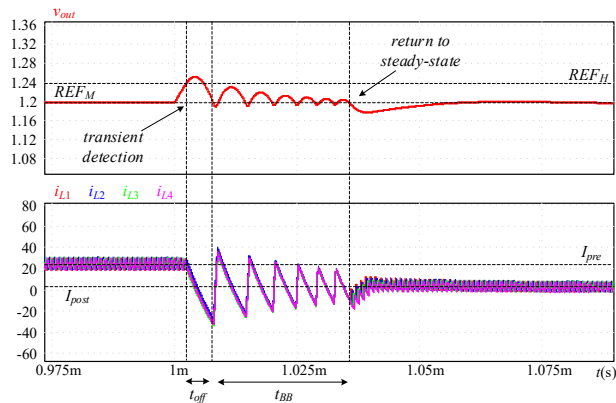


Fig. 7. Simulation results of a four-phase interleaved buck converter operation during 100A unloading transient step.

described in Section II, the charge-injection phase is omitted during unloading-transient mitigation and the TSU initiates the single-comparator based control sequence. The linear controller takes back control after the inductors' currents converge to the new operating point, marked as t_{BB} in Fig. 7.

The TSU's operation for complex and high SRR load-patterns is illustrated in Fig. 8. Here, the load status changes during the convergence period to allow verification of transient-within-transient scenarios. In addition, a variable-slope load-transient event is also simulated to validate the capabilities of the control algorithm to satisfy low slew-rate load changes. It can be seen that the TSU reacts to the pulsed load-transients by altering between loading and unloading transient suppression sequences (t_{sw}). In case the consecutive load-transient does not trigger the window comparators, the time-duration of the remaining mitigation phases inherently adopt with respect to the new charge injection rate to the output capacitor. Therefore, the large signal control scheme realized by the TSU can support a wide variety of loading patterns at high frequencies and react to rapid load-changes while maintaining tightly regulated output voltage.

IV. EXPERIMENTAL RESULTS

The hybrid VRM controller introduced in this paper alongside the high SRR TSU have been validated using a 12V-to-1.2V four-phase high-performance multiphase VRM. An experimental prototype with all the analog front-end peripherals required for the validation of the TSU operation has been built and tested. The multiphase VRM parameters are shown in Table I. Fig. 9 shows the experimental prototype setup, which comprises a specifically designed PCB to supply DDR memory, digital controller realized on FPGA, and Intel-certified DDR4 load emulation modules. Each DDR4 module is capable of sourcing or sinking up to 14A and the load current pattern is generated by a signal generator, asynchronous to the controller operation. The digital core of hybrid multiphase VRM controller alongside the TSU have been implemented on a Cyclone V FPGA.

Fig. 10 shows the transient response handled by the large signal compensator (TSU) of a loading transient event from

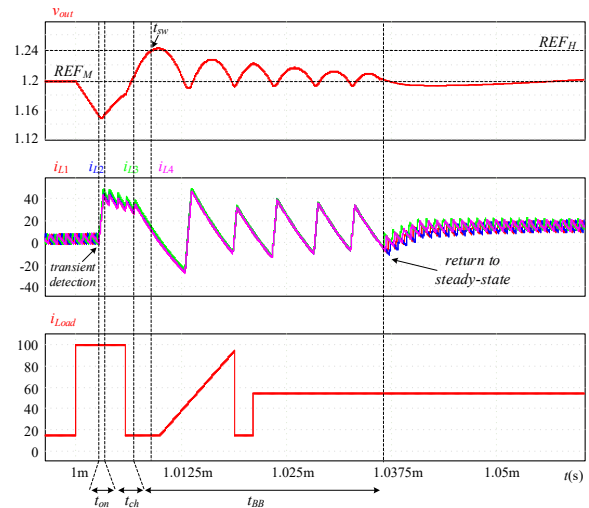


Fig. 8. Simulation results of a four-phase interleaved buck converter operation during a complex loading pattern with high SRR and variable load current slew-rate.

TABLE I – EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	Value/Type
Input voltage V_{in}	12V
Nom. output voltage	1.2V
Power stage	SiC820, 70A
Inductor	120nH
Output capacitance, C_{out}	5mF
Switching frequency, f_{sw}	900KHz

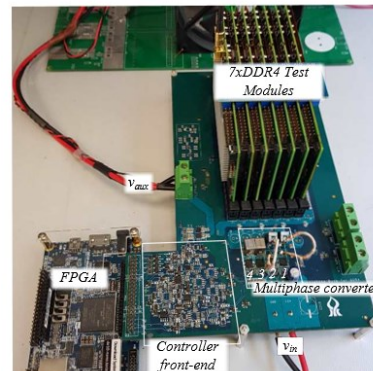


Fig. 9. Four-phase multiphase buck VRM experimental setup, including all the front-end peripherals and seven DDR4 test modules.

0A to 80A. i_{L1} represents the leading phase inductor current, stepping up from the average current of 0A per-phase to 20A as the load changes. The output voltage at the load point is denoted as v_{out} and shows a maximal voltage deviation of 60mV and a full recovery period after $17\mu s$. The override control signal which indicates the TSU operation is denoted as en shown in red alongside the control signal to the high-side transistor of the leading phase, $cntrl1$. As can be seen,

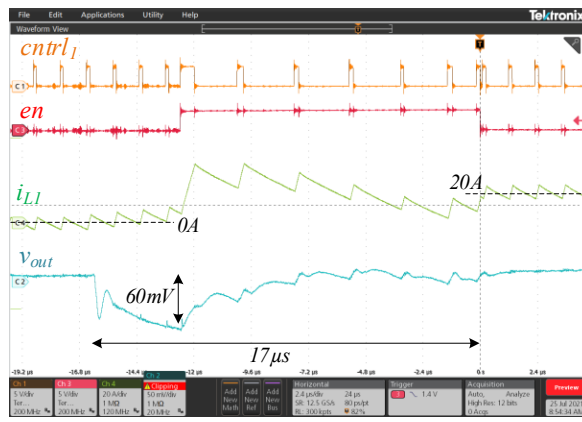


Fig. 10. Transient suppression unit experimental results for 0A–80A load-step during four-phase operation.

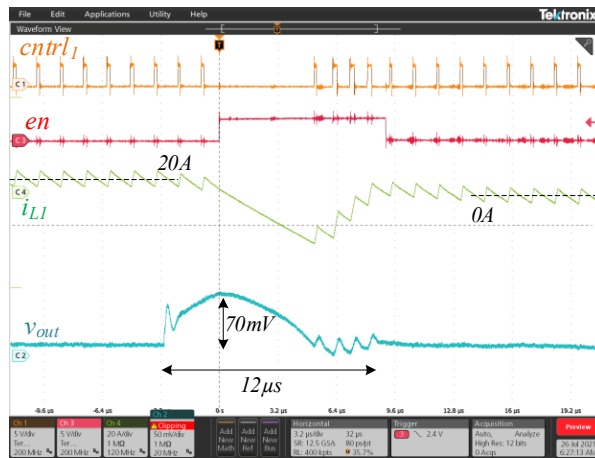


Fig. 11. Transient suppression unit experimental results for 80A–0A load-step during four-phase operation.

the charge-injection phase totals in 3 on-off switching-cycles.

Fig. 11 demonstrates the transient mitigation capabilities of the TSU during an unloading transient event from 80A to 0A. i_{L1} represents the leading phase inductor current, stepping down from the average current of 20A pre-phase to 0A as the load changes. Here, the maximal output voltage deviation is 70mV with a full recovery period of 12 μ s. The override control signal which indicates the TSU operation is denoted as *en* shown in red alongside the control signal to the high-side transistor of the leading phase, *cntrl1*. As can be seen, the charge-injection phase has been omitted according to the algorithm discussed in II to provide an enhanced transient suppression capabilities for the unloading case.

V. CONCLUSION

A non-linear control method for high-SRR high-performance loads has been presented achieving near-optimal transient-mitigation for a wide variety of loading-patterns. The control algorithm processes the information arriving from comparator-based analog interface directly from the output voltage to dynamically adjust the control sequence to provide the best possible transient recovery. This allows real-time adaptation of the drive signals to support

variable slew-rate and transient-within-a-transient events. The control algorithm has been validated experimentally on a 12V-to-1.2V prototype using intel-certified load emulator and demonstrated near-optimal transient mitigation capabilities of the TSU under extreme load-transient conditions.

ACKNOWLEDGMENTS

This research was supported by the ISRAEL SCIENCE FOUNDATION grant number 2186/19.

This research was supported by Vishay Ltd., Siliconix division.

REFERENCES

- [1] M. Dayarathna, Y. Wen, R. Fan, "Data Center Energy Consumption Modeling: A Survey," *IEEE Communications Surveys & Tutorials*, pp. 732-794, 2016.
- [2] Y.S. Kwon, C.M. Kyung, "ATOMi: an algorithm for circuit partitioning into multiple FPGAs using time-multiplexed, off-chip, multicasting interconnection architecture," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, pp. 861-864, 2005.
- [3] P. Velmlyl, "Developing Application Specific Integrated Circuits (ASIC) for cloud computing," *2011 International Conference on Electronics, Communication and Computing Technologies*, pp. 43-46, 2011.
- [4] A. Majumder, P. Bhattacharjee, "Current Profile Generated by Gating Logic Reduces Power Supply Noise of Integrated CPU Chip," *2017 IEEE International Symposium on Nanoelectronic and Information Systems (NIS)*, pp. 224-228, 2017.
- [5] Chroma, "High Slew Rate DC Electronic Load for VRM/VRD/Power Pod Testing", Model 63472 datasheet, available at: https://accusr.com/uploads/datasheets/5759_63472flyer.pdf.
- [6] A. Radić, Z. Lukić, A. Prodić, R. H. de Nie, "Minimum-deviation digital controller IC for DC–DC switch-mode power supplies" *IEEE Transactions on Power Electronics*, pp. 4281-4298, 2013.
- [7] G. E. Pitel, P. T. Krein, "Minimum-Time transient recovery for DC–DC converters using raster control surfaces," *IEEE Transactions on Power Electronics*, pp. 2692-2703, 2009.
- [8] E. Meyer, Z. Zhang, Y-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Transactions on Power Electronics*, pp. 1802-1812, 2008.
- [9] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, D. Maksimovic, "Proximate time-optimal digital control for synchronous buck DC–DC converters," *IEEE Transactions on Power Electronics*, pp. 2018-2026, 2008.
- [10] B. Halivni, M. M. Peretz, "Plug-and-Play Optimal Transient Mitigation Control Circuitry for High-Power High-Performance VRM," *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1-6 2019.
- [11] L. Jia, Y. Liu, "Voltage-Based Charge Balance Controller Suitable for Both Digital and Analog Implementations," *IEEE Transactions on Power Electronics*, pp. 930-944, 2013.
- [12] P. M. Cheng, M. Vasić, O. Garcia, J. A. Oliver, P. Alou, J. A. Cobos, "Multiphase buck converter with minimum time control strategy for RF envelope modulation," *IEEE Applied Power Electronics Conference and Exposition*, pp. 904-909, 2011.
- [13] J. Alico, A. Prodić, "Multiphase optimal response mixed-signal current programmed mode controller," *IEEE Applied Power Electronics Conference and Exposition*, pp. 1113-1118, 2010.
- [14] K. B. Cheng, M. Drenzo, "Auto-tuning of hybrid ripple-based constant on-time control for fast load transients and dynamic voltage

- transitions of multiphase voltage regulators," *IEEE Applied Power Electronics Conference and Exposition*, pp. 224-229, 2017.
- [15] B. Halivni, T. Urkin, M. Mordechai Peretz, "Advanced Control Features of Hybrid Current-Programmed Digital Controller in Multiphase VRM Applications," *IEEE Applied Power Electronics Conference and Exposition*, pp. 2472-2479, 2021.
- [16] B. Halivni, M. M. Peretz, "Digital Controller for High-Performance Multiphase VRM with Current Balancing and Near-Ideal Transient Response," *IEEE Applied Power Electronics Conference and Exposition*, pp. 2206-2213, 2020.
- [17] W. Huang, G. Schuellein, D. Clavette, "A scalable multiphase buck converter with average current share bus," *IEEE Applied Power Electronics Conference and Exposition*, pp. 438-443 vol.1, 2003.
- [18] C. Y. Yeh, L. S. Yang, T. J. Liang, R. L. Lin, J. F. Chen, H. T. Yang, "Digital and analog hybrid control of multiphase power modules with low output-voltage and high output-current," *International Conference on Electrical Machines and Systems*, pp. 2125-2129, 2008.
- [19] X. Zhou, P. Xu, F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1153-1162, 2000.
- [20] P. Zumel, C. Fernández, A. de Castro, O. García, "Efficiency improvement in multiphase converter by changing dynamically the number of phases," *IEEE Power Electronics Specialists Conference*, pp. 1-6, 2006.
- [21] W. Qiu, C. Cheung, S. Xiao, G. Miller, "Power Loss Analyses for Dynamic Phase Number Control in Multiphase Voltage Regulators," *IEEE Applied Power Electronics Conference and Exposition*, pp. 102-108, 2009.
- [22] Y. Su, K. B. Cheng, W. Wu, "High-efficiency multiphase DC-DC converters for powering processors with turbo mode based on configurable current sharing ratios and intelligent phase management," *IEEE Applied Power Electronics Conference and Exposition*, pp. 191-196, 2017.
- [23] Chunxiao Sun, B. Lehman, R. Ciprian, "Dynamic modeling and control in average current mode controlled PWM DC/DC converters," *IEEE Power Electronics Specialists Conference*, pp. 1152-1157, 1999.
- [24] G. E. Pitel, P. T. Krein, "Minimum-Time transient recovery for DC-DC converters using raster control surfaces," *IEEE Transactions on Power Electronics*, pp. 2692-2703, 2009.
- [25] Y. Qiu, X. Chen, H. Liu, "Digital average current-mode control using current estimation and capacitor charge balance principle for DC-DC converters operating in DCM," *IEEE Transactions on Power Electronics*, pp. 1537-1545, 2010.
- [26] S. Chattopadhyay, D. Somshubhra, "A digital current-mode control technique for DC-DC converters," *IEEE Transactions on Power Electronics*, pp. 1718-1726, 2006.
- [27] C. Jingquan, A. Prodic, R. W. Erickson, D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions Power Electronics*, pp. 411-419, 2003.