High-Conversion Ratio Multi-Phase VRM Realized with Stacking of Generic Series-Capacitor-Buck Converter Cells

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***Abstract*— This paper introduces a new design approach for multiphase nonisolated DC-DC topology. The design approach is based on a new generic hybrid cell that consists of both capacitor and inductor. Using a stand-alone cell, the approach contributes to a high modularity of the resulting converters and enables high conversion ratios at higher efficiencies. The unique interaction between the capacitor and the inductor result in a soft charging operation, which curbs the losses of the converter, and contributes to higher efficiency. The method was used to create a multiphase voltage regulator module VRM. The new converter significantly extends the effective duty ratio and lowers the voltage stress of the transistors, while delivering high current to the output and has inherent current sharing to balance the load between the phases. Experimental results of a modular interleaved three phase prototype demonstrate an excellent proof of design methodology concept and agree well with the simulations and theoretical analyses developed in this study. Typical applications are point-of-load (PoL) and voltage regulator modules (VRM).**

Keywords—Data center, DC-DC power converters, high conversion ratio, point-of-load converter, series capacitor buck converter, voltage regulator module.

I. Introduction

With the development of cloud computing and data centers, the demand for efficient, high-power consumption has grown significantly [1]-[5]. In recent years, DC distribution systems have been used widely to replace traditional AC systems in data centers due to their high levels of efficiency. The increased popularity of using 48 V DC power distribution networks in today's computing industry, where multiple CPUs and DRAMs are part from the main consumers, has reinforced the need for 48 V-to-1.x V PoL systems. The majority of modern supply methods consist of using either a two-stage conversion in series (48 V-to-12 V and 12-to-1.x V) or a direct-conversion approach (48V-to-1.x V) that are either magnetically isolated or nonisolated [6]-[19].

Recently, many step-down conversion solutions were introduced based on switched-capacitor converters (SCC) or constructed by inductors i.e., derivatives of buck converters. The two-stage approach is commonly applied by multiphase interleaved buck converters for the second stage, aiming to achieve a fast dynamic response and deliver a high current to consumers while reducing the output-volume filter and obtain high efficiency over wide load range, where the objective of the first-stage converter is to maintain high efficiency [6]-[12]. However, although both stages are highly efficient, the overall 48 V-to-1.x V conversion efficiency is the multiplication between efficiencies of each stage and is relatively low.

The development of GaN-based FETs enables the use of high-density single-stage conventional buck converters for the direct-conversion approach; however, multilevel buck converters remain impractical due to narrow "on" time (a duty cycle of 1/48) compounded by high switching frequencies. Other solutions consist of combinations of the buck topology with flying capacitors, offering many advantages [20]-[40]. The capabilities of an extended effective conversion ratio, multilevel multiphases, and a wider dynamic range reduce the inductor voltage swing and lower the switching loss. One of many derivations of the multiphase buck converters with extended-duty cycles—known as the series-capacitor buck converter—performs better than a buck converter and stands out as an attractive solution [21], [26]. This type of converter can produce fast dynamic responses to load changes along with the symmetrical operation and provides natural current sharing between phases while reducing the transistors' voltage stress. However, the existing topologies with extended-duty ratios may be limited for regulation in high-power applications with very high conversion ratios and high currents.

The objective of this study is to introduce a regulated modular multiphase, nonisolated topology for very high conversion ratios and high-power applications with high efficiency. The main concept is to develop the desired topology based on generic hybrid cells with optimal design guidelines that can easily meet the industry requirements for a wide use of cases and applications, where cloud computing and data centers are typical examples. This paper expands the study published in [13].

The development of hybrid generic cell as a basic building block is shown in Fig. 1. The cell includes single inductor, one capacitor and two switches that are driven in a complementary method. Multiple cells can be connected for current sharing and energy processing. This unique approach of designing with a generic cell, allow the capability of extension of any desired number of phases, with the benefits of higher duty ratio resolution, can lower the voltage stress on the transistors, and inherent current balancing, making the multi-phase topology an ideal candidate for high output current with high conversion ratio applications. The combination between cells for implement DC-DC converter with high conversion ratio will be described and analyzed in the next sections.

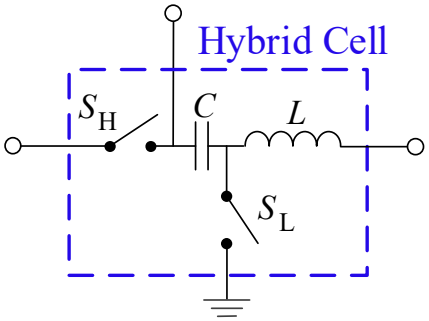


Fig. 1. Generic LC cell for hybrid modular multi-phase converter.

The rest of the paper is organized as follows. Section II presents the operation principle of three phase of series capacitor buck converter and provides typical key waveforms of the new converter. In Section III, a full steady-state analysis of the converter is delineated. Experimental results are provided in Section IV and Section V concludes the paper.

II. Multi-Phase Series Capacitor Buck Converter

Throughout the paper, the concept will be presented and analyzed on a three-phase topology, named as a triple series capacitor buck converter (TSCBC), as illustrated in Fig. 2(a). The connection between cells is by connecting all inductors output to the load stage, and by connecting the high side (voltage level) of the flying capacitor from one cell to the high side switch (S_{xH}), of the next cell. Additional switch is used to connect between high side point of the flying capacitor from the latest cell to the low side switch (S_{xL}) of the previous cell. To simplify the explanation of the circuit operation of the multi-phase topology described in Fig. 2(a), assume that the output capacitor C_o and flying capacitors C_1, C_2 and C_3 are large and the voltage ripple across them is negligible comparing to their DC voltages.

Description of the TSCBC operation is aided by the idealized timing diagram in Fig. 2(b) and the sub-circuits with their currents paths highlighted in Fig. 3. The switching period is divided into six-time intervals with six states (I–VI), where states II, IV, VI are identical and function as a "balance" state. During state I, switches S_{1H}, S_{2L} and S_{3L} are ON, [i.e., phase 1 is ON, phases 2 and 3 are OFF, see Fig. 3(a)], capacitor C_1 and inductor L_1 are charging from the input source through the load. Throughout this state, inductors L_2 and L_3 are discharged to the load, where in this stage these inductors are being connected between GND to the output capacitor C_o. In states II, IV and VI [see Fig. 3(b)], switches S_{1L}, S_{2L} and S_{3L} are ON, where all inductors are been connected to GND in one node and to the output capacitor C_o in the second node. As a result, all phases are OFF, and all inductors' currents are discharged through the load, i.e., the stored energy in the inductors delivered to the output. In state III, switches S_{1L}, S_{2H}, $S_{2\text{-}3}$ and S_{3L} are ON [phase 2 is ON, phases 1 and 3 are OFF, see Fig. 3(c)], inductor L_2 is sourced by series connection of C_1 and C_2, and by C_3, where C_1 and C_3 are discharged while C_2 is charged by C_1. During this state, inductors L_1 and L_3 are discharged to load. In state V, switches S_{1L}, S_{2L}, and S_{3H} are ON [phase 3 is ON, phases 1 and 2 are OFF, see Fig. 3(d)], results in discharged of inductors L_1 and L_2 through the load, while inductor L_3 is sourced by series connection of C_2 and C_3. In this state capacitor C_3 has been charge by C_2 through inductor L_3 and the load. Note that the charging and discharging of the capacitors are so-called soft-charged [41] or no-charged [42] and can significantly reduce the energy loss.

III. Steady State Analysis

The steady-state analysis of the TSCBC topology presented in this section is assisted by a steady-state simulation of a 40 W, 48 V-to-1 V converter, operating at 500 kHz switching frequency per-phase, and is depicted in Fig. 2(b). and Fig.4. The simulation shows the key waveforms of the TSCBC topology include inductors currents and timing diagrams for all switches.

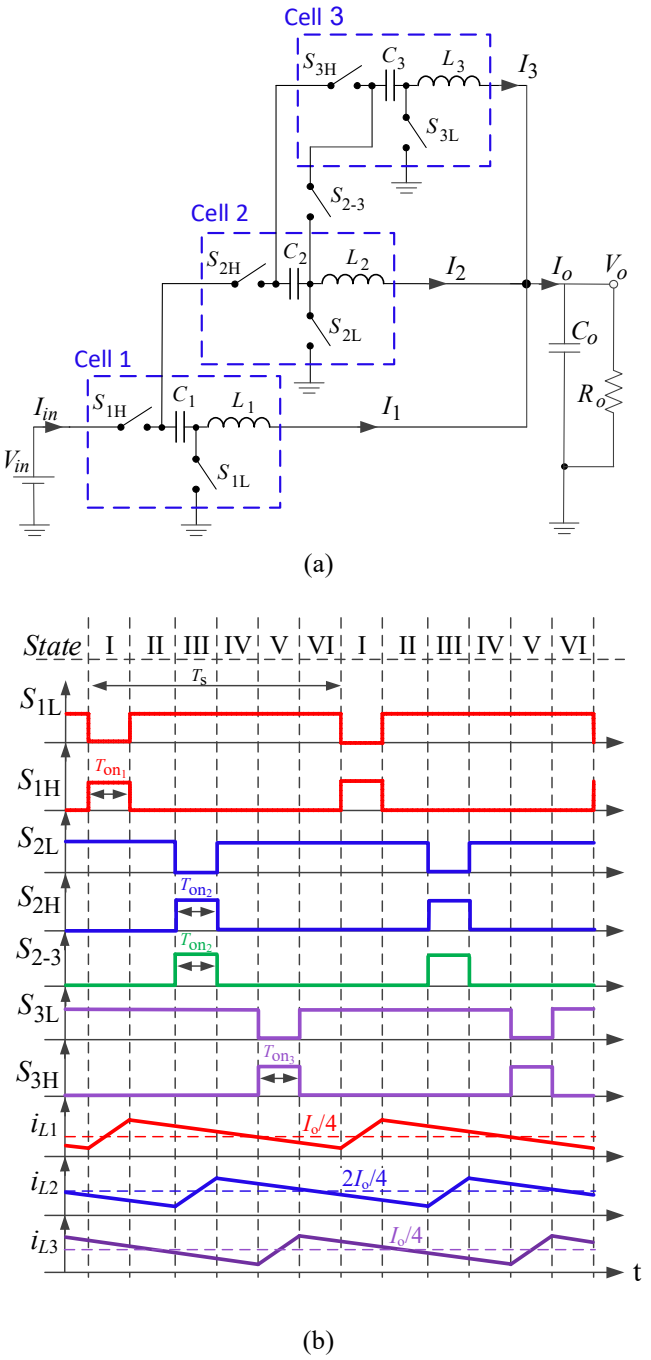


Fig. 2. (a) Circuit diagram of triple (3ph) series capacitor buck converter. (b) Timing diagram and idealized waveforms of TSCBC topology.

A. Conversion Ratio

The analysis of the TSCBC is based on the inductor-voltage second balance of each phase, i.e., inductors L_1, L_2 and L_3 and on the current-second balance of the output capacitor C_o. Following are the inductors equations from each of switching states. Due to inductor voltage second balance in the steady-state, the absolute slew rates of the inductors currents during the ON time (DT_s) is equal to the absolute slew rate during the OFF time ([1-D]·T$_s$). Hence, Δi_{L1} can be expressed as:

$$\left|\frac{-V_o}{L_1}\right|_{off} = \left|\frac{(V_{in} - V_{C1}) - V_o}{L_1}\right|_{on}, \qquad (1)$$

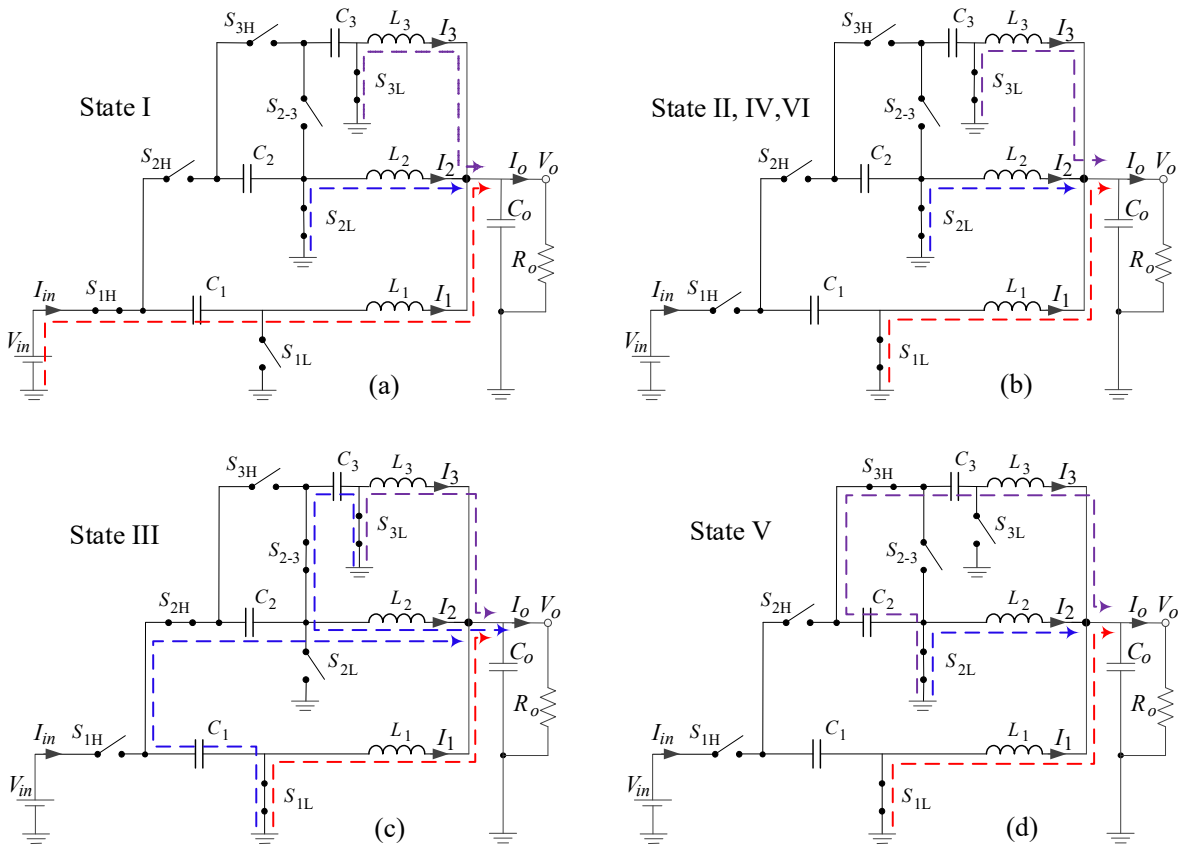


Fig. 3. Operation states I-VI. (a) State I: phase 1 is ON, and phases 2 and 3 are OFF. (b) States II, IV and V: all phases are OFF. (c) States III: phase 2 is ON, phases 1 and 3 are OFF. (d) State V: phase 3 is ON, phases 1 and 2 are OFF.

where L_1 is discharging during states II, III, IV, V and VI, and been charge at state I.

In similar manner, Δi_{L2} can be expressed as:

$$\left|\frac{-V_o}{L_2}\right|_{off} = \left|\frac{(V_{C1}-V_{C2})-V_o}{L_2}\right|_{on}, \tag{2}$$

where L_2 is discharging during states I, II, IV, V and VI, and been charge at state III.

Accordingly, Δi_{L3} can be expressed as:

$$\left|\frac{-V_o}{L_3}\right|_{off} = \left|\frac{(V_{C2}-V_{C3})-V_o}{L_3}\right|_{on}, \tag{3}$$

where L_3 is discharging during states I, II, III, IV, and VI, and been charge at state V.

The expressions Δi_{L1}, Δi_{L2} and Δi_{L3} are represent also the inductors' ripple. Note that at the ON state of phase 2, capacitor C_3 is connected in parallel to series capacitors C_1 and C_2, hence the (V_{C1} - V_{C2}) in equation (2) can be replaced by V_{C3}. From equations (1)-(3) and by replacing V_{C1} - V_{C2} with V_{C3} and some manipulation, a system of three linear equations and three unknowns can be written as:

$$\begin{cases} V_o = (V_{C2}-V_{C3})D_3 \\ V_o = V_{C3}D_2 \\ V_o = (V_{in}-V_{C1})D_1 \end{cases}, \tag{4}$$

where D_1, D_2, D_3 are the ON time for each phase respectively. Solving the system will yield to the average capacitors' voltages:

$$\begin{aligned} V_{C1} &= \left[\frac{2}{D_2}+\frac{1}{D_3}\right]V_o, \\ V_{C2} &= \left[\frac{1}{D_2}+\frac{1}{D_3}\right]V_o, \\ V_{C3} &= \frac{1}{D_2}V_o, \end{aligned} \tag{5}$$

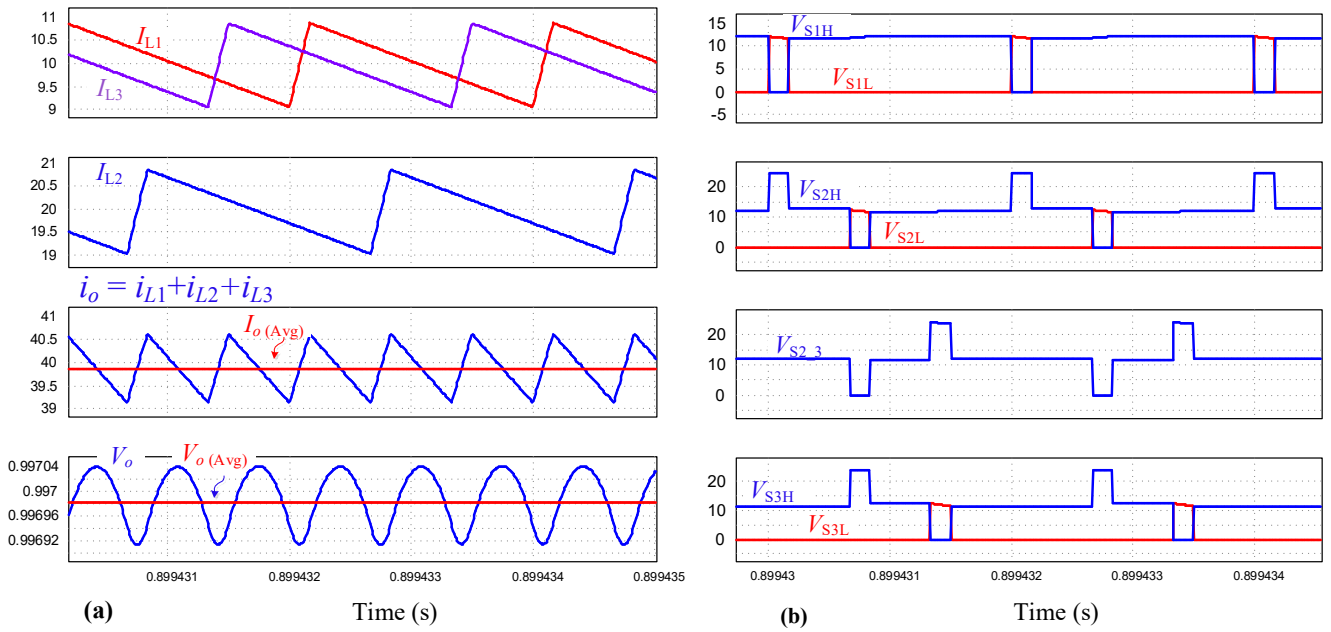
The voltage conversion ratio can be derived from (4) and (5), and can be expressed as:

$$\frac{V_o}{V_{in}} = 1\Big/\left(\frac{1}{D_3}+\frac{2}{D_2}+\frac{1}{D_1}\right). \tag{6}$$

Therefore, in the private case, where setting equal duty ratios, i.e., D_1=D_2=D_3=D, for the three phases, results in average capacitors voltages of $V_{C1} = 3V_{in}/4$, $V_{C2} = 2V_{in}/4$, and $V_{C3} = V_{in}/4$. Moreover, the expression for voltage conversion ratio is reduced to:

$$\frac{V_o}{V_{in}} = \frac{D}{4}, \tag{7}$$

which is four times higher compared to the duty ratio of a typical buck converter.



(a) **(b)**

Fig. 4. Simulation results of TSCBC single module. (a) output voltage and inductors and output currents where all duty cycles are equals, (b) The voltages across all switches: S_{1L}, S_{1H}, S_{2L}, S_{2H}, $S_{2\text{-}3}$, S_{3L}, and S_{3H}.

B. Inductors' Currents and Balancing

For simplification assume very low load at the output of the converter. The converter's output current analysis can be calculated by the output capacitor, where $i_o = C_o(dV_o/dt)$ and by the fact that at steady state, the average capacitor current is equal to zero. Due to the current second balance of the capacitor, and by the taking the absolute slew rate of the output capacitor current during charging and discharging, the following equation can be written as:

$$\left(I_{L1}+I_{L2}+I_{L3}\right)\Big|_{\text{charge}} = I_{\text{out}}\Big|_{\text{discharge}} . \tag{8}$$

The average value of each of the inductor's currents at steady state can be calculated using the fact that the charge balance is achieved for each of the capacitors [41]. For example, the charge delivered to C_2 during state III must equal the charge consumed from C_2 (by C_3) during state V. This yield to:

$$\begin{aligned} Q_{C1},\ & \frac{1}{2} I_{L_2} \frac{D_2}{f_s}\Big|_{\text{charge}} = I_{L_1} \frac{D_1}{f_s}\Big|_{\text{discharge}} , \\ Q_{C2},\ & \frac{1}{2} I_{L_2} \frac{D_2}{f_s}\Big|_{\text{charge}} = I_{L_3} \frac{D_3}{f_s}\Big|_{\text{discharge}} , \\ Q_{C3},\ & I_{L_3} \frac{D_3}{f_s}\Big|_{\text{charge}} = \frac{1}{2} I_{L_2} \frac{D_2}{f_s}\Big|_{\text{discharge}} . \end{aligned} \tag{9}$$

Solving the system using equation (8) yields the average inductors currents:

$$\begin{aligned} I_{L1} &= \frac{D_2 D_3}{D_2 D_3 + D_1 D_2 + 2 D_1 D_3} I_{\text{out}} , \\ I_{L2} &= \frac{2 D_1 D_3}{2 D_1 D_3 + D_2 D_3 + D_1 D_2} I_{\text{out}} , \\ I_{L3} &= \frac{D_1 D_2 D_3}{D_2 D_3^2 + D_1 D_2 D_3 + 2 D_1 D_3^2} I_{\text{out}} , \end{aligned} \tag{10}$$

Therefore, in the private case, setting equal duty ratios D_1=D_2=D_3=D, for the three phases, results in average inductor currents of $I_{L1} = I_{\text{out}}/4$, $I_{L2} = I_{\text{out}}/2$, and $I_{L3} = I_{\text{out}}/4$. From the equations can be seen that phase 2 is with double current compared to phases 1 and 3 caused by discharge of both capacitors C_1 and C_3 at state III, through inductor L_2. The inductors' current balance between phases can be achieved by setting the duty cycle of phase 2 to be half of the duty cycle of phases 1 and 3, where the duty ratios between phases can be written as:

$$D_2 = 2D_1 = 2D_3 \ . \tag{11}$$

IV. Simulation and Experiential Results

The verification and proof-of-concept demonstration of the design methodology is carried out by a simulation and experimental of three-phase series capacitor buck converter.

Fig. 4 shows the steady-state simulation of a 40 W, 48 V-to-1 V converter waveforms for output current of 40 A with equal duty ratios of 1/12. Fig. 4(a) demonstrate the output voltage and inductors and the sum of the inductor currents. Note that due to the three-phase interleaved operation of the converter, the effective switching frequency at the output of the converter triples, from 500 kHz to 1.5 MHz. From the results, natural current sharing between phases and with a ratio of 2:1 between I_{L2} to I_{L1} and I_{L3}. The simulation includes the $R_{DS\,(on)}$ given in Table I, so that the output voltage and current are slightly lower than expected. Fig. 4(b) shows the voltages of the switches, where the maximum stress is $2V_{\text{in}}/4$ and can be observed on S_{2H}, $S_{2\text{-}3}$ and S_{3H}.

TSCBC prototype that operates at 333 kHz switching frequency per phase was built and tested. Table I lists the components values and nominal parameters of the experimental prototype. Each phase in the converter have been designed to be symmetrical, as can be seen in Fig. 5. each hybrid cell consists of one dual switch, inductor and flying capacitor. Microchip dsPIC33 controller used to generate the complementary switches S_{xL} and S_{xH} respectively. The experiments were performed with output voltage range of 1-1.5V and maximum load of 50 A. Fig. 6, shows the three-phase inductors currents and the output current which is the sum of all three-inductors currents, (interleaved mode). The measured average capacitors voltages are as expected from the

theoretical analysis, i.e., $V_{C1} \approx 36$ V, $V_{C2} \approx 24$ V and $V_{C3} \approx 12$ V, as can be observed from Fig. 7. The efficiency from simulation compared to experimental measurement is shown in Fig. 8 with 48 V input and various output voltages. Obviously, the differences are due to other parasitic that were not included in the simulation.

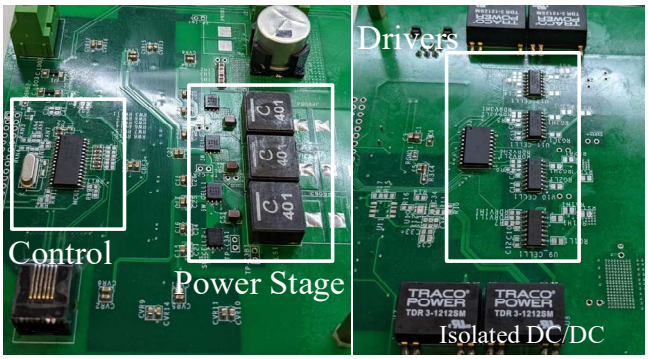
TABLE I.

EXPERIMENTAL PROTOTYPE PARAMETERS

	Power Stage	
Component	**P/N**	**Value/Type**
Input Voltage - V_{in}		48 V
Output voltage range - V_{out}		1 - 1.5V
Switching frequency - f_{sw}		333 kHz per phase
Input capacitor - C_{in}	EEE-FK2A221AV	220 µF, 100 V
Output capacitor - C_{out}	EEF-GX0D561R	560 µF, 2 V
Inductors - L_1, L_2, L_3	XAL1580_401MEB	0.4 µH, 60 A
Capacitors - C_1, C_2, C_3	CNA6P1X7R2A475K250AE	4.7 µF, 100 V
MOSFETs ($R_{DS\,on}$)	Vishay 2Ch, SIRB40DP	3.25 mΩ, 40 A, Dual
Load resistance - R_{load}		20-100mΩ
	Floating Driver	
Driver	2EDF7275F	
Isolated DC/DC	TDR 3-1212SM	
	Digital Section	
Microcontroller	dsPIC33FJ16GS502	16 bit, 40 MIPS
Buffers & Line Drivers	MC74VHC244DWR2G	

V. CONCLUSIONS

A modular hybrid topology has been demonstrated. It is based on the developments described in this paper. It comprises multiple phases for high current delivery and uses series capacitors operated in a soft charging mode. The introduction of series capacitors and their operation in a soft charging mode, significantly lowers the voltage stress of the transistors, highly extends the duty ratio, and provides an inherent current sharing between the phases.



(a) (b)

Fig. 5. Prototype PCB (a) top view of the power stage that include microcontroller, one dual MOSFETs per cell, power inductors and flying capacitors. (b) bottom view that include buffer, drivers, and isolated DC/DC supplies.

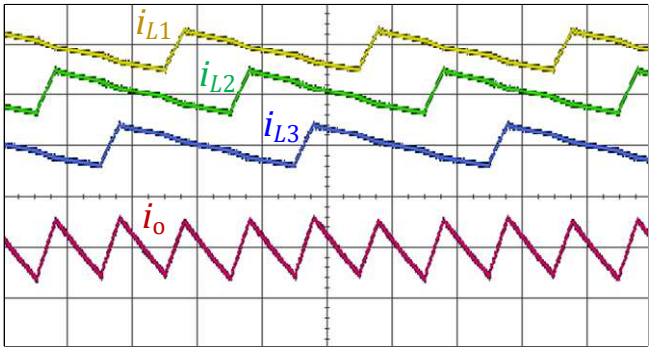


Fig. 6. Inductors' current waveforms: yellow - I_{L1}, green - I_{L2}, blue - I_{L3}, and red - output current. Phases are interleaved by 120 degrees.

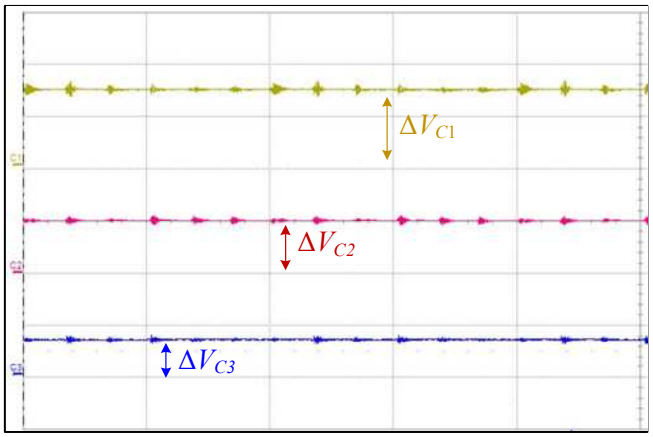


Fig. 7. Capacitors DC level measurements, yellow - V_{C1}, red - V_{C2}, blue - V_{C3}, all channels are 22 V/div.

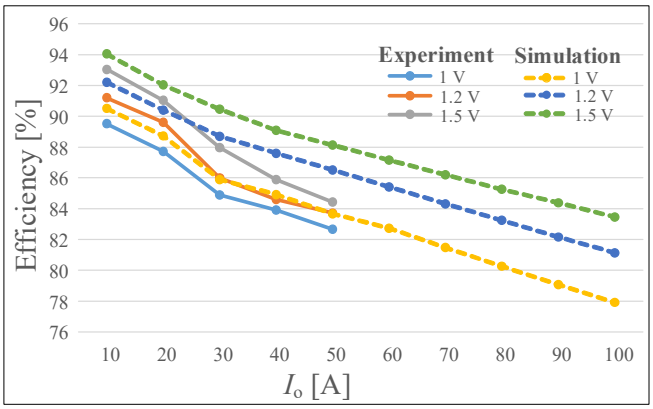


Fig. 8. Efficiency measured by simulation vs experiment for different output voltages. Simulation include the ESR of all components in the power stage.

These properties reduce the VRM's volume and potentially can increase the efficiency in direct-conversion of 48 V-to-1.x V, that is common and highly desired in data centers and other cutting-edge applications. Initial experimental study of an interleaved three-phase modular prototype demonstrates the behavior, which is in an excellent agreement with simulation and theoretical analysis.

The new design methodology where identical hybrid cells, comprised of both inductor and capacitor, are used to construct an *n*-stage converter, which can be used effectively for variety of applications, is demonstrated. This technique significantly reduces the complexity of design and implementation of switched-mode power converters for multiple use cases. Any conversion ratio can be achieved seamlessly and efficiently, using only identical cells, or modules and with well-defined design guidelines. This ultimately establishes the enabling technology for reliable, fast and power-oriented design of high conversion ratio power-converters, as a new baseline in the field.

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