Carrier Based Pulse Width Modulation for Low Distortion Sinewave Generation using Hybrid Harmonics Elimination Method

Ron Vaizman, *Student Member* Bar Halivni, *Student Member* and Mor Mordechai Peretz, *Member, IEEE*
The Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev, P.O. Box 653, Beer-Sheva, 8410501 Israel
ronvaiz@post.bgu.ac.il, morp@ee.bgu.ac.il
http://www.ee.bgu.ac.il/~pemic

2023 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-6654-7539-6/23/$31.00 ©2023 IEEE | DOI: 10.1109/APEC43580.2023.10131346

***Abstract*— this paper introduces a hybrid harmonic elimination carrier-based pulse width modulation (HECBPWM) method for sinewave generation. The harmonic elimination algorithm is validated via an FPGA based digital controller and a three-phase multilevel inverter experimental prototype. The harmonic elimination algorithm generates the inverter PWM signals to eliminate unwanted harmonics of the output voltage waveform. The HECBPWM utilize continues duty cycle trajectories as a function of the desired modulation index for the PWM generation. The duty cycle functions reduce computing power requirements by using asynchronous calculation procedure and pre-calculated coefficients. The adaptation of algorithm for full-bridge single phase inverter and a three-level NPC single-phase inverter is detailed and demonstrated experimentally. The experimental prototype operation with an inductive load is shown along with the cancelation of multiple unwanted harmonics at the output voltage.**

Keywords – NPC, Harmonic distortion, Harmonic Elimination.

I. INTRODUCTION

With the proliferation of electric vehicles (EVs), electrical motor drive and control became a major interest of EV manufacturers. It has been approximated by the year of 2040 the majority of sold cars are electric [1], therefore improving motor-drive capabilities result in significant reduction of greenhouse gasses and improving. EVs are not producing greenhouse gasses during their operation, however the charging phase utilizes electric grid power. The power drawn from the grid produces greenhouse gasses in a much lower scale than a typical combustion engine operation for the same power rating [2]. The main concern of EV manufacturers is to extend the EV battery life, this is achieved by upgrading the battery management system [3-5] or improving the EV motor power train. The motor power train of a typical EV comprises energy storage, an inverter stage for DC to AC power conversion and a motor. The reduction of the inverter stage losses is carried out by using more efficient wide bandgap switching devices such as GaN or SiC [6-9]. Another approach to improve the inverter efficiency by implementing enhanced methods for sinewave generation [10-12].

The concept of selective harmonic elimination (SHE) was introduced back at the previous century [13-15]. Since then SHE has drawn a lot of attention due to the ability of controlling the harmonic content of a switching sequence. SHE allows to achieve an optimal switching sequence in terms of switching action count per harmonic distortion obtained at the output current. The implementation of SHE minimizes harmonic losses, reduces the switching losses, and is suitable for low-frequency applications [16-18]. Successful realization of the SHE equations requires a large computing effort and usually handled off-line, outside of the controller real-time tasks. A common implementation of the SHE equation results are memory demanding look-up tables (LUTs) [19-22]. The shift between one LUT to another is carried out by interpolation, which complicates the utilization of SHE where dynamic response is required [23-24]. Accurate solution of the SHE equations using a numerical solver is highly complicated where higher order equations are introduced. [25].

In single-phase applications the predominant modulation strategy is using sinusoidal pulse width modulation (SPWM) [26-29]. The SPWM method handles the unwanted harmonics by pushing the harmonic content towards the carrier frequency harmonic. The remaining harmonic content at the carrier frequency can be filtered using smaller passive components due to its high frequency nature. SPWM is very flexible in terms of switching sequence PWM generation, and can generate a switching sequence for any type of DC to AC conversion.

Multilevel inverters are highly popular in high voltage applications [30-33]. Multilevel inverters minimize the amplitudes of the unwanted harmonics and reduce the switching losses. Multilevel inverter topologies can be categorized to three basic topologies: cascaded h-bridge (CHB) [34-35], flying capacitor (FLC) [36-37] and neutral point clamped (NPC) [38-39]. Despite CHB multilevel inverters are good candidates in terms of simplicity, this type of inverters requires additional input voltage sources which

complicates the implementation of such inverters. The trade-off of using FLC and NPC inverters is the natural capacitor balancing issues [40-41], which requires very fast dynamic response and rule-out modulation strategies such as SHE.

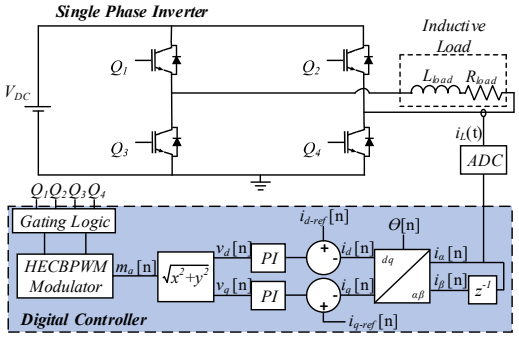


Fig. 1. Simplified schematic diagram of an inverter with field oriented controller and the dedicated hybrid harmonic elimination block.

The objective of this study is to introduce a new switching method employing a Hybrid Harmonic Elimination Carrier Based Pulse Width Modulation. The new method achieves superior performance in terms of generated sinewave distortion for given switching actions count of a single sinewave base frequency period. The HECBPWM is implemented in a digital controller platform using asynchronous calculation methodologies to reduce the computational efforts. A further objective of this paper is to examine the implementation of HECBPWM on a single-phase NPC multilevel inverter. The full inverter platform is shown in Fig. 1 including a single-phase inverter and a digital controller to deliver field-oriented control and the HECBPWM switching method.

The rest of the paper is organized as follows (some parts have been omitted to the brevity of the digest and will be provided in the final version of the paper), Section II describes in detail the hybrid harmonic elimination methodology and its principle of operation. The implementation aspects of the introduced HECBPWM is thoroughly described in Section III, which also includes a detailed discussion on single-phase NPC multilevel inverter implementation. Section IV details a simulation case study of the hybrid harmonics elimination method and is followed by experimental validation on a single-phase NPC multilevel inverter platform in Section V. Section VI concludes the paper.

II. Harmonic Elimination Methodology

In sinewave generation converters, PWM gate driving is typically generated by using an on-line method such a CBPWM, traditionally the PWM signal is generated by comparing a high frequency carrier triangular wave with the desired reference signal shape. A demonstration of the CBPWM for a sinewave reference signal is shown in Fig. 2(a), the resultant modulation signal is generated by comparing a sinewave to a carrier wave. The carrier wave frequency determines the switching frequency of the gate drivers, and the sinewave determines the base frequency of the first harmonic. The amplitudes ratio of the sinewave and the carrier wave is defined as the modulation index. By using the CBPWM method, unwanted harmonics are pushed away towards the carrier frequency, resulting low harmonic distortion.

Another method for sine generation is angle based pulse width modulation, where the calculation of the pulse edges timings can be determined prior to the system operation. The pulse edges timings are stored in look-up tables for rapid accesses of the controller during system operation. By emulating a motor rotating frame, the pre-calculated edges are put together and a sinewave generation PWM is generated as show in Fig. 2(b). Angle based pulse width modulation can achieve an optimal sinewave PWM signal in terms of switching count versus signal distortion is obtained.

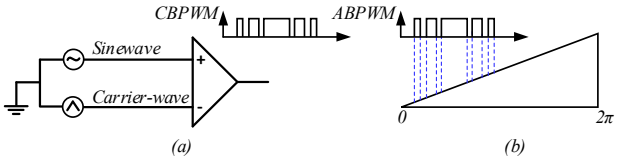


Fig. 2. Sinewave PWM generation methods, (a) typical carrier-based pulse width modulation implementation, (b) typical angle-based pulse width modulation implementation.

For the simplicity of implementation, a case of unipolar voltage waveform is examined for a single-phase full bridge inverter as shown in Fig.3. The single-phase full bridge (FB) inverter comprises of two half-bridge branches, each branch transistors are working in a complementary manner. Typical loads of the single-phase FB inverter are motors, grid, and even audio application. Such loads are typically inductive in nature, therefore, can be emulated via an inductor-resistor pair as shown in Fig.3.

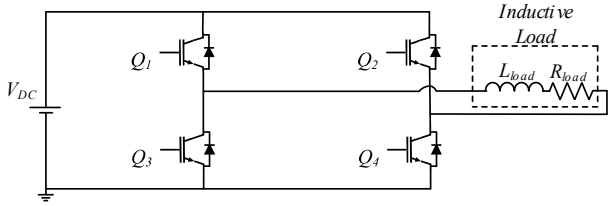


Fig. 3. Single phase full bridge inverter with an inductive load emulator.

Modulators for sinewave generation create a PWM pattern as a function of the modulation index. The modulation index defined as the ratio of the resultant sinewave first harmonic amplitude V1 and the DC source voltage VDC. By controlling the modulation index the intensity of the first harmonic can be governed. To maintain the desired first harmonic amplitude the modulation index is adjusted to compensate for load changes, as can be seen in a field-oriented control loop of Fig. 1. In order to fit within traditional control loops, the HECBPWM receives a modulation index value and generates a pulse pattern with respect to the current state of the load. The conceptual block diagram of HECBPWM is depicted in Fig. 4, and comprises of a duty cycle calculation block, which is the core of the

HECBPWM method. The duty cycle calculation block receives the modulation index and generate the appropriate duty cycle commands. The multiplexing stage along with the gating logic block completes HECBPWM operation. The multiplexing stage translates the duty cycle commands to the desired PWM modulation signal, and the gating logic is responsible for delivering the PWM signals to the appropriate corresponding transistors. In addition, the gating logic generates the complementary PWM signals for each transistor pair and adds dead-time to protect the system by preventing possible shoot-through events.

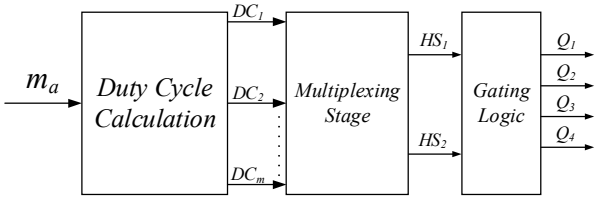


Fig. 4. Conceptual block diagram of HECBPWM.

The following section thoroughly describes the HECBPWM calculation block duty cycle generating method. The mathematical expressions provided are suitable for the generalized case where, m numbers of duty cycle calculation are required. The first stage of generating the duty cycle commands is describing the output voltage waveform. Fig. 5 demonstrate a unipolar voltage waveform of a single-phase full bridge inverter. The HECBPWM divides each quarter of the reference signal period into m sections, each section duty cycle is determined by the duty cycle calculation block outputs. The selection of m is determined by number of the unwanted odd harmonics to be eliminated in addition to the fundamental harmonic, e.g. if the requirement is eliminating the 7th harmonic, then the number of left edges is 4.

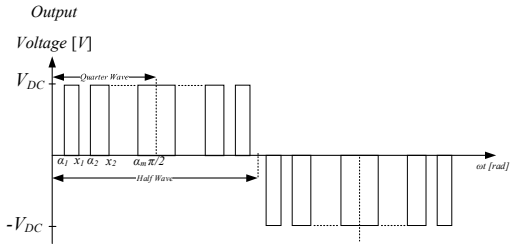


Fig. 5. Unipolar voltage waveform of a single-phase full bridge inverter.

As can be seen in Fig. 5 each section (x_{n+1}-x_n) is divided into two complementary angle intervals, the on-time interval is determined by x_n-α_n, the rest of the section is defined as the off-time interval. The angle of x_n is function of m and can be referred as a stopping point of the on-time interval. The voltage waveform pulses count per a full reference signal period is given by 2m-1. Due to the half and quarter wave symmetry, the voltage waveform does not contain a DC or even harmonics. This allows to determine the voltage expression for a quarter wave period and the only harmonic content is located in the odd harmonics. The Fourier integral coefficients of the voltage expression can be shown as:

$$b_n = \frac{4}{\pi}\left[\int_{\alpha_1}^{x_1} V_{DC}\sin(n\omega t)d(\omega t) + \int_{\alpha_2}^{x_2} V_{DC}\sin(n\omega t)d(\omega t) \ldots + \int_{\alpha_m}^{\frac{\pi}{2}} V_{DC}\sin(n\omega t)d(\omega t)\right] \quad (1)$$

The expression in (1) can be written as a series of trigonometric components as follows:

$$b_n = \frac{4V_{DC}}{n\pi}\sum_{k=1}^{m}\cos(\alpha_k n) - \cos\left(\frac{\pi k}{2m}\right), \quad (2)$$

Where n is the harmonic number, and k is series running index. In the case where m edges are chosen, the solution of such system with order of m, require m coefficient equations. The equations of (3) and (4) shows the system coefficient equations and the solution vector respectively. The solution vector is constructed in order to eliminate the odd harmonics and to maintain the first harmonic amplitude. This dictates that the first harmonic has a value as a function of the modulation index, and the rest of the other terms are zero.

$$f = \begin{bmatrix} \sum_{k=1}^{m}\cos(\alpha_k) - \cos\left(\frac{\pi k}{2m}\right) \\ \sum_{k=1}^{m}\cos(3\alpha_k) - \cos\left(3\frac{\pi k}{2m}\right) \\ . \\ . \\ . \\ \sum_{k=1}^{m}\cos(n\alpha_k) - \cos\left(n\frac{\pi k}{2m}\right) \rightarrow (n = odd, n \neq 1) \end{bmatrix}; \quad (3)$$

$$T = \begin{bmatrix} \frac{m_a\pi}{4} \\ 0 \\ . \\ . \\ . \\ 0 \end{bmatrix}. \quad (4)$$

The system described by (3) and (4) cannot be solved analytically and must be solved using a numeric solver. The most suitable solver for these types of applications is the Newton-Raphson numeric solver. The numeric solvers accuracy is highly impactful to the HECBPWM ability to eliminate the undesired harmonics. The Newton-Raphson iterative solver is suitable for this application in terms of accuracy, however, usually the main problem of employing such algorithm is the initial guess of the solution. The initial guess could lead the solver to divergence, this can be avoided by a methodical selection of initial values. In the HECBPWM algorithm, the initial guessed values are the stopping point of every pulse x_n. The usage of the pulses stopping points as the solver initial guesses, extensively reduce the solving efforts of the Newton-Raphson iterative solver for high order systems. In order to solve the system of equations by the numeric solver, the system of equation derivative has to be described as well as shown in (5).

$$\frac{df}{d\alpha}=\begin{bmatrix}\sum_{k=1}^{m}-\sin(\alpha_k)\\ \sum_{k=1}^{m}-3\sin(3\alpha_k)\\ .\\ .\\ .\\ \sum_{k=1}^{m}-n\sin(n\alpha_k)\rightarrow(n=odd,n\neq 1)\end{bmatrix}. \quad (5)$$

The results of the system of equations solution for different modulation indices from 0 to 1 construct the angle trajectories. Fig. 6 demonstrate the angle trajectories for the case where $m=3$, at this case the 3rd and the 5th harmonics are eliminated. As can be seen from Fig. 6 each of the angle trajectory is confined within equal section of the quarter period of the reference signal, in this example the angle limits in 30°. The angle trajectories are converted to on-time interval pulse duration. The duty cycle command for each section is given by (6). Where m is the number of the angle trajectories, α is the trajectory value, and k is trajectory number that changes from 1 to m.

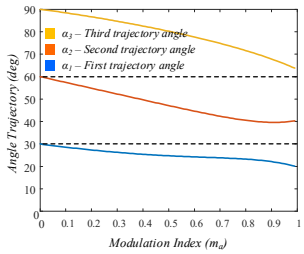


Fig. 6. Angle trajectories as a function of m_a from 0 to 1 for $m=3$.

$$DC_k=\frac{\frac{\pi}{2mk}-\alpha_k}{\frac{\pi}{2m}}. \quad (6)$$

The translation of the angle trajectories into duty cycle trajectories is performed via (6) and the resultant trajectories are presented in Fig. 7 .The duty cycle trajectories represent the duty cycle of each section as a function of the modulation index that result harmonic elimination at any value of m_a. Fig. 7 shows the duty cycle trajectories for the case where $m=3$ and this can be further elaborated to higher order of m while avoiding the hurdle of substituting the first initial guess for every angle trajectory.

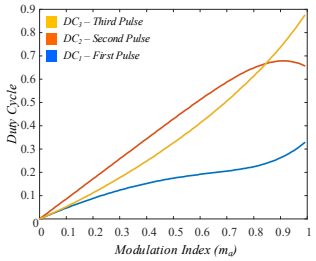


Fig. 7. Duty-cycle trajectories as a function of m_a for m=3.

The traditional of implementation harmonic cancellation methods are carried out by lookup tables and angle-based modulation. The usage of lookup tables in high resolution operation require high volume of the controller memory and are less suitable for applications where continues information of the duty cycle is required. The HECBPWM algorithm can be implemented without using lookup table, thus, saving memory space and provide a continue information of the duty cycle. The trajectories of Fig. 7 are interpolated as a polynomial expression as a function of the modulation index. The expression of the duty cycle trajectories as polynomials enables real-time duty cycle calculations for any given modulation index. Each pulse has its own polynomial expression which can be solved by the controller to obtain the duty cycle command dynamically. In comparison to simulation results obtained via PSIM, a good approximation of the duty cycle trajectories is achieved with polynomials with order of four or higher. The basic fitting can be carried out in high-level languages such as MATLAB and the resultant fitting equation is given as:

$$DC_x=a\cdot m_a^4+b\cdot m_a^3+c\cdot m_a^2+d\cdot m_a^1+e\cdot m_a^0. \quad (7)$$

Duty cycle trajectories polynomials results can be compared with a carrier wave to generate the required PWM patterns. A further discussion on the implementation of the HECBPWM algorithm is described in the following section.

III. Practical Implementation

The HECBPWM algorithm introduced in previous section produce the duty cycle equations and thereby enables the calculation of the duty cycle commands for harmonic cancelation in real-time. This section provides a comprehensive review of the practical implementation aspects and realization challenges of HECBPWM algorithm. The HECBPWM modulator is constructed of three stages as can be shown in Fig. 4. The first stage is the duty cycle functions and the second stage is the multiplexing stage which is the sorting system to acquire the desired sequence. The third stage is gating logic which is responsible for the generation of the transistors gating signals, handling complementary signal generation and prevents possible shoot-through.

Fig.8 shows the multiplexing stage conceptual block diagram and its key components. The system contains trailing-edge (blue) and leading-edge (red) sawtooth generators, and a set of comparators to compare the duty cycle functions outputs with the carrier signals. The comparators outputs are fed to the trailing-edge (blue) and leading-edge (red) sequence multiplexer. The quarter wave multiplexer (green) receives the set of sequences from the previous multiplexing components to combine them as a repetitive switching sequence. The demultiplexer shown in purple direct the generated gating signal to each of the full-bridge branches with the assistant of the gating logic module.

The next stage in the multiplexing stage is sorting the pulses generated by the comparing stage in the correct order. Trailing-edge pulses sequence is relayed to the output and

followed by the leading-edge pulses sequence. The identification of each quarter wave and the appropriate edge type is performed by the quarter wave detection register. The quarter wave register is used by the multiplexer block (Fig. 8) to sort and align the pulses of the trailing-edge and leading-edge sequences in the desired order to the next demultiplexing stage. The half wave detection is responsible for the unipolar wave generation for every high side switch HS_1 and HS_2 by controlling the demultiplexing stage, as can be shown in Fig. 8. Following this procedure result in a HECBPWM unipolar switching sequence which is passed to the full bridge transistors by the gating logic block.

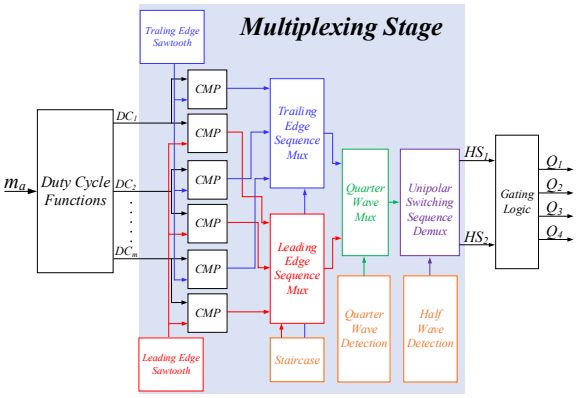


Fig. 8. Multiplexing Stage conceptual block diagram.

In this work the PWM signal is generated via a straightforward clock based PWM generator. The digital implementation of the PWM generators introduce rounding errors due to the usage of integers in order to reduce the computational resources. PWM generator non-idealities result in odd harmonics within the output signal. This can be solved by increasing the digital controller clock frequency to obtain higher resolution of the carrier signal, which result in an increased PWM resolution. The frequency of the sawtooth generators can be calculated by the following expression:

$$f_{\text{Sawtooth}} = f_{\text{Base}} \cdot 4 \cdot m \,. \tag{8}$$

Where f_{Base} is the base harmonic frequency, and m is the number of the duty-cycle trajectories. In a closed loop form of a field-oriented control the base frequency f_{Base} value is derived from the motor speed.

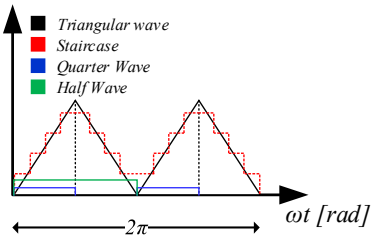


Fig. 9. Multiplexers select generation, for the case of $m=4$.

Fig. 9 shows the division of the reference signal period into half-wave, quarter wave and the quarter wave sections of the HECBPWM algorithm. The double edge sawtooth in Fig. 9 is divided into a staircase signal responsible for the correct order of the pulse generation that arrives from the comparing stage according to Fig 8. The sequence of pulses is sorted by increasing order until it reaches the maximal stair and then by decreasing order and is repeated continuously.

The demonstration of the HECBPWM algorithm operation on a multilevel inverter is performed using a single-phase NPC multilevel inverter case study. Fig. 10 shows the single-phase NPC multilevel inverter which comprises of four transistors at each branch and two clamping diodes. Multilevel inverters are capable of improving harmonic distortion and reducing switching losses. Due to the multilevel nature of the converter the voltage stress at each transistor is reduced in comparison to the traditional full bridge configuration.

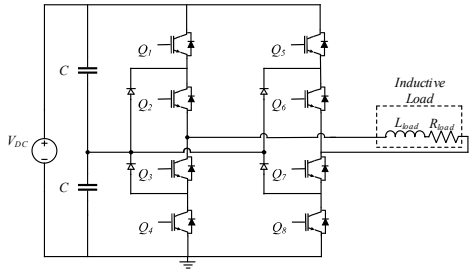


Fig. 10. Single phase three-level NPC multilevel inverter.

The bus capacitors C (Fig. 10) works as a voltage divider to produce additional voltage levels. For the case of three-level inverters as can be seen in Fig. 10, the operating modes of the NPC multilevel inverter are shown in Fig. 11. Fig. 11(a) demonstrate a zero voltage at the output where Fig. 11(b) provides half of the DC bus to the load and in Fig. 11(c) the entire DC bus voltage is delivered to the inverter output. Increasing the multilevel level count is beneficial by reducing the output signal THD. The unwanted harmonics in this case of multilevel inverters are significantly lower than the case of the full-bridge inverter. The HECBPWM implementation for multilevel inverters can be done by minor adaptation of unipolar block by adding another switching sequence to the system.

Although harmonic distortion improvement is obtained by implementing a multilevel inverter, the multilevel nature of the converter introduces additional control challenges to the system. The main issue is capacitor balancing which is typical for multilevel inverters. In the ideal case the capacitor voltage is equal half of the DC bus voltage, however, in practice it is not the case as current is being drawn from the capacitor is unneglectable, and causes the voltage across the bus capacitors to oscillate. In this work, the voltage level at each capacitor is assumed to be constant and does not oscillate in order to demonstrate the HECBPWM implementation.

During a half reference signal period four switches operate to generate the multilevel unipolar voltage waveform, the four switches which take part for the first half of the reference signal switching period are Q_1, Q_2, Q_7 and Q_8. If the switching sequence of each transistor pair is identical (Q_1, Q_8 or Q_2, Q_7), the multilevel inverter operates

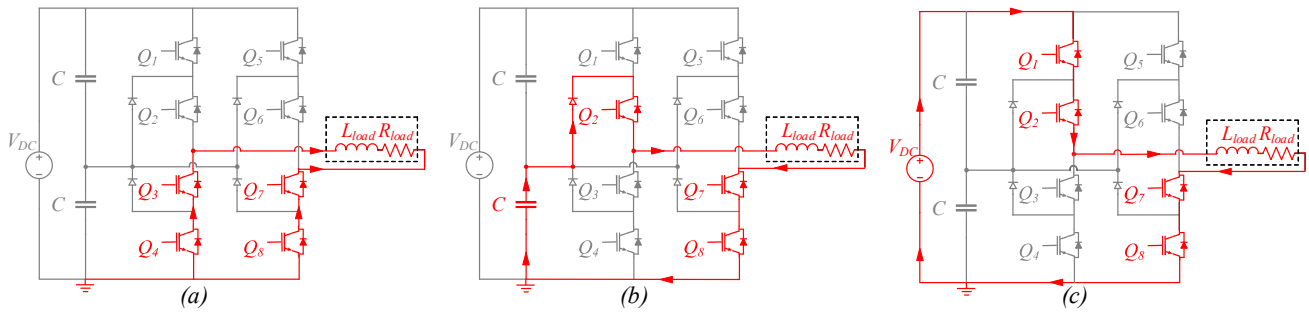


Fig. 11. Multilevel voltage configurations, (a) imposing zero voltage, (b) imposing $V_{DC}/2$, (c) imposing V_{DC}.

like a typical full bridge inverter and the generated output voltage waveform is identical to the non-multilevel case. At this type of operation, the clamping diodes and the bus capacitors are not used but the stress across the transistors does not change.

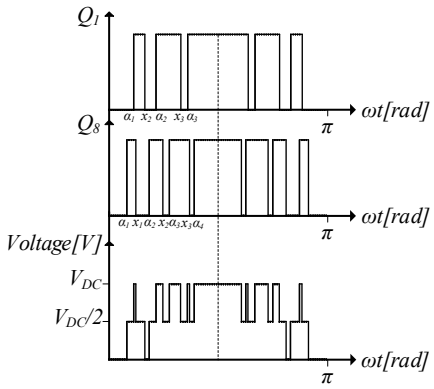


Fig. 12. Three level multilevel inverter switching sequence for Q_1 and Q_8, $m=3$.

The multilevel inverter PWM signals for the three-level inverter are obtained by super-position of different switching sequences sets of HECBPWM. Fig. 12 shows the PWM signals of Q_1 and Q_8 to demonstrate a three-level output voltage generation. Assuming Q_1 receives a switching sequence of m, and Q_8 receives a switching sequence of $m+1$, the two switching sequences have shared properties of eliminating the first $m-1$ odd harmonics beyond the fundamental harmonic. These overlap properties determine the resultant output voltage waveform (Fig. 12).

The switching sequence of Q_1 (Fig. 12) has a pulse count of $2m-1$, while the pulse count of Q_8 is $2(m+1)-1$, their overlap properties are eliminating the 3rd and the 5th harmonics. Although Q_8 switching sequence has the ability to eliminate the 7th harmonic, only the sherd harmonic elimination properties decide the harmonic content of the output voltage waveform. Different combination of gating signals sequences can be selected, however, the selection of m and $m+1$ provide the best results in terms of pulse count and harmonic distortion reduction.

The full HECBPWM modulator implementation for single-phase three-level inverter is depicted in Fig. 13 The HECBPWM multilevel modulator adds another multiplexing stage for the control of additional transistors and the duty cycle functions comprise of another set of polynomials. The upper duty cycle functions block contains functions for the case of m and the bottom block handles the case of $m-1$. The staircase blocks at the top at bottom are adapted for case of m and $m-1$ respectively. The multiplexing and the demultiplexing stage operate from a shared quarter wave and half wave detectors. The generated signals are delivered to the gating logic to generate another switching sequences for the appropriate transistors of the multilevel inverter. The generated getting signals are operated in a complementary manner where the transistor pairs are Q_3-Q_1, Q_7-Q_5, Q_6-Q_8, and Q_2-Q_4.

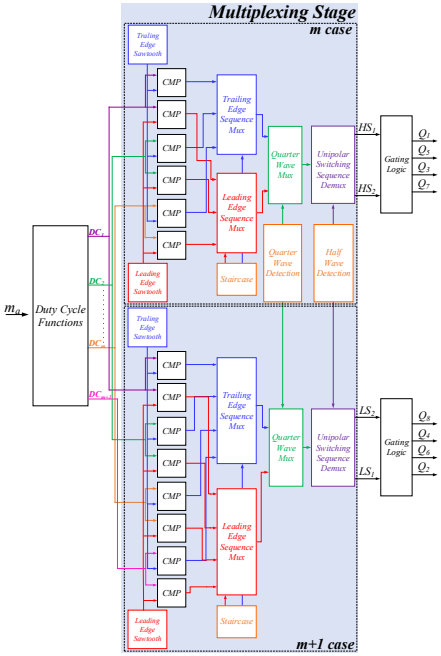


Fig. 13. HECBPWM modulator for single-phase three-level inverter.

IV. Simulation Verification

Using the analysis and observations from previous sections, a set of simulation have been conducted in PSIM (PowerSim, Inc.) to verify the effectiveness of the new HECBPWM modulator procedure in an open loop operation of a full-bridge inverter and an NPC multilevel single-phase

inverter. The inverter parameters are presented at Table I. In order to verify the harmonic cancellation capabilities of the HECBPWM various cases of m are examined. The simulations are demonstrating the ideal case where dead-time is neglectable, capacitors are constantly balanced, and transistors are ideal. In addition, for harmonic elimination of the unwanted harmonics as described in section II, the HECBPWM also push the residual unwanted harmonic content toward the carrier frequency as occurs at carrier-based switching methods.

TABLE I – SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	*Symbol*	*Value*
Input voltage	V_{DC}	75V
Base Frequency	f_{Base}	50Hz
Inductor	L	5.8mH
Load Resistance	R	14.5Ω
Modulation index	m_a	0.95

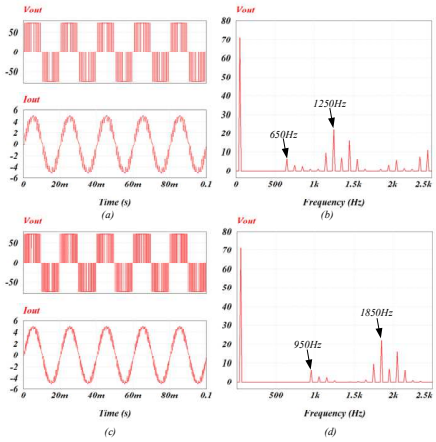


Fig. 14. Full-bridge single-phase inverter, (a) Output voltage (top) and output current (bottom) for $m=6$. (b) Output voltage harmonic content for $m=6$. (c) Output voltage (top) and output current (bottom) for $m=9$. (d) Output voltage harmonic content for $m=9$.

In Fig. 14 the HECBPWM method is implemented for a full-bridge single-phase inverter. Fig. 14(a) shows the output voltage (top) and output current (bottom), Fig. 14(b) display the harmonic content of the output voltage via FFT. For the case where $m=6$ the first visible harmonic is located at 650Hz, which is the 13th harmonic. This exhibit the elimination of $m-1$ harmonics and the resultant output voltage harmonic content does not contain the odd harmonics from the 3rd to the 11th. Since no even harmonics are present as an axiom for solving the system of equations, the highest harmonic content is located at 1250Hz which is the trailing-edge and leading-edge generators carrier frequency. The generated harmonics between the first visible harmonic up to the carrier harmonic are fairly small in comparison to the carrier generated harmonics. The first harmonic amplitude is 71.25V according to the selected modulation index value. In a similar manner, Fig. 14(d) demonstrate the inverter operation for the case where $m=9$. The first visible harmonic content located at 950Hz which is the 9th harmonic and the highest harmonic present within the output signal is located at the frequency of the carrier generators harmonics at 1850Hz.

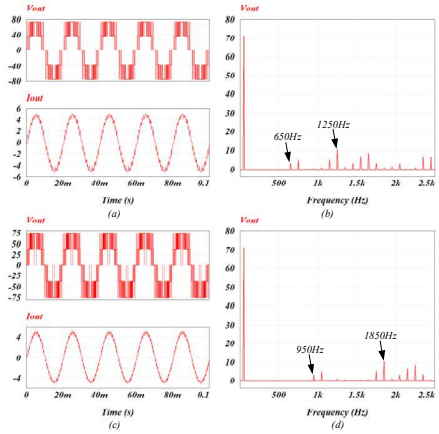


Fig. 15. Three-level NPC single-phase inverter, (a) Output voltage (top) and output current (bottom) for $m=6$. (b) Output voltage harmonic content for $m=6$. (c) Output voltage (top) and output current (bottom) for $m=9$. (d) Output voltage harmonic content for $m=9$.

In Fig. 15 the HECBPWM method is carried out for a three-level single-phase inverter. Fig. 15(a) shows the output voltage (top) and current (bottom) waveforms and Fig. 15(b) present the harmonic content of the output voltage via FFT. For the case where $m=6$, The first visible harmonic is located at 650Hz, the unwanted harmonics amplitudes are fairly small in comparison to the full-bridge case due to the multilevel operation of the inverter. The highest amplitude is obtained at 1250Hz, this result resembles to the full-bridge case. In Fig. 15(c) the output voltage (top) and current (bottom) are presented for the case where $m=9$. The first visible harmonic is located at 950Hz and the highest harmonic content is located at 1850Hz. As can be seen from Fig. 14 and Fig. 15 the resultant output voltage harmonic content behavior is with good agreement to the introduced HECBPWM algorithm of section II.

V. EXPERIMENTAL RESULTS

In order to experimentally validate the HECBPWM algorithm operation, a multilevel three-phase inverter has been designed and built. The algorithm implementation has been demonstrated for single phase three-level inverter and full bridge inverter, and the digital controller is implemented using an Altera Cyclone V FPGA. The parameters of the system are summarized in Table I. The three-level three-phase NPC inverter experimental prototype is shown Fig. 16, each inverter phase comprises of four IGBT transistors, two clamping diodes and a capacitor bank. The realization of the inverter utilizes two inverter phases, each phase represents a half-bridge branch. The examination of the full-bridge single-phase inverter require the operation of phase transistors in pairs.

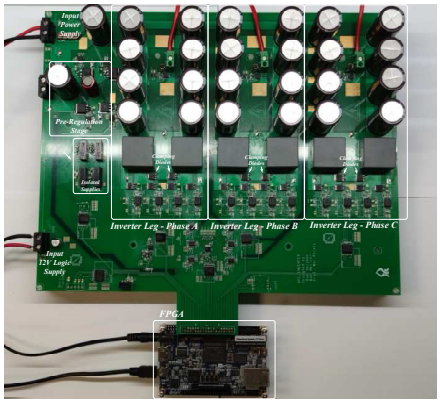
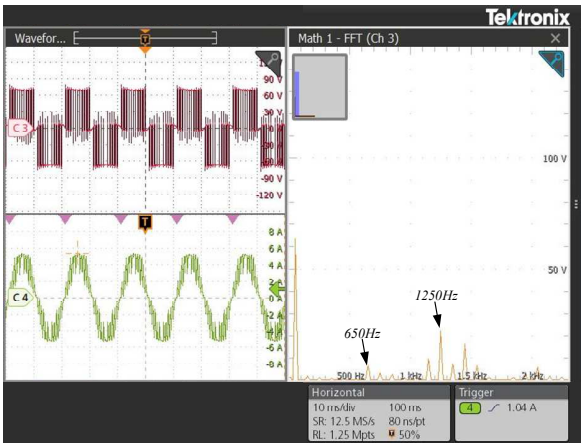
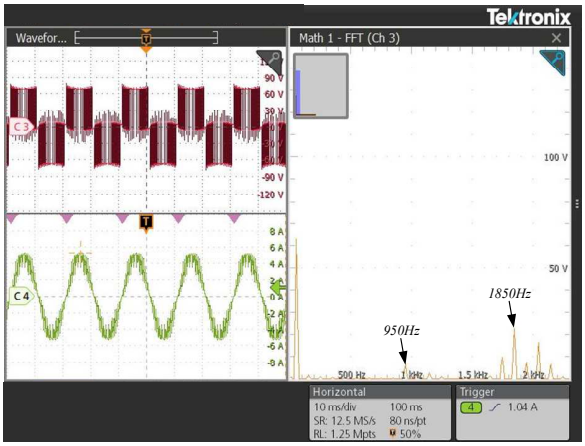


Fig. 16. Prototype board, including full-bridge and three-level NPC inverters.



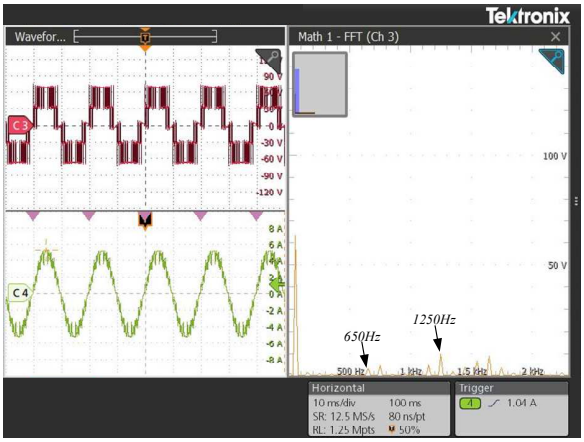
(a)



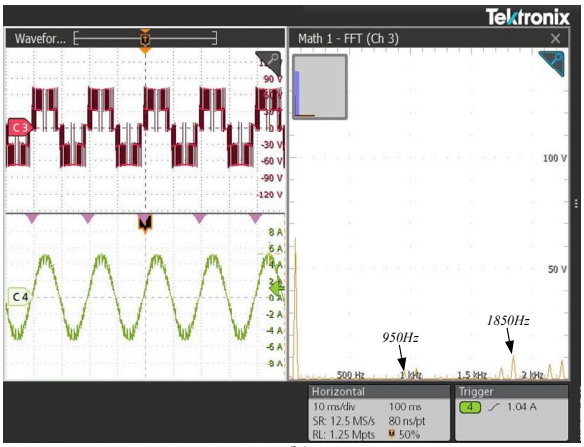
(b)

Fig. 17. Full-bridge single phase inverter waveforms with HECBPWM harmonic cancelation method (a) $m=6$. (b) $m=9$. v_{out} (red) 30V/div, i_{out} (green) 2A/div, *FFT* (yellow) 50V/div, time scale 10ms/div.

Fig. 17 demonstrate the full-bridge single phase inverter waveforms with HECBPWM harmonic cancelation method for the cases where $m=6$ and $m=9$. The first harmonic amplitude in the full-bridge inverter case is slightly lower than the simulation results, this is due to the dead-time added in the experimental gating signal and the saturation voltages of the IGBT transistors. These parasitic effects contribute to the appearance of very small harmonic content at the eliminated harmonics. The parasitic caused harmonics content is very low and can be filtered by the inductive load. The highest unwanted harmonic content is located at the carrier frequencies of 1250Hz and 1850Hz respectively. These results are in a good agreement with the results of the simulation and the theoretical calculations.



(a)



(b)

Fig. 18. Three-level NPC single-phase inverter waveforms with HECBPWM harmonic cancelation method. (a) $m=6$. (b) $m=9$. v_{out} (red) 30V/div, i_{out} (green) 2A/div, *FFT* (yellow) 50V/div, time scale 10ms/div.

The three-level NPC single-phase inverter waveforms with HECBPWM harmonic cancelation can be seen in Fig. 18. In the multilevel scenario the first harmonic content is lower from the same reasons as shown for the full-bridge single-phase case. In addition to the previously mentioned parasitic effects, the bus capacitor unbalance further contributes to output voltage distortion. The additional distortion manifest as additional energy in the eliminated harmonics frequencies. Despite the appearance of odd harmonics, their effect on the output voltage is neglectable and can be filtered by the load inductive nature. As expected the highest unwanted harmonic content is located at the carrier frequencies in a similar manner to the full-bridge

single phase inverter case. These results in terms of harmonic elimination capabilities of the HECBPWM algorithm match the simulated results obtained via PSIM.

VI. Conclusion

A Hybrid Harmonic Elimination Carrier Based Pulse Width Modulation method for sinewave generation has been introduced and validated via a FPGA based digital controller and a three-phase multilevel inverter experimental prototype. The harmonic elimination algorithm is capable of producing the inverter control signals in order to eliminate unwanted harmonics of the output voltage waveform. The HECBPWM allows the generation of continues duty cycle trajectories as a function of the desired modulation index. The duty cycle functions are extrapolated offline and without the need of bulky lookup tables, this contributes to the reduction of the digital controller computational efforts. The HECBPWM harmonic elimination capabilities are demonstrated using a full-bridge single phase inverter and a three-level NPC single-phase inverter in both simulations and experimentally. The experimental three-phase multilevel inverter prototype results show the cancelation of multiple unwanted harmonics while powering an inductive load. The experimental results are with excellent correlation to the simulated results.

References

[1] Electric Utility Roles in the Electric Vehicle (EV) Market: Consensus Principles for Utility EV Program Design, Great Plains Inst.,Minneapolis, MN, USA, Apr. 2018.

[2] Taking the High Road: Strategies for a Fair EV Future, Workers, United Auto. Detroit, MI, USA, Jul. 2019.

[3] A. A. A. Al-Karakchi, G. Putrus, R. Das, "Smart EV charging profiles to extend battery life", *52nd International Universities Power Engineering Conference,* pp. 1-4. 2017.

[4] A. A. A. Al-Karakchi, G. Lacey, G. Putrus, "A method of electric vehicle charging to improve battery life,"*50th International Universities Power Engineering Conference,* pp. 1-3, 2015.

[5] J. S. S, K. R, S. P, N. G. Iyer, A. M, N. S. B, "A Review on Charge Control Techniques for Batteries in Electric Vehicles," Second *International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies,* pp. 1-6, 2022.

[6] A. I. Maswood, P. L. A. Vu, M. A. Rahman, "Silicon carbide-based inverters for energy efficiency," *IEEE Transportation Electrification Conference and Expo*, pp. 1-5 2012.

[7] K. Ohta "Variable Switching Frequency Control for Efficiency Improvement of Motor Drive System by Using GaN Three Phase Inverter" *IEEE International Conference on Industrial Technology*, pp. 119-123, 2020.

[8] J. Lee, D. Chun, J. Park, Y. Jung, E. G. Kang, M. Y. Sung, "Design of a novel SiC MOSFET structure for EV inverter efficiency improvement," *IEEE 26th International Symposium on Power Semiconductor Devices & IC's,* pp. 281-284. 2014.

[9] S. Ozdemir, F. Acar, U. S. Selamogullari, "Comparison of silicon carbide MOSFET and IGBT based electric vehicle traction inverters," *International Conference on Electrical Engineering and Informatics*, pp. 1-4, 2015.

[10] Ş. G. Roşu, C. Rădoi, M. Teodorescu, A. Savu, R. I. Bojoi, "Performance analysis of slope and frequency modulated carrier PWM methods for grid connected converters,"*8TH INTERNATIONAL SYMPOSIUM ON ADVANCED TOPICS IN ELECTRICAL ENGINEERING,* pp. 1-6, 2013.

[11] A. M. Trzynadlowski, R. L. Kirlin, S. F. Legowski, "Space vector PWM technique with minimum switching losses and a variable pulse rate," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 2, pp. 173-181,1997.

[12] C. Vazquez, "Switching losses reduction in current-controlled single-phase inverters, *"International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, pp. 650-655, 2008.

[13] F. G. Turnbull, "Selected harmonic reduction in static D-C — A-C inverters," *IEEE Transactions on Communication and Electronics*, vol. 83, no. 73, pp. 374-378, 1964.

[14] H. S. Patel, R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I Harmonic Elimination," *IEEE Transactions on Industry Applications*, vol. IA-9, no. 3, pp. 310-317, 1973.

[15] H. S. Patel, R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part II Voltage Control Techniques," *IEEE Transactions on Industry Applications*, vol. IA-10, no. 5, pp. 666-673, 1974.

[16] J. Jamaludin, N. A. Rahim, Hew Wooi Ping, "New three-phase multilevel voltage source inverter with low switching frequency," *TENCON 2011 - 2011 IEEE Region 10 Conference*, 2011

[17] K. Chaniago, N. A. Rahim, J. Selvaraj, "Single-phase seven-level voltage source inverter with low switching frequency," *TENCON 2009 - 2009 IEEE Region 10 Conference*, pp. 1-5, 2009.

[18] A. Shboul, I. Safi, S. Alhawamdeh, M. G. Batarseh, "Discussing single phase PWM voltage source inverters with different frequency modulation factors," *4th International Symposium on Environmentally Friendly Energies and Applications*, pp. 1-5, 2016.

[19] M. Ahmed, A. Sheir, M. Orabi, "Real-Time Solution and Implementation of Selective Harmonic Elimination of Seven-Level Multilevel Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1700-1709, 2017.

[20] Q. Jiang, D. G. Holmes, D. B. Giesner, "A method for linearizing optimal PWM switching strategies to enable their computation on-line in real-time," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, pp. 819-825 vol.1, 1991.

[21] R. J. Chance, J. A. Taufiq, "A TMS32010 based near optimized pulse width modulated waveform generator," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, pp. 903-908 vol.1, 1988.

[22] J. R. Tibola, H. Pinheiro, R. F. de Camargo, "Closed loop selective harmonic elimination applied to a grid connected PWM converter with LCL filter," *XI Brazilian Power Electronics Conference*, pp. 746-752, 2011.

[23] S. R. Bowes, P. R. Clark, "Transputer-based harmonic-elimination PWM control of inverter drives, "*IEEE Transactions on Industry Applications*, vol. 28, no. 1, pp. 72-80, 1992.

[24] J. Cheng, T. Xu, D. Chen, G. Chen, "Dynamic and Steady State Response Analysis of Selective Harmonic Elimination in High Power Inverters," *IEEE Access*, vol. 9, pp. 75588-75598, 2021.

[25] Y. Sahali, M. K. Fellah, "Selective harmonic eliminated pulse-width modulation technique (SHE PWM) applied to three-level inverter/converter," *IEEE International Symposium on Industrial Electronic*, pp. 1112-1117 vol. 2, 2003.

[26] A. B. Afarulrazi, M. Zarafi, W. M. Utomo, A. Zar, "FPGA implementation of Unipolar SPWM for single phase inverter," *International Conference on Computer Applications and Industrial Electronics*, pp. 671-676, 2010.

[27] E. Sunarno, I. Sudiharto, I. Ferdiansyah, S. D. Nugraha, O. A. Qudsi, M. G. Muhammad, "Design of Single-Phase Full Bridge Inverter for Uninterruptible Power Supply," *International Conference on Applied Information Technology and Innovation*, pp. 27-31, 2019.

[28] K. Zhang, Y. Kang, J. Xiong, J. Chen, "Direct repetitive control of SPWM inverter for UPS purpose," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 784-792, 2003.

[29] Y. Peng, W. Sun, F. Deng, "Internal Model Principle Method to Robust Output Voltage Tracking Control for Single-Phase UPS Inverters with Its SPWM Implementation," *IEEE Transactions on Energy Conversion*, vol. 36, no. 2, pp. 841-852, 2021.

[30] J. S. Lai, F.Z. Peng, "Multilevel converters-a new breed of power converters, *"Conference Record of the IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, pp. 2348-2356 vol.3, 1995.

[31] J. Rodriguez, J.S. Lai, F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, 2002.

[32] J. I. Leon, S. Vazquez, L. G. Franquelo, "Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2066-2081, 2017.

[33] A. Poorfakhraei, M. Narimani, A. Emadi, "A Review of Modulation and Control Techniques for Multilevel Inverters in Traction Applications," *IEEE Access*, vol. 9, pp. 24187-24204, 2021.

[34] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, 2007.

[35] M. Marchesoni, M. Mazzucchelli, S. Tenconi, "A non-conventional power converter for plasma stabilization,"*19th Annual IEEE Power Electronics Specialists Conference*, pp. 122-129 vol.1, 1988.

[36] N. Pallo, T. Foulkes, T. Modeer, S. Coday, R. Pilawa-Podgurski, "Power-dense multilevel inverter module using interleaved GaN-based phases for electric aircraft propulsion, "*IEEE Applied Power Electronics Conference and Exposition*, pp. 1656-1661*,* 2018.

[37] M. F. Escalante, J. Vannier, A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications, "*IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 809-815, 2002.

[38] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter, "*IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518-523, 1981.

[39] J. Rodriguez, S. Bernet, P. K. Steimer, I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219-2230, 2010.

[40] A. Choudhury, P. Pillay, "Space Vector Based Capacitor Voltage Balancing for a Three-Level NPC Traction Inverter Drive," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1276-1286, 2020.

[41] J. Pou, D. Boroyevich, R. Pindado, "New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1026-1034, 2002.