Integrated Delay-Line Based High-Resolution PFM-PWM Modulator

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***Abstract*— This article introduces a new architecture for an all-digital high-resolution variable-frequency variable-duty-cycle modulator. Constructed through digital standard-cell delay-line and simple combinatorial logic, the modulator produces PWM signals with time-resolution of a single delay-element for both switching frequency and duty-cycle attributes, thus making it a promising candidate for integration in hybrid controllers of high frequency resonant converters operating in the MHz range. Since the entire architecture is realized through standard cells, the solution also scales with fabrication technology and is described in HDL, which translates onto hardware using automated process. The modulator has been designed on a 0.18μm 5V CMOS platform, totaling 0.18mm^2 of effective silicon area as well as on an Altera FPGA to demonstrate the versatility of the architecture. Experiment results of the FPGA prototype are provided as well as post-layout simulations of the ASIC realization for a variety of mitigation sequences achieving time-resolution of 220ps and 200ps, respectively.**

Keywords – LLC, resonant converter, time-domain analysis, PWM, PFM.

I. INTRODUCTION

Digital architectures and realizations of controllers for switched mode power supplies (SMPS) have been in pursuit by both industry and academia for many years [1]-[10]. Beyond the conventional attributes of flexibility, scalability and noise immunity, this approach allows for assimilation of complex control laws and algorithms to enhance transient performance [11]-[12] and optimize steady-state operation [13]. Such control schemes may involve hybrid frequency and duty-cycle modulation to improve efficiency [14]-[15], perform regulation tasks [16]-[17] or execute convoluted mitigation sequences [18]. Following the miniaturization trend of IoT devices and portable consumer electronics requiring point-of-load (PoL) power conversion, such controllers are expected to operate at high switching frequencies with very high time-resolution to fully exploit these state-of-the-art control algorithms [19]-[22].

Pulse width modulators are key components of modern controllers [23]-[27]. Their respective pulse width modulation resolution must comply with the regulation accuracy and be higher than the analog-to-digital converter's (ADC) to avoid limit cycle oscillations [28]-[29]. Moreover, these modules are characterized by their frequency and duty-cycle range, monotonicity and linearity characteristics and their dynamic performance. Therefore, in the context of digitally controlled low-volume SMPS, a miniaturized HR PWM modulator with lean silicon utilization capable of generating gating signals with adjustable frequency and duty-cycle is an essential building block to achieve the regulation goals.

The conventional approach to implement HR digital pulse-width modulator (HR-DPWM) is by a fast-clocked counter-comparator scheme [30]-[31]. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n{\cdot}fs$, which directly translates into increased power consumption and complex design to realize the high-speed circuitry. Traditionally, these architectures can be altered to include single [4] or several [32] delay-lines (DL) to improve the duty-cycle resolution of the generated PWM signals. For example, the monolithic HR-DPWM module presented in [4] achieves time-resolution of 200ps for the duty-cycle attribute while the switching frequency resolution is bounded by the reference clock signal. Consequently, these modulators can be incorporated in constant switching frequency SMPS to enhance regulation capabilities but will result in limited improvement when integrated in resonant topology-based power-supplies. Here, state-of-the-art control schemes require high-resolution attributes for both control variables, i.e. switching-frequency and duty-cycle [16],[21].

The objective of this study is therefore to introduce a new high-resolution variable-frequency variable-duty-cycle modulator (HR-VFVDM) for low-power high-frequency and volume-sensitive controller architectures, as shown in Fig. 1.

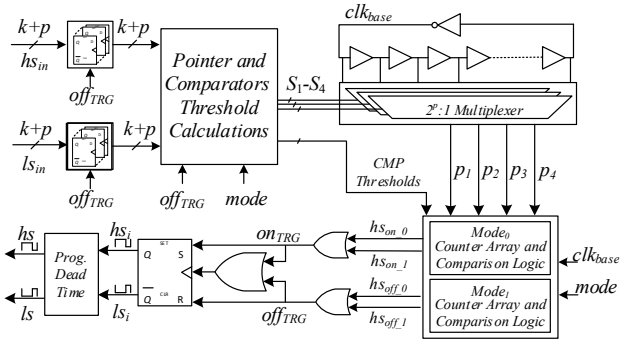

Fig. 1. Simplified block diagram of the high-resolution variable frequency variable duty-cycle modulator.

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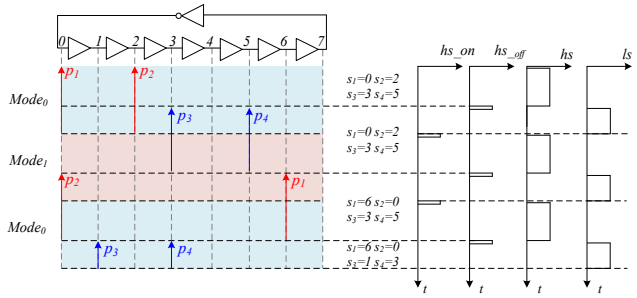

Fig. 2. Illustrative example of the HR-VFVDM operation with p=3, hs_in[2:0]=3'b001 and ls_in[2:0]=3'b010.

Time-resolution of a single delay-element (DE) is obtained for both frequency and duty-cycle attributes of the generated PWM signals while ensuring single-cycle convergence operation. The modulator's architecture is delay-line based and is entirely described in HDL using standard-cell libraries without extensive custom design to allow fast adaption and implementation in various development or fabrication platforms. It is a further objective of this paper to discuss specific realization aspects of delay-line based architectures on programmable fabrics such as FPGAs and as an integrated module in an ASIC solution.

The rest of the paper is organized as follows: Section II describes the HR-VFVDM architecture and covers its principle of operation. Section III details practical implementation issues along with design and realization guidelines. Post-layout validation and experimental results are provided in section IV. Section V concludes the letter.

II. Architecture and Mode of Operation

The HR-VFVDM operates in an asynchronous manner [4], i.e. not synchronized to an external clock, and therefore its architecture is meticulously tailored to the signal paths between its sub-modules, as depicted in Fig. 1. It comprises a register-based input stage that samples the PWM signals' on-time commands ($hs_{in}[n]$ and $ls_{in}[n]$) and dead-time ($dt[_n]$) on a cycle-by-cycle basis followed by a digital computational logic that produces two sets of internal signals (s_1-s_4 and *CMP Thresholds*), as shown Fig. 1. The former is used as input to the multiplexer-array which yields time-delayed replicas of the ring-oscillator base clock (p_1-p_4) while the latter is fed into the counter-comparator sub-modules producing internal signals that mark the initiation and termination of each switching-cycle segment (hs_{on} and hs_{off}). These signals are processed by the output logic block and the delay-line based dead-time module to produce the resulting PWM signals, *hs* and *ls*.

The reference clock signals of the HR-VFVDM counter-comparator sub-modules are not confined to a specific location in the ring-oscillator as in conventional realizations but rather modified on a cycle-by-cycle basis by the internal computational blocks to accommodate the instantaneous gating commands, $hs_{in}[n]$ and $ls_{in}[n]$. This is carried out by the multiplexer array that provides direct access to all propagating signals in the DL as shown in Fig. 1, which is the enabler for the high-resolution attributes of the modulator. Therefore, each segment of the generated PWM signal is individually produced with time-resolution of a single delay-element, i.e. the falling- or rising-edges of the PWM signals can be positioned without any limitations along the DL which translates into a heel-to-toe algorithm. To ensure stabilization of the multiplexer array's outputs prior to the beginning of each switching-cycle the modulator's operation is divided into two modes that interchange periodically, $mode_0$ and $mode_1$, as well as dedicated hardware for each mode as shown in Fig. 1.

The on-time commands, $hs_{in}[n]$ and $ls_{in}[n]$, are sampled periodically and stored in dedicated registers as shown in Fig. 1. Here, the first k bits form the coarse section of the command dictating the required number of full-cycle count while the remaining p bits represent the fine-tuning addition in accordance with the DL length, i.e. 2^p DEs as shown in Fig. 1. The LSB sections of the sampled signals are used to calculate the multiplexer-array inputs (s_1-s_4) with respect to their previous values according to:

$$\begin{cases} s_1 = s_4 + hs_{in}[p-1:0] \\ s_2 = s_4 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \\ s_3 = s_2 + hs_{in}[p-1:0] \\ s_4 = s_2 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \end{cases}, \quad (1)$$

where s_1-s_2 are associated with $mode_0$ and s_3-s_4 with $mode_1$. The resultant delayed replicas of clk_{base}, i.e. p_1-p_4 in Fig. 1, are fed into the counter-comparator sub-modules and act as their respective clock signals with frequency of:

$$f_{base} = \frac{1}{2^{p+1} \cdot t_{de}}, \quad (2)$$

where t_{de} is the average time delay of each DE. The p_1- and p_3-fed counter-comparator modules control the falling-edge of the PWM output for $mode_0$ and $mode_1$, respectively while p_2 and p_4 are utilized in the same manner to control its rising-

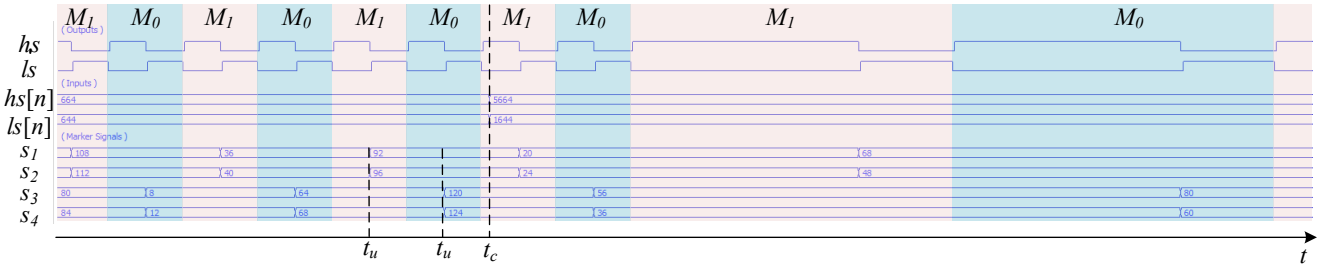

Fig. 3. Logical simulations carried out in QuestaSim for steady-state and transition mitigation sequences.

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edge instance. This is carried out by comparing the internal counters' values with the MSB sections of the on-time commands (*CMP Thresholds*) yielding the hs_{on} and hs_{off} signals as shown in Fig. 1. Accordingly, the internal high-side PWM signal (hs_i) rises at the beginning of each switching cycle with the positive-edge of hs_{on} and remains high until hs_{off} resets the SR-FF thus driving the low-side PWM signal (ls_i) with logic high value. These signals are then passed through a DL-based programmable dead-time module [4] to produce the final PWM signals, *hs* and *ls*.

The operation of the HR-VFVDM and the pointers' movement along the DL are demonstrated in the illustrative example of Fig. 2 for a case of p=3 and different on-time commands for the two PWM segments. Here, the LSB section of *hs_in*[*n*] is 3'b001 which results in an added time interval of t_{de} to the first segment of the PWM signal. This is carried out by positioning the p_1 and p_3 pointers one DE apart from p_4 and p_2, respectively. In a similar manner, the LSB section of *ls_in*[*n*] is 3'b010 which results in positioning p_2 and p_4 two DEs apart from p_1 and p_3, respectively, yielding in a $2t_{de}$ extension to the *ls* signal. The s_1-s_4 values are calculated on a cycle-by-cycle basis according to (1) thus not confining the initiation signal, *hs_on*, to a fixed position in the DL. Moreover, the pointers calculations are carried out at the rising edge of the *hs_off* signal, i.e. at the falling edge of the *hs* signal, which ensures steady inputs to the ring-oscillator multiplexer-array module in the succeeding switching cycle.

Logical simulations carried out in QuestaSim for a 13-bit HR-VFVDM are shown in Fig. 3. Here, the DL consists of 128 DEs (p=7) and the multiplexer-array comprises four 2^7:1 multiplexers. The inputs of the module, i.e. $hs_{in}[n]$ $ls_{in}[n]$, are specified at the top of the timing diagram along with the mode status ($mode_0$ or $mode_1$). For simplicity reasons, the dead-time is kept constant and equals 63 DEs. According to (1), the fine-segment of the on-time commands is derived and equals to 24 and 4 for the high-side and low-side drive signals respectively until the change in both duty-cycle and switching frequency is enforced in the marked time location of t_c. As can be seen, s_1-s_4 signals are interchangeably updated every switching-cycle according to (1) at the falling edge of the hs_i signal, marked as t_u instances in Fig. 3. To best showcase the capabilities of the HR-VFVDM, both the duty-cycle and switching frequency attributes are abruptly modified from 13'd664 and 13'd644 to 13'd5664 and 13'd1644. As can be seen, the resultant PWM signals nor the internal control signals suffer from non-continuities and single-cycle convergence is achieved.

III. Practical Implementation

A. IC Implementation

The realization of the HR-VFVDM relies on an automated digital implementation flow, using vendor's standard cells thus completely eliminating the need for custom design. The ASIC implementation is described through three main steps. In the first step, each module is described in HDL as a standalone unit. This is done for the simplicity of the verification and functionality simulations. Then, each unit is translated into hardware using synthesis and timing verification tools into an optimized gate-level representation. In this step physical design constraints are enforced to ensure tight and dense realization of DL-based structures such as the ring-oscillator and high symmetry in modules such as the multiplexer-array which comprises several instantiations of the same sub-module. In the third step, all units are integrated together onto the higher hierarchy of the HR-VFVDM. Here, the automated place-and-route tools are instructed to position specific sub-modules adjacent to each other in accordance with the required data paths along with conventional area and timing constraints to achieve compact silicon realization without compromising on resolution. This prohibits the CAD tools to perform general area optimization but rather take into account the asynchronous nature of the architecture and its structure as depicted in Fig. 1.

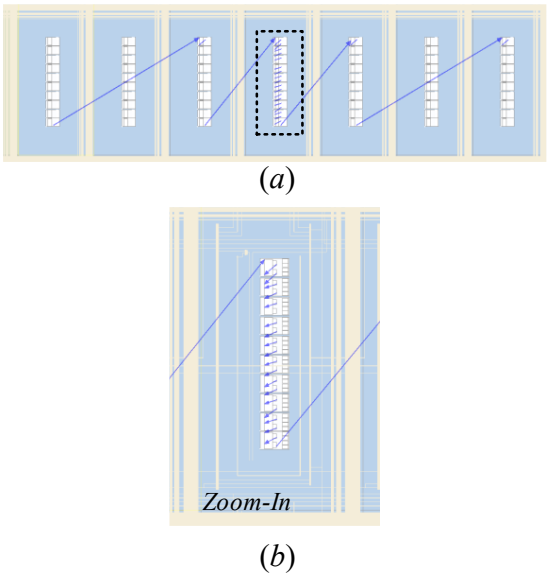

Fig. 4. Internal FPGA routing of a DL-based sub-module.

B. FPGA Implementation

Realization of DL-based architectures on programmable fabrics such as FPGAs largely follows the ASIC design guidelines with several key modifications. First, an in-depth investigation of the target FPGA should be conducted with emphasis on DL-based structures that can be exploited in the implementation of the ring-oscillator or the programmable dead-time modules. For example, Xilinx Virtex FPGAs [33] include several custom designed voltage-tolerant components (IODELAY) to perform high resolution delay adjustments for DDR interfaces that can be instantiated as part of the HR-VFVDM. However, such an approach may be limited due to available hardware resources and will entail additional design efforts during a transition to ASIC.

An alternative approach, pursued in this study, is realizing DL-based structures with simple look-up tables (LUTs) available in every programmable fabric unit or with dedicated delay-cells that are typically instantiated to fix hold

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time violations in synchronous designs. To ensure constant propagation delay, their location should be fixed and confined to a pre-determined position. However, in most FPGAs delay-cells are not found in all rows or columns of the mesh grid which results in gaps between routed regions of the DL, as can be seen in Fig. 4a. Therefore, some degradation is expected in terms of time-resolution due to the additional delay, an undesired phenomenon that can be minimized by positioning the sub-modules in adjacency according to the data flow. Shown in Fig. 4b is a zoom-in on a configurable logic block (CLB) and its internal routings between delay-cells realized as part of the ring-oscillator.

IV. Post Layout Validation and Experimental Results

To validate the operation of the new HR-VFVDM, it has been realized in TowerJazz 0.18μm 5V CMOS process as well as on Altera Cyclone V FPGA. The source codes, i.e. the HDL (Verilog) codes, for the FPGA and ASIC implementations are identical and were converted to hardware using Quartus environment and Cadence tools, respectively. Shown in Fig. 5 is the resultant layout with overall silicon area of 0.18mm^2. As can be seen, the layout encapsulates the core attributes of the design, among them the symmetry between $mode_0$ and $mode_1$ hardware, the adjacency of the DL and the multiplexer array, etc. The DL comprises 128 DEs and the on-time commands, i.e. $hs_{on}[n]$ and $ls_{on}[n]$, are 13-bit long.

Shown in Fig. 6-8 are post-layout results of the integrated realization during steady-state and multiple transition scenarios carried out in Virtuoso environment with Cadence ADE simulation tools to account for both routing delays and parasitics. Steady-state operation is demonstrated in Fig. 6 for hs_{on}=2280 and ls_{on}=1720. The switching frequency and the duty-cycle remain constant and equal 1.25MHz and 57%, respectively. As can be seen, the *mode* signal changes periodically indicating the operating time intervals of each hardware module ($Mode_0$ or $Mode_1$ in Fig. 5). The SR-FF input signals, *on_trg* and *off_trg*, are shown to exemplify the relationships between the counter-comparator modules and the generated PWM signals. The HR attributes of the generated PWM signal are shown in the zoom-in of Fig. 5b where the *on_trg* signal rises to logic high asynchronously to the ring-oscillator reference signal, *clk_base*.

Fig. 7 demonstrates the HR-VFVDM response to a step in the duty-cycle while the switching frequency is kept constant at 470kHz. Prior to the transition event, the values of $hs_{on}[n]$ and $ls_{on}[n]$ are 6719 and 3918, respectively. In this scenario the on-time commands are swapped, resulting in complementary duty-cycle with the same switching frequency. As can be seen, the HR-VFVDM supports constant switching frequency operation without compromising on the HR attributes of the generated PWM signals thus allowing integration in a variety of constant switching frequency power supplies.

Fig. 8 demonstrates the modulator's response to an abrupt change in both duty-cycle and switching frequency attributes. Prior to the transition event the switching

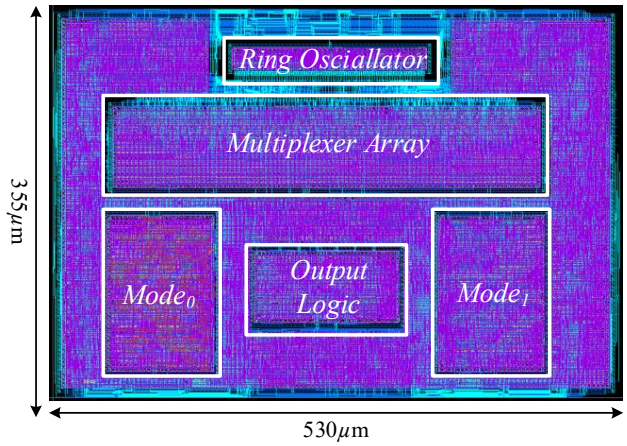

Fig. 5. HR-VFVDM layout.

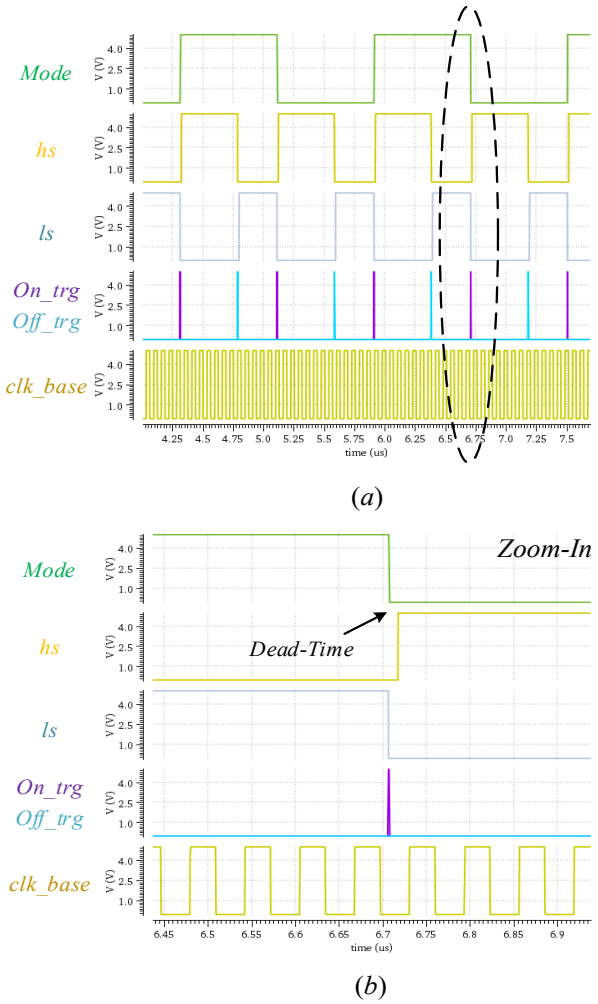

Fig. 6. Post layout simulations. (a) HR-VFVDM steady-state operation. (b) Zoom-in on a transition event.

frequency is 880kHz and the on-time commands of $hs_{on}[n]$ and $ls_{on}[n]$ are 959 and 4721, respectively. The modified values of $hs_{on}[n]$ and $ls_{on}[n]$ are 3193 and 7746 resulting in the new switching frequency of 457kHz. As can be seen, the new steady-state is achieved within a single switching cycle

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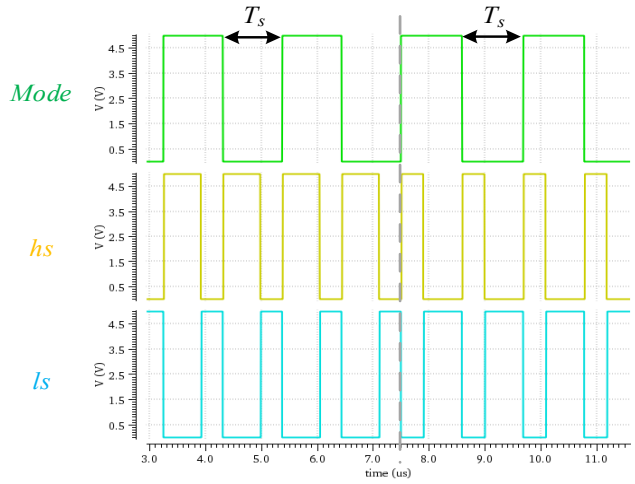

Fig. 7. Constant frequency operation (f_{sw}=470kHz) with a step in the duty-cycle command.

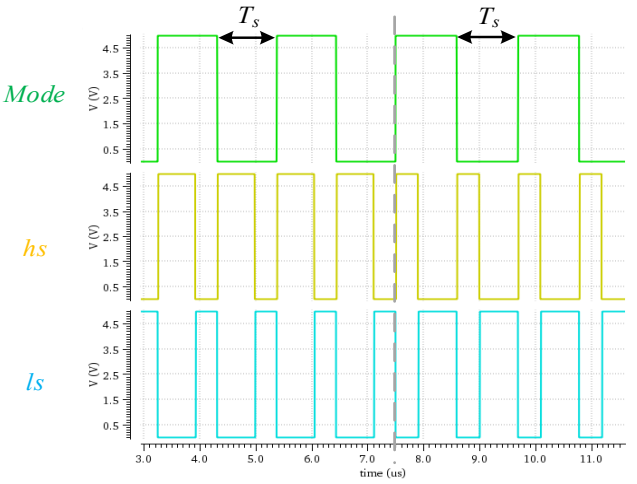

Fig. 8. HR-VFVDM response to a change in both switching frequency and duty-cycle commands.

thus validating its compatibility in advanced hybrid PFM-PWM controllers for resonant converters [16],[21]. The time-resolution for the ASIC realization is extracted from the post-layout simulations of Fig.6-8 and equals approximately 200ps regardless of the operating point which validates the monotonicity attribute of the architecture.

Shown in Fig. 9a-b are experimental waveforms of the FPGA-based realization operating in the MHz range (1.8MHz and 1.2MHz) with arbitrary duty-cycle commands (38% and 26%). As can be seen, correct operation is obtained regardless of the relatively complicated routing of asynchronous designs in programmable platforms which validates the design guidelines discussed in IV.

V. Conclusion

A new architecture for an all-digital PFM-PWM modulator has been presented and verified through post-layout simulations and experimental data. The modulator generates gating signals with adjustable switching frequency,

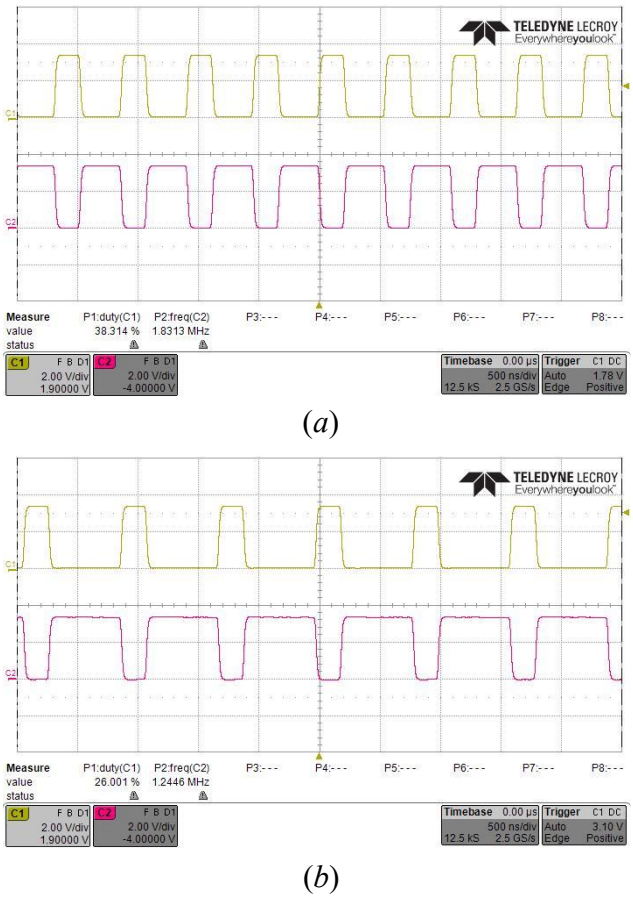

Fig. 9. Experimental results of the FPGA-based realization. (a) f_{sw}=1.8MHz and D=38%. (b) f_{sw}=1.2MHz and D=26%.

duty-cycle and dead-time attributes with time resolution of a single DE. The assignment of the on-time intervals for each PWM segment is carried out on a cycle-by-cycle basis by simple combinatorial logic and DL structures. The solution is compact, scalable and is based on standard cells alone, without any custom design modules, making it an attractive candidate for integration in modern controller ICs.

The HR-VFVDM has been designed in a digital-oriented approach and implemented on a 0.18μm 5V CMOS process resulting in total silicon area of 0.18mm^2 as well as on a programmable logic fabric to showcase the adaptability of the architecture. Experimental results of the FPGA prototype are provided as well as post layout simulations for multiple mitigation sequences demonstrating single-cycle convergence and stable operation in the MHz range without compromising on resolution.

Acknowledgements

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