A Self-Adjusting Sinusoidal Power Source Suitable for Driving Capacitive Loads

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***Abstract*—A new self-adjusting current-fed push–pull parallel inverter (SA–CFPPRI) is presented and tested by simulation and experimentally. The power source includes a soft switching control circuitry and a controllable inductor. The SA–CFPPRI can drive a capacitive load at any frequency within the design range. It will maintain zero voltage switching of the main transistors and follow the input frequency signal even when the resonant elements and/or the load vary. Possible range of applications for the proposed power source is: piezoelectric transformers and motors, ac bus for a distributed power system and other loads that need to be fed by a sinusoidal waveform. The experimental results of the laboratory unit (160 Vrms at 93 kHz and nominal output power of 5 W) verify the analytical analysis and proposed design procedure.**

***Index Terms*—Phase comparator, push–pull parallel resonant inverter (PPPRI), sinusoidal power source, variable inductor.**

I. Introduction

THE favorable drive signal for a number of capacitive loads is a sinusoidal waveform. For example, piezoelectric devices and in particular piezoelectric motors need to be driven by a high frequency sinusoidal waveform [1]–[6]. This is required since the optimal performance is obtained when the drive is of low harmonics contents.

Capacitive loads pose a number of non-trivial power electronics design problems. The major one being the reactive current that may reduce dramatically the efficiency if it is allowed to pass through the power switches. Another problem is the need to accommodate load changes (both the active and reactive parts) without affecting the amplitude, waveform and efficiency of the power driver. The current-fed push–pull resonant inverter (CFPPRI) [7] was shown earlier to be a useful topology for driving capacitive load [5]. However, the basic CFPPRI suffers from a number of drawbacks that will reduce the efficiency and increase distortion if the load capacitance or operating frequency is non-constant. In this study, we explored the possibility of converting the CFPPRI into a self-adjusting system that will accommodate load capacitance changes and frequency shifts without increasing the losses or distorting the waveform fed to the load.

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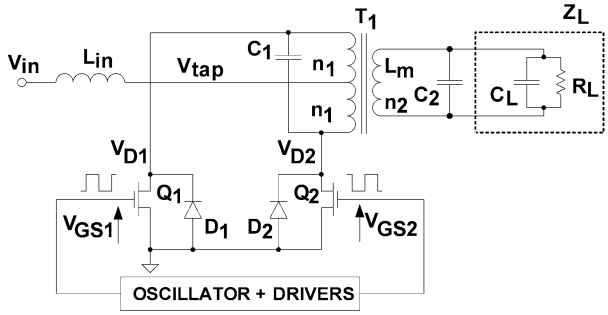


Fig. 1. Basic configuration of the CFPPRI loaded by a capacitive load.

II. Current-Fed Push–Pull Parallel Resonant Inverter (CFPPRI)

The basic CFPPRI topology (Fig. 1) includes a push–pull stage with two transistors (Q_1, Q_2) driving a parallel resonant network and fed by a series inductor $L_{\rm in}$. The load (capacitive in this case) is fed via a secondary winding that allows for amplitude adjustment by the turns ratio $(n_2/2n_1)$. The resonant frequency $(f_{\rm r})$ of the parallel resonant network will be

$$f_{\rm r} = \frac{1}{2\pi\sqrt{L_{\rm m}C_{\Sigma}}} \tag{1}$$

where $L_{\rm m}$ is the secondary inductance and C_{Σ} is the total capacitance reflected to the secondary $(C_1(n_2/2n_1)^2 + \mathrm{C}_2 + C_{\rm L})$.

When the gate drive frequency of the CFPPRI, $f_{\rm s}$, matches the resonant frequency, $f_{\rm r}$, the transistors will operate under zero voltage switching (ZVS) conditions [Fig. 2(a)] and in this case the reactive current of the equivalent resonant network will not pass through the switches. This is the most desirable case. If the frequency of the gate drives is lower than the resonant frequency [Fig. 2(b)], the operation will include a "Boost" period in which one transistor and one antiparallel diode are carrying the inductor current [8], [9]. This will cause distortion in the output voltage and will increase the conduction losses. If the gate drive frequency is higher than the resonant frequency [Fig. 2(c)], the operation will be under hard switching conditions. This will cause distortion of the load signal and will introduce switching losses. In many practical applications, an exact matching of the resonant elements to the gate drive frequency (and the desired output frequency) is not possible. Interconnecting cable capacitances, tolerances of the passive components and the variability of the load capacitance will cause the CFPPRI stage to operate in one of the mismatched modes, which would be highly undesirable in some applications such as piezoelectric motors.

The sensitivity of the CFPPRI to deviation of the drive frequency from the resonant frequency can be remedied by

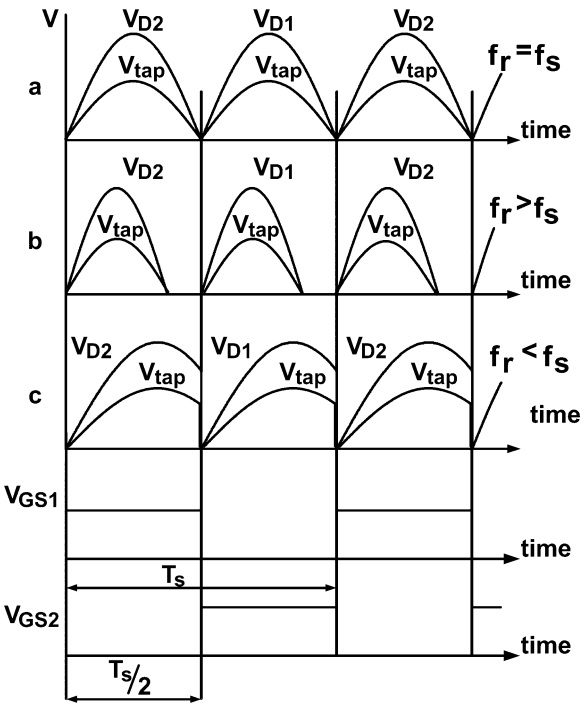


Fig. 2. Gate voltages ($V_{\rm GS}$), drain voltages ($V_{\rm D}$) and tap voltage ($V_{\rm tap}$) when the gate-drive frequency matches (a) the resonant frequency, and (b) when it is lower or (c) higher than the resonant frequency.

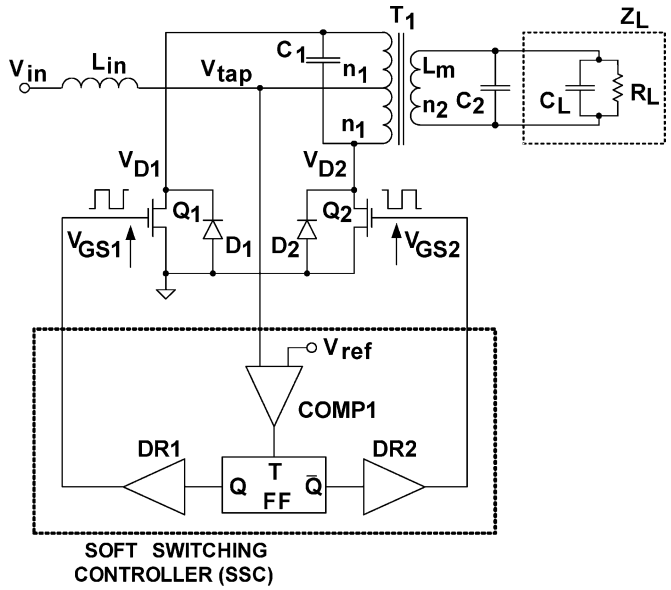


Fig. 3. Soft switching controller (SSC) for a CFPPRI.

locking the drive frequency to the resonant frequency. That is, to make the gate drive frequency equal to the resonant frequency. This converts, in fact, the operation from a driven to a self-driven CFPPRI configuration [7] except that an active driver is included and an active comparator is used to detect the zero crossing (Fig. 3). This soft switching control (SSC) method is employed in commercial controllers/drivers (e.g., UC3872 by Texas Instruments) that include all the associated circuitry—such as a starting and protection circuitries.

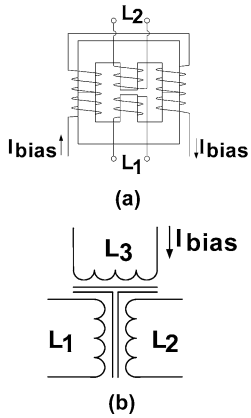


Fig. 4. (a) Variable inductor and (b) its schematics symbol.

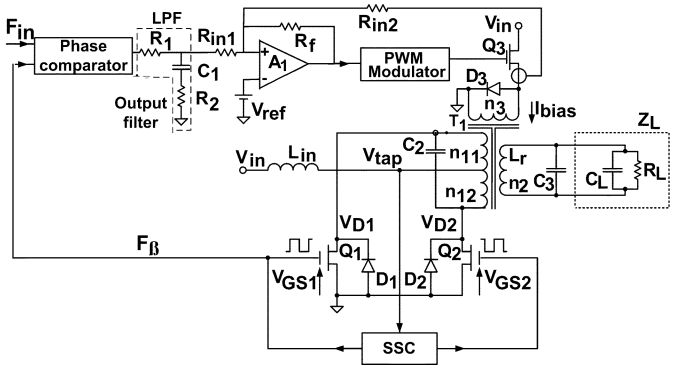


Fig. 5. Basic configuration of the SA–CFPPRI.

The SSC ensures ZVS even if the inductance and total capacitance of the resonant network are non-constant since it forces the gate drive frequency to match the resonant frequency. However, if the load needs to be driven at a predetermined frequency, the SSC solution, by itself, is not sufficient. This deficiency is solved in proposed approach by applying a variable inductor [10], [11].

III. Self-Adjusting CFPPRI (SA-CFPPRI)

By including both a SSC and a variable inductor, the CFPPRI can be made to operate at a desired switching frequency and at the same time maintain ZVS. The variable high frequency inductor presented earlier [10] is based on an E core with a gapped center leg and bias windings on the non-gapped side legs (Fig. 4). The self-adjusting operation is achieved by including into the CFPPRI the variable inductor and introducing a buck type converter, for feeding the bias windings. Frequency tracking is accomplished by closing the loop on a phase comparator that generates an error signal as function of a phase mismatch between the desired frequency and the SA-CFPPRI frequency (Fig. 5).

The bias drive of the SA–CFPPRI is designed as a closed feedback loop configuration to maintain a forced current control. This is required to reduce the order of the outer feedback loop. The simplified block diagram of the SA–CFPPRI (Fig. 6) includes, therefore, two feedback loops: an inner current loop and an outer phase loop.

Starting from left side, $K_{\rm p}$ represents the gain of the phase comparator while the blocks “Int1” and “Int2,” stand for the

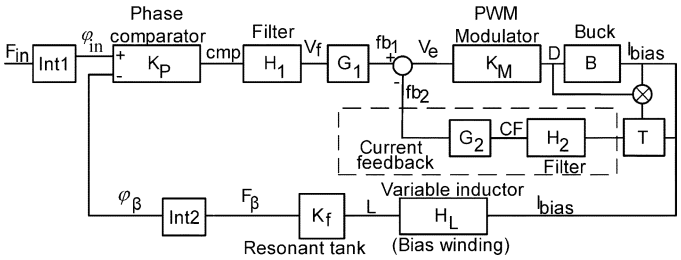


Fig. 6. Simplified control block diagram of proposed SA-CFPPRI.

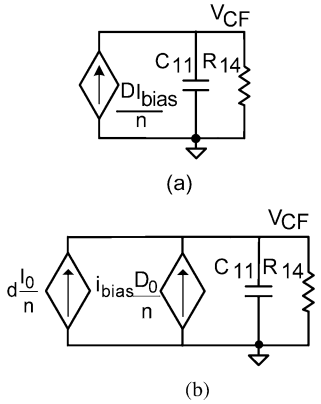


Fig. 7. Current feedback circuitry including the current transformer: (a) large signal and (b) small signal.

integration operation that transfers frequency into phase. H_1 is the phase comparator's output filter designed to be of the lag-lead type (Fig. 5). G_1 and G_2 are the gains of the summing amplifier A_1. $K_{\rm M}$ (Fig. 6) is the transfer ratio of the modulator (error signal to duty cycle). B is the transfer function of the Buck converter (duty cycle to current). T is the transfer ratio of the pulse transformer and H_2 is the pulse transformer filter. $H_{\rm L}$ is the relationship between the bias current and the inductance of the bias winding n_3 of T_1 (Fig. 5). And finally, $K_{\rm f}$ is the response of the tank to the bias current (the ratio of resonant frequency to bias current).

When considering the low frequency response of the system, $K_{\rm P}, G_1, G_2, K_{\rm M}, H_{\rm L}$ and $K_{\rm f}$ (Fig. 6) can be assumed to be fast responding as compared to H_1 (response of phase comparator filter) and B (Buck converter) [12]. Without current feedback around the Buck converter, the system will be of a second order form and therefore hard to stabilize. This is because the transfer function from error signal to inductor current is expected to be a first order system and when in series with integrator (Int2, Fig. 6) the loop gain of the system will be of the second order form. Current feedback is implemented [Fig. 7(a)] by sensing the switch current of the buck converter with a current transformer, filtering the signal by an R–C network and feeding the signal back to the summing amplifier A1 (Figs. 5 and 6). The bias inductor current can be expressed as

$$I_{\rm bias} = \frac{DV_{\rm in}}{sL_{\rm b0}} \tag{2}$$

where "s" is the Laplace operator, $L_{\rm b0}$ is the bias inductor value for a given operating condition and D is the duty cycle of the buck converter. After linearization, the small signal transfer function between duty cycle and the inductor current $b(s)$, is expressed as

$$b(s) = \frac{i_{\rm bias}}{d} = \frac{V_{\rm in}}{sL_{\rm b0}} \tag{3}$$

where $i_{\rm bias}$ is the small signal inductor current and d is the duty cycle perturbation.

Since the current is sensed at the switch branch (Fig. 5), the average current feedback signal $I_{{\rm f}(av)}$ can be expressed as [Fig. 7(a)]

$$I_{\rm f}(av) = \frac{DI_{\rm bias}}{n} \tag{4}$$

where $n = n_2/n_1$ is the turns ratio of the current transformer. Applying, once again, linearization around the operating point (denoted by the subscript 0) we find the expression for the small signal average feedback current $(i_{\rm f}(av))$

$$i_{\rm f}(av) = \frac{dI_{\rm bias0}}{n} + \frac{i_{\rm bias}D_0}{n}. \tag{5}$$

Hence, the small signal equivalent circuit of the current sensing circuitry (T and B in Fig. 6) can be represented by Fig. 7(b). The voltage feedback signal $v_{\rm CF}$ that will develop at the output of the current sense filter will thus be

$$v_{\rm CF}(s) = \left[d\frac{I_0}{n} + i_{\rm bias}\frac{D_0}{n}\right]\frac{R_{14}}{sC_{11}R_{14}+1}. \tag{6}$$

Combining (3) and (6) yields

$$v_{\rm CF}(s) = \left[d\frac{I_0}{n} + d\frac{V_{\rm in}}{sL_{\rm b0}}\frac{D_0}{n}\right]\frac{R_{14}}{sC_{11}R_{14}+1}. \tag{7}$$

Consequently, the transfer function $v_{\rm CF}$ to d, $[cf(s)]$ can now be expressed as

$$cf({\rm s}) = \frac{v_{\rm CF}}{d}(s) = \left[\frac{V_{\rm in}}{sL_{\rm b0}}\right] \times \left[\frac{D_0R_{14}}{n}\left[s\left(\frac{L_{\rm b0}I_0}{V_{\rm in}D_0}\right)+1\right]\frac{R_{14}}{sC_{11}R_{14}+1}\right]. \tag{8}$$

It should be noted that this equation combined the effect of B (the Buck converter), (T the pulse transformer), and H_2 (the pulse transformer filter) (Fig. 6).

For a given nominal operating point, one can design the feedback as a frequency independent gain by pole zero cancellation

$$s\left(\frac{L_{\rm b0}I_0}{V_{\rm in}D_0}\right)+1 = \frac{R_{14}}{sC_{11}R_{14}+1}. \tag{9}$$

Isolating C_{11}, yields the flat filter transfer function criterion

$$C_{11} = \frac{L_{\rm b0} I_0}{V_{\rm in} D_0 R_{14}}. \tag{10}$$

Note that the resistor R_{14} also controls the total gain of the block. Once R_{14} is chosen, C_{11} value can be selected according to (10).

Taking into account G_2 (error amplifier gain) and $K_{\rm M}$ (modulator's transfer ratio) (Fig. 6), the closed loop transfer function of the Buck converter from the output of $H_1, v_{\rm f}$ (Fig. 6) to the bias current $i_{\rm bias}, A_{\rm CL\_CL}({\rm s})$ is:

$$A_{\rm CF\_CL}(s) = \frac{i_{\rm bias}}{v_{\rm f}} = \frac{G_1 K_{\rm M} b}{1 + G_2 K_{\rm M} c f} \tag{11}$$

where $K_{\rm M}, b, G_2$ are the current loop transfer functions and G_1 is the error amplifier gain (Fig. 6) [12].

Inserting (8) into (11) one gets

$$A_{\rm CF\_CL}(s) = \frac{G_1 K_{\rm M} b}{1 + \frac{D_0 R_{14} K_{\rm M}}{n} G_2 b \left[s \frac{L_{\rm b0} I_0}{V_{\rm in} D_0} + 1 \right] \frac{1}{s C_{11} R_{14} + 1}}. \tag{12}$$

And for the case of the pole-zero cancellation (10)

$$A_{\rm CF\_CL}(s) = \frac{G_1 K_{\rm M} b}{1 + b G_2 K_{\rm M} \frac{D_0 R_{14}}{n}}. \tag{13}$$

Applying (3) and selecting G_1 to be equals to G_2, (13) reduces to a first order system with a bandwidth of $\omega_{\rm CL}$

$$A_{\rm CF\_CL}(s) = \frac{A_{\rm CL0}}{1 + s/\omega_{\rm CL}} \tag{14}$$

where

$$A_{\rm CL0} = \frac{n}{D_0 R_{14}}$$
$$\omega_{\rm CL} = G_2 K_{\rm M} \frac{D_0 R_{14}}{n} \frac{V_{\rm in}}{L_{\rm b0}}.$$

Equation (14) implies that for the frequency range $\omega < \omega_{\rm CL}$, the current feedback has transformed the buck converter (from error signal to bias current) from a first order system to a zero order system. If the parameters of (13) are chosen such that the bandwidth $\omega_{\rm CL}$ of the current converter is larger than the bandwidth of the overall system then the closed loop response of the system $f_\beta / f_{\rm in}, A_{\rm PF\_CL}(s)$, can be expressed as

$$A_{\rm PF\_CL}({\rm s}) = \frac{f_\beta}{f_{\rm in}}(s) = \frac{1}{s} \frac{A_{\rm PF}}{1 + \beta_{\rm PF} A_{\rm PF}} \tag{15}$$

where

$$A_{\rm PF} = K_{\rm p} h_1 A_{\rm CF\_CL} K_{\rm f} H_{\rm L}$$
$$\beta_{\rm PF} = \frac{1}{s}.$$

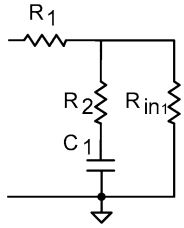


Fig. 8. Phase comparator output filter.

After some manipulation the closed loop transfer function of the system can be shown as a first order system of bandwidth ω_0

$$A_{\rm PF\_CL}(s) = \frac{1}{1 + s/\omega_0} \tag{16}$$

where

$$\omega_0 = K_{\rm p} h_1 A_{\rm CF\_CL} K_{\rm f} H_{\rm L}.$$

The parameters h_1 and $A_{\rm CF\_CL}$ in above expressions stand for the transfer functions of the phase comparator output filter, H_1, and the current feedback closed loop, $i_{\rm bias}/v_{\rm f}$ (Fig. 6) at frequencies close to ω_0. The filter, H_1, is designed to be a lag-lead network (Fig. 8) [12] and the zero is placed to be below ω_0. Consequently, h_1 will be flat at frequencies around ω_0

$$h_1({\rm s}) = \frac{R_{\rm in1}}{R_1 + R_{\rm in1}} \frac{({\rm s C_1 R_2} + 1)}{{\rm s C_1 R_T} + 1} \xrightarrow{\omega = \omega_0} \frac{R_2}{R_1} \tag{17}$$

where $R_{\rm in1}$ is input resistance of the summing amplifier A_1 of Fig. 5. R_1, R_2, C_1 are the filter network components (Fig. 8) and $R_{\rm T} = R_1 \| R_{\rm in1}$.

IV. Simulation and Experimental Results

A prototype SA-CFPPRI was designed, simulated, built and tested experimentally (a detailed circuit diagram is given in Fig. 9). The simulation was carried out on a SPICE compatible behavioral model of the system using PSPICE/ORCAD (Cadence, USA) (Evaluation version 9.2). The modeling approach [12] was to describe the non-linear subsystems by large-signal dependent sources that emulate the functional relationships of the elements.

The target parameters of the experimental units were: Input voltage: 11 VDC; Output voltage: $V_{\rm out}$ = 160 Vrms; Nominal output power: 5 W; Load capacitance range: C_L = 1.1 nF–9.1 nF; Frequency range: $f_{\rm in}$ = 80 kHz–150 kHz.

Transformer characteristics were: Core type: ETD29; Magnetizing inductance (secondary side): L_m =1.5 mH; Turns ratio: $n_2 : n_{11} = n_2 : n_{12} = 3{:}20; n_3 = 80$ turns. The inner current loop was designed to have a bandwidth of 6 kHz. The over all closed loop response of the system was designed to have a bandwidth of about 3 kHz with a nominal output capacitance of 2.1 nF at a carrier frequency of 93 kHz.

Typical waveforms of the experimental unit are given in Fig. 10. The operational range of the prototype is summarized

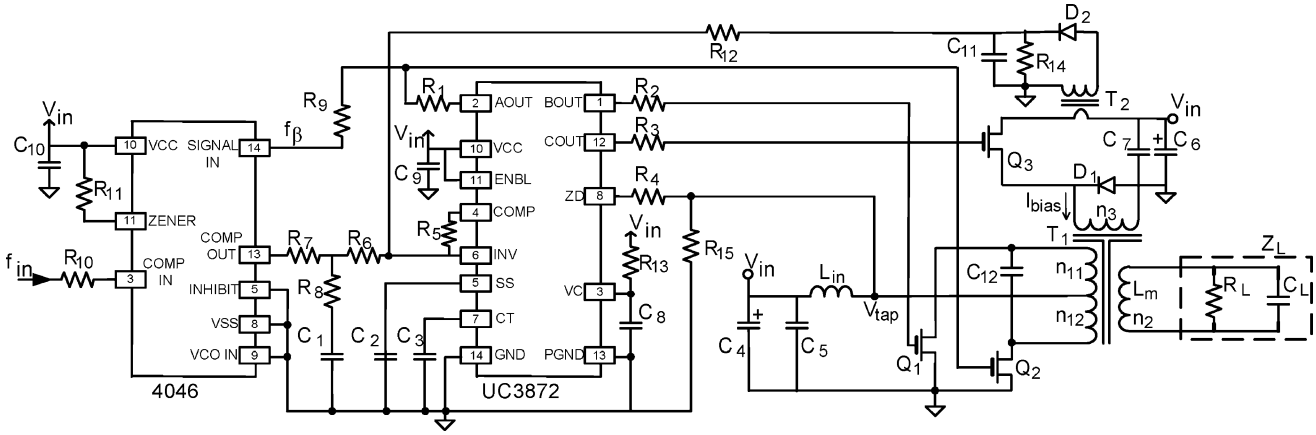


Fig. 9. Complete experimental circuit setup.

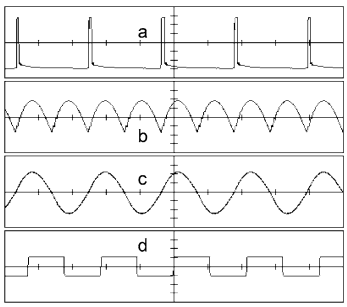


Fig. 10. Experimental results. (a) Control pulses to bias Buck converter (2V/div). (b) Tap voltage (5V/div). (c) Output voltage (100 V/div). (d) Input frequency signal (5 V/div). Horizontal scale 5 μs/div.

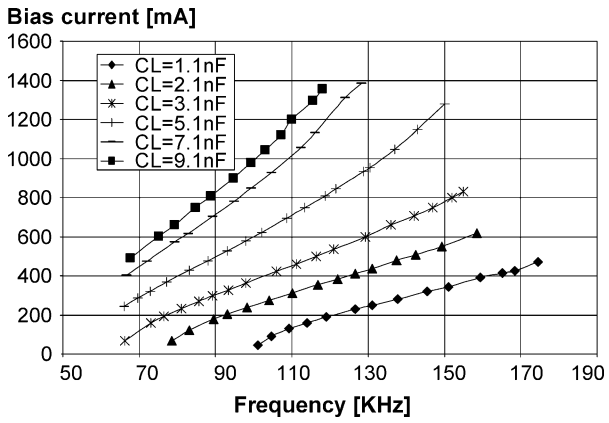


Fig. 11. Measured bias current as a function of operating frequency for various load capacitances of experimental unit.

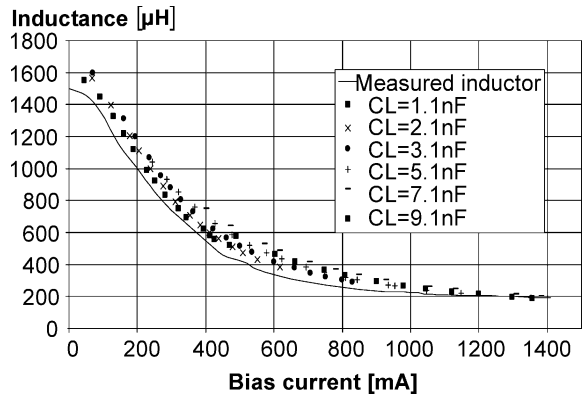
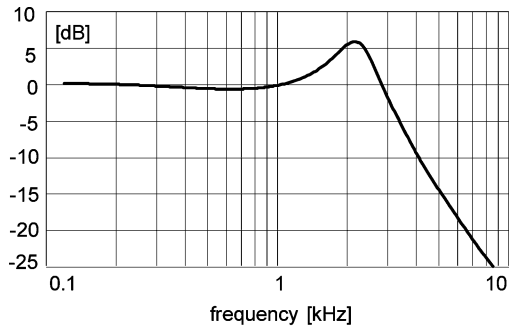
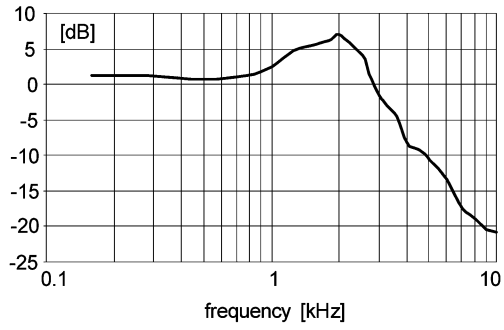


Fig. 12. Inductance of variable inductor as a function of bias current. Measured (solid line) and calculated from experimental results.



(a)



(b)

Fig. 13. (a) Calculated and (b) measured overall closed loop response ($f_\beta/f_{\rm in}$).

in Fig. 11. The experimentally measured bias currents and their corresponding calculated inductances are given in Fig. 12. The closed loop response of the system was measured and cross checked by simulation for two cases: (a) ac response $f_\beta/f_{\rm in}$ (Fig. 13) and (b) step response (Figs. 14 and 15). A very good agreement was obtained between the simulation results and the laboratory measurements.

The efficiency of the experimental unit (taking into account the total input power to power stage and control section) was found to be about 67% when the inductors bias current was low

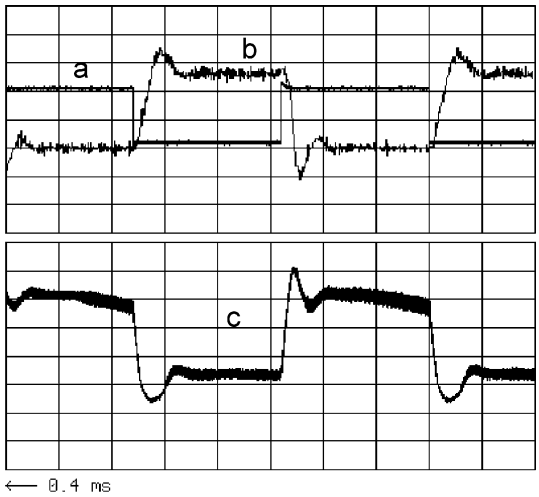


Fig. 14. Measured response of experimental unit to a step in input frequency around 93 KHz (with output capacitance of 2.1 nF). (a) Modulating signal. (b) Output frequency change (1.56 kHz/div). (c) Error signal at the output of phase comparator filter (H_1) of Fig. 5 (20.5 mV/div). Horizontal scale: 1 ms/div. (b) was measured the frequency jitter (Jfreq) feature of the Lecroy WaveRunner digital oscilloscope.

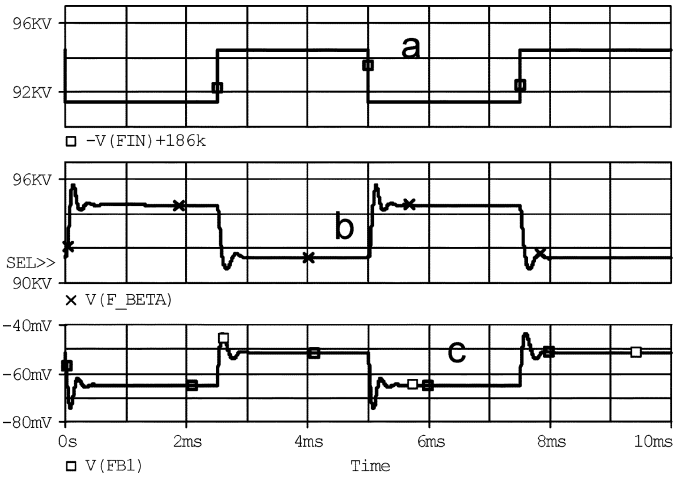


Fig. 15. Simulated response of experimental unit to a step in input frequency around 93 KHz (with output capacitance of 2.1 nF): (a) modulating signal, (b) output frequency change, and (c) error signal at the output of phase comparator filter (H_1) of Fig. 5.

and about 52% when the variable inductor was forced to its minimum value (highest bias current).

V. Conclusion

The proposed SA-CFPPRI was shown to be able to drive variable capacitive loads under ZVS for any drive frequency (within the operation range of the design). For a variable inductor that can be controlled over some m:1 ratio, the range of allowed load capacitor variation that the SA-CFPRRI will accommodate is also about m:1. It is expected that the system should be able to drive inductive loads as long as the variable inductor can be controlled to keep the tank in resonance for the given drive frequency. Amplitude control can be easily incorporated by another Buck stage that will feed the input series inductor. The operating frequency range of the system can be adjusted by selecting the nominal value for the variable inductor.

The reactive power of the system, circulating in the tank (but not passed by the transistors) is a function of the quality factor Q of the system that is, $\omega_s L/R_L$. For proper operation, Q should be relatively high $(Q > 5)$. It implies that this approach is perhaps limited to low up to medium power (hundreds of Watts) and may not be practical to high power applications due to the very high currents that need to be handled by the tank. This is especially true for high operating frequency because the size of high frequency high current inductor will be large given the available core materials. This situation, however, is not different from that of any other resonant inverter.

A possible application of proposed SA–CFPPRI includes drivers for piezoelectric motors. The advantages of using SA–CFPPRI in this case are: the generation of a sinusoidal wave with low distortion, the ability to compensate for device capacitance changes and interconnecting cables capacitances, and the relatively high efficiency. The latter is due to the fact that the resonant current is locked at the secondary and does not pass through the switches, and the fact that ZVS is automatically maintained. The over all efficiency measured for the experiment system is modest but is maintained constant over the whole frequency range. Without a self adjusting, controllable inductor, reasonable efficiency can be obtained at one frequency only—the frequency that matches the resonant frequency of the fixed inductor. At high frequencies, when the bias current needs to be high so as to lower the inductance, the efficiency is expected (and was measured) to drop due to increased losses of the bias section. The losses include two parts: copper losses of the bias winding and Buck converter losses. The relatively low efficiency that was observed at large bias currents is evidently due to converter losses. These can possibly be improved by a better design of the bias Buck converter. In particular, synchronous rectification and soft switching could be beneficial (see Appendix for a detailed design considerations and losses estimation of the bias section).

Another benefit of the SA-CFPPRI as a piezoelectric motor driver is the compatibility with optimizing control schemes. For example, by adding a frequency sweep arrangement one can lock to the optimal frequency in terms of efficiency, torque, or speed.

The proposed approach that is based on the variable inductor and the SSC circuitry could be useful in other applications, such as for driving an ac distributed system bus or driving resistive loads (e.g., fluorescent lamp) when the drive frequency needs to be constant or controlled.

Appendix
Power Stage Design Considerations

The following procedure is suggested for practical CFPPRI design. The proposed design approach is demonstrated by considering the following set of specifications. The solution for other design constraints, such as adjustable input/output voltage or changes in the load power, can be derived by following the same rationale.

a) Load specifications: Output power (P_L), rms output voltage (V_{out_rms}), nominal frequency (f_L), the range of frequency change$(f_{L_min} - f_{L_max})$, the nominal

capacitance of the load ($C_{\rm L}$) and the expected range of load capacitance ($C_{\rm L\_min} - C_{\rm L\_max}$).

b) Input voltage (dc) ($V_{\rm in}$).

A. Magnetizing Inductance (Secondary Side), L_m

Calculate the maximal (initial) inductance value (zero bias current), $L_{\rm m\_max}$, for the extreme operating point (minimal operating frequency, $f_{\rm L\_min}$, and lowest load capacitance, $C_{\rm L\_min}$)

$$L_{\rm m\_max} = \frac{1}{4\pi^2 f_{\rm L\_min}^2 C_{\Sigma\_\rm min}}. \tag{18}$$

In most practical cases, the range of inductance change, of controlled inductor (Fig. 4), is approximately 1:7. Check validity of design for minimal inductance scenario

$$\frac{L_{\rm m\_max}}{7} \geq \frac{1}{4\pi^2 f_{\rm L\_max}^2 C_{\Sigma\_\rm max}}. \tag{19}$$

If (19) does not hold, the initial specifications need to be changed.

B. Input to Output Voltage Ratio

The peak voltage at the primary side is given by [8]

$$V_{\rm pr\_pk} = \pi V_{\rm in}. \tag{20}$$

According to the load voltage demands, calculate the transformer's turns ratio by

$$n = \frac{V_{\rm out\_rms}}{\pi V_{\rm in}/\sqrt{2}}. \tag{21}$$

C. Transformer Design T_1

1) Resonant Current: The peak value of the resonant current circulating in the tank (secondary side) is given by

$$I_{\rm sec\_pk} = \frac{V_{\rm pr\_pk} \cdot n}{Z_{\rm r}} \tag{22}$$

where $Z_{\rm r} = \sqrt{L_{\rm m}/C_\Sigma}$ is the characteristic impedance of the parallel LC resonant network at the secondary.

Since the resonant frequency is locked to the switching frequency the resonant current, in present design, will be sinusoidal with rms value$I_{\rm sec_rms}$, of $1/\sqrt{2}$ the peak value.

The primary resonant current carries the input current and therefore

$$I_{\rm pr\_rms} = \frac{P_{\rm L}}{V_{\rm in}\eta} \tag{23}$$

where η is the expected efficiency, 70%–80% is a good starting point.

However, since a snubber capacitor (C_1) is placed across the primary (Fig. 1), some of the resonant current will circulate in the primary winding. Assuming that this current will be about 10% of the resonant current (is detailed in Appendix E), a better estimation of I_{pr_pk} will be

$$I_{\rm pr\_rms} \approx \frac{P_{\rm L}}{V_{\rm in}\eta} + 0.1 I_{\rm sec\_rms}. \tag{24}$$

2) Core Selection: Calculate the area product, $A_{\rm pdes}$, needed for magnetic element to comply with design specifications [inductance value (Appendix A) and resonant current (Appendix C.1)]

$$\begin{aligned} A_{\rm Pdes} &= A_{\rm e} A_{\rm w} \\ &\geq \frac{L_{\rm m\_max}\, I_{\rm sec\_pk}\left(\frac{1}{\rm n} I_{\rm pr\_rms} + I_{\rm sec\_rms}\right)}{\rm JKB_{max}} 1.3 \end{aligned} \tag{25}$$

where $A_{\rm e}, A_{\rm w}$ are the effective magnetic area and the window area of selected core, respectively. J is the current density in [$\rm A/m^2$], K is the fill factor (constant smaller than 1) and $B_{\rm max}$ [Tesla] is the maximal flux density allowed. The factor 1.3 takes into account the fact that the area product needs to be greater than the normally calculated $A_{\rm p}$ to ensure sufficient space for the bias windings, a ratio of 1:1.3 is a good starting point (to be verified in Appendix C.7).

3) Number of Turns and Wire Selection, Transformer Section: Once the practical core is selected, calculate

$$n_{\rm sec} = \frac{L_{\rm m\_max}\, I_{\rm sec\_pk}}{B_{\rm max} A_{\rm e}}. \tag{26}$$

Dividing (26) by (21) yields the number of turns of the primary

$$n_{\rm pr} = \frac{n_{\rm sec}}{n}. \tag{27}$$

For the secondary side calculate

$$A_{\rm wire\_sec} = \left(\frac{I_{\rm sec\_rms}}{J}\right). \tag{28}$$

For the primary side

$$A_{\rm wire\_pr} = \left(\frac{I_{\rm pr\_rms}}{\rm J}\right). \tag{29}$$

4) Air Gap, l_g: The required permeability that will produce the desired inductance $L_{\rm m\_max}$ according to the selected core's characteristics is

$$\mu_{\rm r} = \frac{l_{\rm e} L_{\rm m\_max}}{n_{\rm sec}^2 \mu_0 A_{\rm e}} \tag{30}$$

where $l_{\rm e}$ is the selected core's magnetic length in [m] and μ_0 is the permeability constant [1.26 10^{-6} H/m].

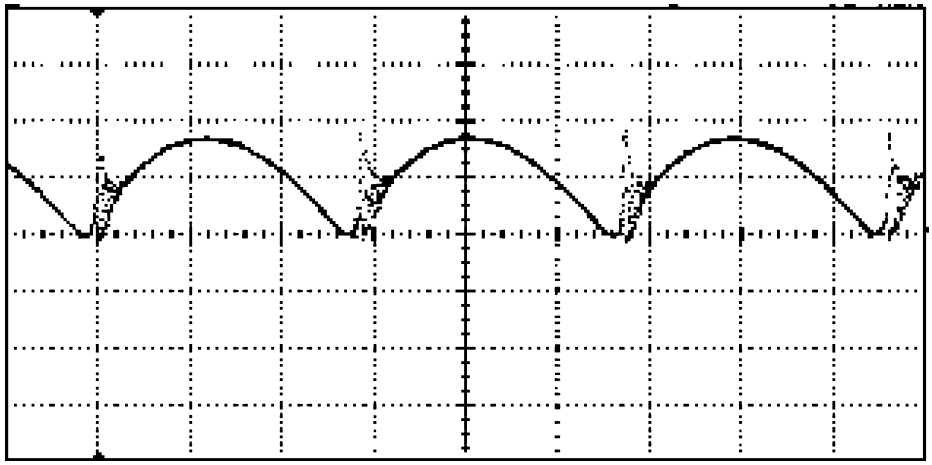


Fig. 16. Tap voltage (10 V/div) without snubbing capacitance (C_1) and no feed-forward network (R_4, $R15$ Fig. 9). Horizontal scale 2 μs/div.

The desired air gap is given by the approximate equation

$$l_{\rm g} = \frac{l_{\rm e}}{\mu_{\rm r}}. \tag{31}$$

Substituting (30) in (31) yields

$$l_{\rm g} = \frac{n_{\rm sec}^2 \mu_0 A_{\rm e}}{L_{\rm m\_max}}. \tag{32}$$

5) Number of Turns and Wire Selection, Bias Section: From the core manufacturer's data, determine the Amper-turn needed to saturate the core to its minimum value by

$$n_{\rm bias} \cdot I_{\rm bias} = H_{\rm max} \cdot L_{\rm e}. \tag{33}$$

It should be noticed that the copper losses of the bias winding $P_{\rm bias}$ are independent of $n_{\rm bias}$

$$P_{\rm bias} = \frac{(H_{\rm max} \cdot l_{\rm e})^2 \rho \ell}{A_{\rm wb}} \tag{34}$$

where $H_{\rm max}$ is the maximal magnetic flux of selected core material in [A/m] obtained from manufacturer's data, $A_{\rm wb}$ is the bias window area in $[m^2]$, ρ is the specific resistance of the wire material and ℓ is the average wire length of one turn.

Equation (34) implies that for a given bias window area, $A_{\rm wb}$, the copper losses can be considered constants. If lower bias wire losses are required one has to increase A_w.

Select the number of turns, taking into account that fewer turns of the bias winding will cause a high bias current to saturate the core, increasing the conduction losses of the buck type bias driver. On the other hand, when applying many turns, insulation between layers of turns is essential to handle the high voltage induced.

Once the number of turns is selected, the wire area needed can be calculated by

$$A_{\rm wire\_bias} = \left(\frac{n_{\rm bias} I_{\rm bias\_rms}}{K_{\rm B} A_{\rm wb}} \right) \tag{35}$$

where $K_{\rm B}$ is the fill factor of the bias winding.

D. Input Inductance, $L_{\rm in}$

To comply with the demand of a current-source like input [8], [11], the input impedance of $L_{\rm in}$ must be much larger than the maximal resonant inductance reflected to the primary [8]

$$L_{\rm in} >> \frac{L_{\rm m\_max}}{4n^2}. \tag{36}$$

In the case that the selected input inductance value does not follow the current sourcing criterion of (36), then the calculation of the resonant tank frequency must take into account the error adjustment due to small input inductance [8] given by

$$f_{\rm r} = \frac{1}{2\pi\sqrt{L_{\rm m} C_\Sigma}} \sqrt{1 + \frac{L_{\rm m}}{{\rm n}^2 L_{\rm in}}}. \tag{37}$$

E. Snubbing Capacitance, C_1

The capacitor C_1 is used in the proposed design (C_{12} in Fig. 9) to reduce the parasitic oscillation that may follow the commutation instance due to leakage inductance and the switches' parasitic capacitances at the primary side of the CFPPRI (Fig. 16). Parasitic ringing will be observed if the leakage inductance current is not zero (due to phase lag and internal delays of the control circuitry) at the commutation instance. When the switches commutates, C_1 locks the leakage inductance current reducing thereby the voltage spikes. However, placing a capacitor across the primary will cause some of the resonant current to circulate in the primary, increasing copper losses of the winding. A good compromise for C_1 selection will be to allow the primary current to carry about 10% of the resonant current

$$C_1 \approx \frac{C_\Sigma n^2}{10}. \tag{38}$$

An additional remedy to reduce the parasitic oscillations due to the leakage inductance current is to make sure that the commutation instance occurs when the primary current is close to zero. This can be accomplished by applying a feed-forward path connection to the zero detection (ZD) node of the SSC [13] (R_4

and R_{15} in Fig. 9) which adjust the commutation time to coincide with the time that the primary current passes through zero. The resulting improvement can be observed in the experimental waveforms of Fig. 10 which was compared to Fig. 16 where neither snubbing capacitance C_1 nor feed-forward path were applied.

F. Power Switches Stresses

1) Voltage: The transistors will absorb the highest voltage when the resonant tank voltage at its peak value

$$V_{\mathrm{DS\_max}} = V_{\mathrm{pr\_pk}} = \pi V_{\mathrm{in}}. \tag{39}$$

2) Current: Since the switching frequency is equal to the resonant frequency, the high-rated resonant current is locked in the tank and does not pass thru the switches. Assuming that the input inductance is sufficiently large (Appendix D), the switches current stress will be

$$I_{\mathrm{Q}} = \frac{P_{\mathrm{L}}}{\eta V_{\mathrm{in}}}. \tag{40}$$

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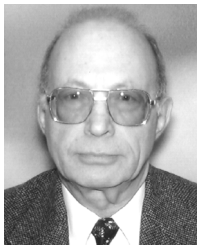

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