A High-Efficiency Resonant Switched Capacitor Converter With Continuous Conversion Ratio

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***Abstract*—A resonant switched capacitor converter with high efficiency over a wide and continuous conversion ratio range is introduced. The efficiency of the topology depends primarily on the conduction losses and is decoupled, to a large extent, from the voltage conversion ratio. This is an advantage over classical switched capacitor converters, for which the efficiency is strongly related to the conversion ratio. The operation principle applies three zero current switching states to charge, discharge, and balance the remaining charge of the flying capacitor. This results in a gyrator, i.e., a voltage-dependent current source, with a wide range of voltage conversion ratios (smaller as well as greater than unity) as well as bidirectional power flow capabilities. The analytical expressions for the conversion ratio and expected efficiency are provided and validated through simulations and experiments. The experimental verifications of the converter demonstrate peak efficiency of 96% and above 90% efficiency over a wide range of voltage gains and loading conditions. In addition, the system was found to be highly efficient at the extreme cases of both light and heavy loads.**

***Index Terms*—current control, digital control, gyrators, pulse modulation, switched capacitor circuits, switched mode power supplies.**

I. Introduction

SWITCHED capacitor converters (SCCs) have limited capabilities for voltage regulation due to the tight relationship between the voltage gain and the converter efficiency [1]–[9]. In such converters, the efficiency is tied to the ratio of the output voltage, V_O, to target voltage, V_T (the no load SCC output voltage), which stems from the rigid proportionality between the input and output charges [1]–[9]

$$\eta = \frac{V_O}{V_T}. \tag{1}$$

Regulation can be obtained either by varying SCC parameters, or inserting a post regulation stage [10]–[12] to match the required conversion ratio. A more sophisticated approach for voltage regulation by SCC is to generate multiple conversion ratios and, therefore, increase the effective operation range [4], [6]–[13]; the system efficiency, however, would remain of a discrete nature. The multiple conversion ratios approach has shown advancement in the utilization of SCC, in particular as a high-efficiency first-stage converter that may be followed by a reduced size local regulator [10]–[12].

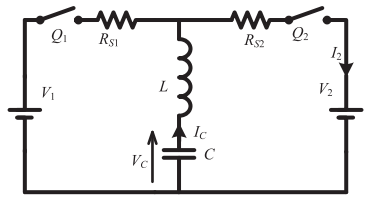

Fig. 1. Conventional 1:1 RSCC. The resistors, R_{S1} and R_{S2}, represent loop series resistances, V_1 and V_2 represent the input and output potentials.

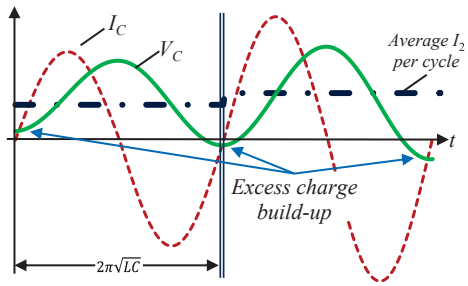

Fig. 2. Typical waveforms of the flying capacitor in the RSCC. The signals are described in Fig.1.

Resonant switched capacitor converter (RSCC) operation with zero current switching (ZCS) has been described in [14]–[22] with the aim to reduce the switching losses, allowing higher switching frequency operation, potentially reducing the total volume of the converter. There, high efficiency is still obtained for discrete conversion ratios.

The main challenge to create an output voltage that is different from the target voltage, in soft-switched SCC, is that the resultant charge balance of the flying capacitor(s) after a charge/discharge cycle is not zero. The residual charge left in the flying capacitor(s) prevents the system from converging to the desired voltage. This excess charge eventually increases/decreases the output voltage such that the charge balance of all the capacitors will be satisfied which will drift the system off from the desired operation point. To better view this problem, consider a generic 1:1 RSCC (see Fig. 1) with a desired output voltage of 0.8. The flying capacitor voltage and current are illustrated in Fig. 2. The current waveform shows that although ZCS is obtained, the charge received from the source is not equal to the one delivered to the output. This translates into an unbalanced capacitor voltage that continues to rise in every cycle.

The conventional method that is applied in commercial applications [23] to manage the residual charge of the

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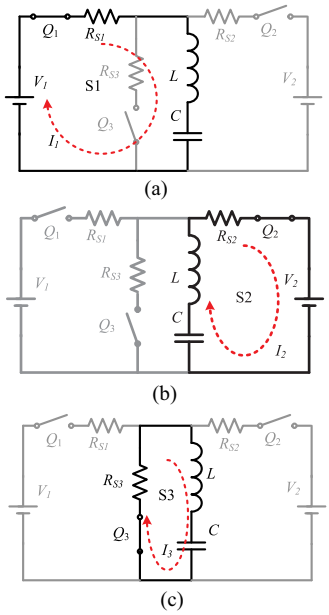

Fig. 3. Introduced RSCC configuration and operation principle: (a) *charge,* (b) *discharge,* and (c) *balance* states.

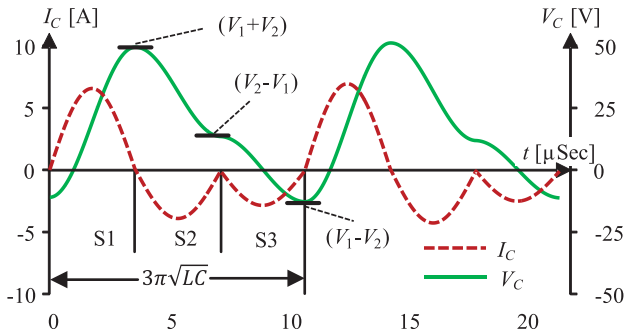

Fig. 4. Typical waveforms (obtained from simulation) of the flying capacitor voltage and current. The circuit parameters are $V_1 = 20$ V, $V_2 = 31$ V, $R_S = 0.15\ \Omega$, $L = 5.2\ \mu$H, $C = 0.25\ \mu$F.

capacitor and allow regulation is by introducing series losses. A more sophisticated approach would be to introduce an additional, lossless, charge/discharge path to satisfy the capacitor charge balance. The latter was adopted in this study.

Studies with seemingly similar concept of circulating the residual charge were recently described in the literature with various realizations. In [24], a topology with an additional switching stage to internally circulate the charge is described. It is named "Sneak Circuit State," to emphasize an inherent feature of the original RSCC configuration. Additional circuitry to circulate the charge was practiced in [25] and [26]. There, the operation of the converter was set above the resonant frequency exhibiting inductive behavior. This allows reversing the inductor current using phase-shift control, which also regulates the power flow direction. In this case, however, soft switching cannot be guaranteed for the entire operation range. The work of Jabbari [27] combines resonant and linear operations to completely discharge the energy of the *LC* tank in every switching cycle. There, the direction of the power flow is still dictated either by the system configuration or by the source of the higher potential.

The objective of this study is to introduce a new RSCC (see Fig. 3) *that disengages the efficiency of the system from the voltage gain*. By doing so, the converter efficiency may be very high and depends primarily on the conduction losses. The converter operates as a voltage-dependent current source, maintains soft switching for the entire operation range, and exhibits bidirectional power flow with wide voltage gains.

The converter in its simplistic form, presented in Fig. 3, is a modification of a soft-switched SCC [2], [3], [5], [28]–[31]. Like the classical design, it includes two switches and a resonant tank. The additional switch S_3 is added to introduce an alternative resonant path of the current to balance the residual charge of the flying capacitor, i.e., it restores the flying capacitor voltage to its original state by reversing its polarity. The mechanism of polarity reversal (charge balancing) lays the foundations to break the rigid connection of input/output voltage and efficiency dependency. Controlling the sequence of the switches governs the power flow direction, hence bidirectional step up/down operation.

II. Principle of Operation

The topology in its generic form, as described in Fig. 3, requires four-quadrant (bidirectional) switches (Q_1, Q_2, and Q_3) that operate in synchronous/complementary action. This is required to support bidirectional and noninverting step up/down operations in a single configuration. However, for more specific cases, such as unidirectional power flow and/or specific conversion types (up or down), the number of switches and the configuration complexity can be significantly reduced. A detailed discussion of the topology derivatives is provided in Section VI.

The operation of the converter shown in Fig. 3 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 4 that illustrates the capacitor voltage V_C and the resonant tank current I_C for the case of a nonunity step up conversion. By turning Q_1 ON, a charge state (S1) is commenced, which resonantly charges the flying capacitor from the input V_1. At zero current, Q_1 is turned OFF and Q_2 is turned ON (state S2). At this point, the flying capacitor resonantly discharges onto the output capacitor. Since the input voltage V_1 and the output voltage V_2 are of different values, only a portion of the charge is delivered to the output and results in V_C that is different to its voltage at the starting point of S1. The amount of this voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning Q_3 ON (S3), the resonant tank is short-circuited. This creates the required charge balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.

As will be explained in detail in the next section, the addition of a third, charge-balancing state to the switching sequence transforms the RSCC into a voltage-dependent current sourcing converter. This leads to an optimal result, where the current that

is output by the current source is injected into the load, thus adjusting the voltage at the output, while keeping it independent of the conversion ratio. With the new topology, dependency is formed between the input voltage V_1 and the output current (rather than the output voltage). In this way, any desired conversion ratio may be obtained (i.e., the conversion ratio becomes continuous), while maintaining high efficiency. It should be noted that under steady-state conditions, the order of the charge/discharge/balance sequence does not affect the operation of the converter for either step up or step down conversion. The order of the sequence will govern the power flow direction, i.e., from V_1 to V_2 or from V_2 to V_1. To deliver power from V_1 to V_2 the sequence will be (S1, S2, S3). That is, *charge* from V_1, *discharge* on V_2 and *reverse* the flying capacitor polarity. In the case of power to be delivered from V_2 to V_1, the sequence will be changed to (S1, S3, S2). The duration of each switching state is half the resonant period, and hence, the switches are turned ON and OFF at ZCS. Voltage regulation may be applied by introducing a time delay between switching states, applying a delay between consecutive sequences, i.e., pulse density modulation (PDM), or by creating packets using ON–OFF burst mode control [6], [27]. The resistors R_S in Fig. 3 represent the parasitic resistances in each loop and are assumed to be negligibly small in the analysis for the current and voltage conversion ratios.

III. Gyrator Mode Power Transfer

In each switching state, the *LC* tank connects to a voltage potential of either V_1 or V_2 or 0. Assuming a high quality factor ($Q \gg 1$) of the resonant tank, the resonant current I_C and the flying capacitor voltage V_C are approximately sinusoidal; hence

$$V_C(t) \approx V_i - (V_i - V_C(0))\cos\left(\frac{t}{\sqrt{LC}}\right) \tag{2a}$$

$$I_C(t) \approx \frac{V_i - V_C(0)}{\sqrt{L/C}}\sin\left(\frac{t}{\sqrt{LC}}\right) \tag{2b}$$

where C is the value of the flying capacitor and L is the series inductance. $t = 0$ represents the start of each switching state and V_i represents the dc voltage, either V_1 or V_2 or 0 V.

Following the principle of operation described earlier, assuming steady-state operation with transition between switching states at zero current, and by using (2a), the voltages at the end of the charge, discharge, and balance states can be expressed as

$$\begin{cases} V_{C,1} \approx V_1 + (V_1 - V_{C,3}) = 2V_1 - V_{C,3} \\ V_{C,2} \approx V_2 + (V_2 - V_{C,1}) = 2V_2 - V_{C,1} \\ V_{C,3} \approx 0 + (0 - V_{C,2}) = -V_{C,2} \end{cases} \tag{3}$$

where $V_{C,1}$ to $V_{C,3}$ represent V_C at the end of stages S1 to S3, respectively. After some manipulation, (3) can be rewritten as

$$\begin{cases} V_{C,1} = V_1 + V_2 \\ V_{C,2} = V_2 - V_1 \\ V_{C,3} = V_1 - V_2. \end{cases} \tag{4}$$

Substituting (2b) into (4) yields the states' peak resonant currents ($I_{pk,\mathrm{S1}}, I_{pk,\mathrm{S2}}, I_{pk,\mathrm{S3}}$)

$$\begin{cases} I_{pk,\mathrm{S1}} = V_2/Z \\ I_{pk,\mathrm{S2}} = V_1/Z \\ I_{pk,\mathrm{S3}} = (V_1 - V_2)/Z \end{cases}, \quad Z = \sqrt{\tfrac{L}{C}}. \tag{5}$$

Assuming identical resonant characteristics for all states, that is, a 1/3 of the operation cycle for each state, the average input and output currents (I_1, I_2) can be obtained and a gyrator relationship between the currents (I_1, I_2) and voltages (V_1, V_2) is formed as follows

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \; g = g_n = \frac{2}{3\pi Z}. \tag{6}$$

Equation (6) shows that for a synchronously run converter, the dependence of the average terminal currents (I_1, I_2) on the average terminal voltages (V_1, V_2) follows a gyrator relationship [32], [33] with a natural gyration gain of g_n. This expression is generic and holds for the case of power flow from V_1 to V_2 as well as for power flow from V_2 to V_1. However, as mentioned earlier, the direction of power flow is governed by the switching stage sequence and reverses for the case of (S2, S1, S3). It should be further noted that due to the gyration action, the converter behaves as a voltage-dependent current source and there is virtually no restriction on the relative magnitudes of V_1 and V_2. That is, V_2 can be equal to, less than, or greater than V_1.

For the case where one of the terminals are loaded by a resistive load R_L in parallel with a filter capacitor C_L the gyrator RSCC (GRSCC) operates as a current sourcing dc–dc converter and the magnitude of the output voltage V_2 depends on the load resistor as would be expected from a gyrator circuit

$$V_2 = gR_L V_1. \tag{7}$$

The voltage gain A will be

$$A = \frac{V_2}{V_1} = gR_L. \tag{8}$$

The natural operating frequency f_n is composed of three half-resonant sections, which are assumed identical. Therefore, f_n can be expressed as

$$f_n = \frac{1}{3\pi\sqrt{LC}}. \tag{9}$$

IV. Fundamental and Practical Characteristics

A. Voltage Regulation

The basic operation mechanism that follows a charge, discharge, and balance states creates a rigid gyration relationship as in (6). In the case that voltage regulation is desired, g should be controlled. By introducing time delay between cycles, that is, effectively changing the operating frequency, g is made controllable and the gyration ratio g and operating frequency can be redefined as

$$g = Gg_n = \frac{2G}{3\pi Z} \tag{10a}$$

$$f_s = Gf_n = \frac{G}{3\pi\sqrt{LC}} \tag{10b}$$

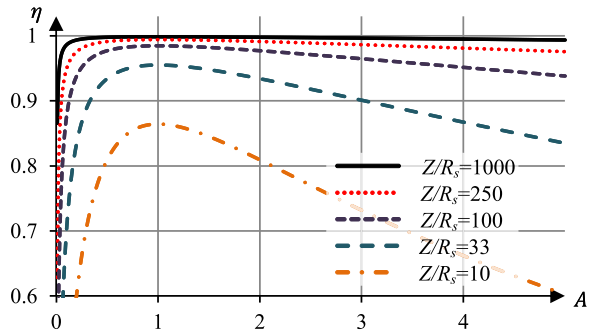

Fig. 5. Theoretical efficiency curves as a function of the voltage gain A with R_S normalized by Z as a parameter.

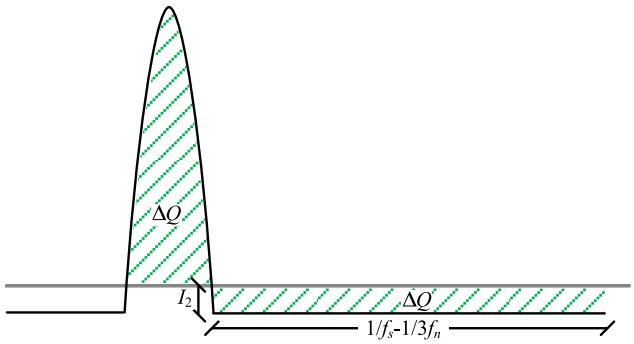

Fig. 6. Current on the output capacitor C_L for one cycle. The confined area is symmetrical above and below zero and represents the charge processed by C_L at each cycle.

in which $G \in (0,1]$ is defined as the regulation factor. In this mode of operation, the output current will be determined by the input voltage and g.

B. Losses and Efficiency

Assuming ZCS, the losses of the converter are primarily due to resistive elements in the conduction paths of each subcircuit. For a full operation cycle at frequency f_s, the current of each subcircuit is composed of one sinusoidal pulse [with a peak value as found in (5)] followed by zero current for the time duration of the delay plus the conduction time of the other two states. Assuming that the output current is constant and neglecting the voltage ripple, the relationship between the rms currents and the average output current I_2 will be

$$\begin{cases} I_{\mathrm{rms,S1}} = \sqrt{\frac{G}{6}}\frac{R_L}{Z} I_2 \\ I_{\mathrm{rms,S2}} = \frac{3\pi}{2}\frac{1}{\sqrt{6G}} I_2 \\ I_{\mathrm{rms,S3}} = \left| \frac{3\pi}{2}\frac{1}{\sqrt{6G}} - \sqrt{\frac{G}{6}}\frac{R_L}{Z} \right| I_2. \end{cases} \tag{11}$$

The total power dissipation can be calculated by summation of the losses of the three subcircuits. Given an identical parasitic resistance R_S for the three subcircuits, the total dissipated power P_{loss} can be expressed as

$$P_{\mathrm{loss}} = I_2^2 \left(\frac{3\pi^2}{4G} + \frac{R_L^2 G}{3Z^2} - \frac{\pi R_L}{2Z} \right) R_S. \tag{12}$$

By substituting (6), (8), and (10a) into (12) and after some manipulations, the equivalent resistance of the converter R_e [2], [3] as a function of the load, voltage ratio, and the circuit parameters is found to be

$$R_e = R_L \frac{\pi}{2} \frac{R_S}{Z} \left(A + A^{-1} - 1 \right). \tag{13}$$

The efficiency of the converter η can now be estimated by

$$\eta = \frac{R_L}{R_L + R_e} = \frac{1}{1 + \frac{\pi R_S}{2Z}(A + A^{-1} - 1)}. \tag{14}$$

Fig. 5 shows typical curves that were obtained from (14) for the expected efficiency as a function of A, for various ratios of $Q{=}Z/R_S$. As can be observed, maximum efficiency is obtained at unity gain $(A = 1)$, and it is a function of the ratio between the resistance and the resonant network characteristics. In Fig. 5, Z has been assumed as constant since it is determined by the natural gyration gain g_n. Expression (14) also implies that the efficiency is independent of G, resulting in a constant efficiency in a voltage regulation mode, when the current is controlled.

Equation (14) and Fig. 5 provide an insight into the operation of the new RSCC-based gyrator converter as well as to the contributing factors of the efficiency. Ideally, assuming negligibly small parasitic resistances, the efficiency of the converter would be 100% *for any finite conversion ratio*. A unique feature hitherto only found in switched-inductor converters is now made available to RSCCs as well.

C. Output Voltage Ripple

Considering the above analysis, the operation of the converter presented in this paper resembles the discontinuous-current-mode pulsed frequency modulation (PFM) operation of conventional switch-mode converters, which are predominantly found as voltage regulators. In this context, estimation of the output voltage ripple is essential for sizing considerations of the output filter. By following the same design rules applied to switch-mode regulators [34], [35], that is, assuming constant output current, the current of the output capacitor (C_L) is similar in shape to the current of the discharge state, but without the average dc offset.

A generic waveform of the output capacitor current is shown in Fig. 6. By approximating the negative part of the current shape, the per-cycle charge transfer ΔQ_{C_L} can be expressed as

$$\Delta Q_{C_L} \approx I_2 \left(\frac{1}{f_s} - \frac{1}{3f_n} \right). \tag{15}$$

Substituting (7), (8), and (10) into (15) yields the expression for the normalized output ripple

$$\frac{\Delta V_2}{V_2} = \frac{1}{A} \frac{C}{C_L} \left(1 - \frac{G}{3} \right) \tag{16}$$

where ΔV_2 is the amplitude of the output ac ripple. The output ripple, as obtained by (16), is inverse linearly dependent on C_L and A. Furthermore, when voltage regulation is employed by varying G, the ripple is expected to deviate by about 30% for the entire operation range of $G \in (0,1]$.

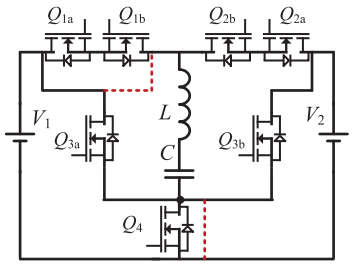

Fig. 7. Gyrator converter in a generalized configuration, with optimized efficiency at voltage gains of $A = \{2,1,0.5\}$. The dashed lines represent alternative routes optimized for a 1:1 configuration.

TABLE I
SWITCH MAPPING FOR UNIDIRECTIONAL DERIVATIVES[1]

Converter Function	Q_{1a}	Q_{1b}	Q_{2a}	Q_{2b}	Q_{3a}	Q_{3b}	Q_4
Step up/down[2]	1	D	2	2	3	O	S
Step up[2]	1	D	D	S	3	O	S
Step down[2]	1	D	D	2	D	O	S
Doubler step up/down	S	3	D	S	3	O	1
Doubler step down	S	D	D	S	3	O	1
Divider step up/down	1	S	S	2	O	3	2
Divider step down	1	S	S	2	O	D	2

[1]Characters in the table represent the following: S—MOSFET is shorted, O—MOSFET is disconnected, D—only a diode is needed. Numbers represent the stages in which the MOSFETs are active.

[2]Dashed route is preferred, but not mandatory. Mapping was suggested correspondingly.

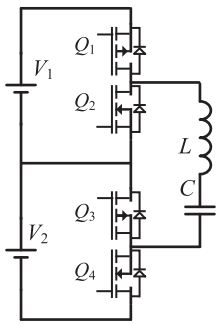

Fig. 8. Gyrator converter realized in full-bridge configuration, with optimized efficiency at voltage gain of $A = -1$.

V. TOPOLOGY DERIVATIVES

The converter of Fig. 3 may be extended to operate in naturally doubling and dividing configurations, i.e., shifting the peak efficiency points to $A = 2$ or $A = 0.5$, respectively. Fig. 7 shows a general topology that is capable of operating bidirectionally at all gains, with the capability of shifting the peak efficiency points. Table I summarizes the possible switch realizations for seven different unidirectional conversion modes, describing which switches can be either bypassed (S-Shorted), disconnected (O-Open) or replaced by a diode (D). Another attractive option that has voltage inversion properties may also be implemented as a bridge configuration (see Fig. 8). Possible state-of-the-art applications for the bridge configuration can be as a balancer/equalizer of energy cells [25], [26] or photovoltaic arrays [29]–[31]. It was found that for the bridge configuration, the four-quadrant switches can be replaced by conventional MOSFETs, while retaining the converter characteristics. As a consequence, the switch count required for the converter is a total of four switches, comparable to conventional RSCC or noninverting buck-boost configuration.

It should be noted that for configurations that are implemented with two-quadrant switches, such as the bridge assembly (see Fig. 8), the insertion of a time delay between states for voltage regulation purposes has to be assigned to the proper state to avoid undesired circulating current. The delay should be located between states such that V_C is at the correct polarity to block the conduction of the MOSFET diodes. Taking the bridge configuration for example (see Fig. 8), the proper sequence for this case would be: *discharge* (S2), *balance* (S3), *charge* (S1), *delay*. It should be noted that, as analyzed above, the order in which the sequence is applied does not affect the characteristics of the converter.

VI. PRACTICAL IMPLEMENTATION AND PERFORMANCE EVALUATION

A. Switch Control and Pulse Density Modulation

As mentioned earlier, voltage regulation is facilitated by introducing a time delay between switching cycles and by doing so the gyration ratio g is made controllable (10). The resultant switching sequence per cycle therefore includes three virtually constant time intervals (neglecting parameters variations) for the charge, discharge, and the balance phases (S1, S2, S3), and a fourth variable time frame for the PDM delay. One way to realize this pulse density modulated sequence is by synchronizing independent counters per interval, which is a relatively complex task for conventional off-shelf digital controllers. In this study, a simplified approach to implement PDM using readily available features of popular microcontrollers, without sacrificing the accuracy of the fixed intervals (to assure ZCS), has been realized. Here, similar to the control operation of resonant converters, the total cycle period is the control variable rather than the residual time delay.

Conventional microcontrollers such as [36] feature a PWM peripheral with multiple channels capable of operating synchronously (i.e., sharing a master period setting) with independent on time and phase delay. PDM realization based on these attributes is depicted in Fig. 9(a) for the basic configuration and in Fig. 9(b) for the bridge version. As can be observed, each gate is linked to an independent PWM channel sharing the same period T_s (f_s^{-1}). For each channel, the on time t_i and the phase-shift (negative) ϕ_i are assigned to create the desired sequence (i is the switch index). The specific time settings per channel are summarized in Table II. The time delay is the result of the time difference between the period (the control variable) and the switches' conduction time, that is,

$$T_d = T_s - 3T,\ T = \pi\sqrt{LC}. \tag{17}$$

As can be seen in Fig. 9 (b), for the special case of the bridge configuration, the switching sequence applies (S2, S3, S1) by overlapping the gate commands. Then, the required time delay is introduced. This is done to avoid reverse conduction paths due to negative potential of the flying capacitor that may result in

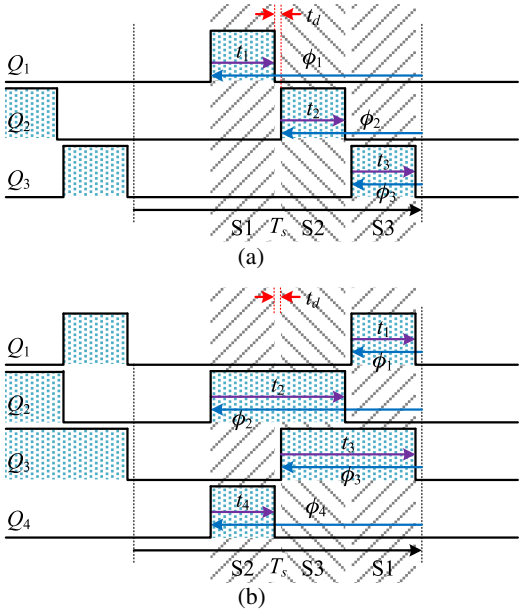

Fig. 9. Timing diagrams for the switching sequences of the GRSCC: (a) Basic configuration (see Fig. 3). (b) Bridge realization (see Fig. 8).

TABLE II
TIME SETTINGS FOR ON TIMES AND PHASE DELAYS OF FIG. 9

	t_1	t_2	t_3	t_4	φ_1	φ_2	φ_3	φ_4
Fig. 9a	T	T	T		3T	2T	T	
Fig. 9b	T	2T	2T	T	T	3T	2T	3T

undesired conduction of the antiparallel diodes. Another benefit of this timing sequence is its compatibility to the conventional on time setting of the PWM periphery.

B. Inductor Design

The inductor, although having a small inductance value, has to sustain relatively high rms currents. However, in contrary to the magnetics design in switched-inductor converters, the per-cycle energy that is stored in the inductor is zero. As a result, the main factor of the inductor sizing stems from the core losses, rather than saturation limits. A convenient way to estimate the volume of the magnetic element is by the area product A_p, which can be expressed as

$$A_p = \frac{L\Delta I I_{\rm rms}}{JK\Delta B} \tag{18}$$

where L is the desired inductance, ΔI is the maximum current variation through the inductor, ΔB is the maximum flux density variation due to ΔI, J is the current density that is allowed through the winding, and K is the fill factor.

For the particular case of the GRSCC, after some manipulations, (18) can be rewritten as

$$A_p = \frac{\max(V_1, V_2) I_{\rm rms}}{3\pi JK\hat{B} f_{\max}} \tag{19}$$

where $\hat{B}$ is the allowed peak flux density.

Using a ferrite core, the area product of the inductor needed for the GRSCC described in the example above is relatively large. The resultant A_p is found to be comparable with an inductor for a buck-boost converter, designed according to the same specifications, operating in continuous conduction mode (CCM). However, since the inductance value that is required for the GRSCC is quite low (e.g., 0.5 μH at 100 kHz), a rod configuration or a ferrite-less (i.e., air core) construction are feasible. Consequently, higher $\hat{B}$ is allowed, resulting in a significantly smaller A_p. A normalized comparison between the required area products for various converter topologies and operation modes has been carried out and is summarized in Table III. A significant reduction of the inductor volume can be noticed for a GRSCC-based design by one-order of magnitude, when compared to a buck-boost of the same features. Table III also provides inductance estimation for operation at specific frequency of 100 kHz.

TABLE III
COMPARISON OF THE AREA PRODUCT, A_p, BETWEEN VARIOUS CONVERTERS DESIGNED FOR VOLTAGE REGULATION

	Buck-boost		**Buck**	**GRSCC**		
	CCM	***BCM*** [a]	***BCM*** [a]	***Full core***	***Rod***	***Air***
$\tilde{A}_P$ [b]	50	10	10	40	10	1
$\hat{B}$ [T]	0.2	0.2	0.2	0.05	0.2	2
L [μH] at 100kHz	35	5	10	0.5	0.5	0.5

[a] Boundary Current Mode.
[b] Normalized to GRSCC with air core.

C. Efficiency Comparison of the GRSCC With a Switched-Inductor Buck-Boost Converter

To evaluate the efficiency features of the GRSCC, a comparative analysis versus a buck-boost topology has been carried out. The basis for comparison took into account operation with identical target parameters ($P_o = 100$ W, $V_o = 20$ V), similar conduction losses, and switching losses when available. It should be noted that since the area product calculation of the magnetic element described above is based on equal losses, this factor has been removed from the efficiency estimation.

To establish a fair comparison for similar converters dimensions and reasonable losses, a synchronous buck-boost converter operating at BCM has been evaluated. The converter's efficiency taking into account conduction losses as well as switching losses (due to overlap) can be expressed as

$$\eta_{BB} = \left[1 + 1.3\frac{R_s}{R_L}\left(\frac{1+A}{A}\right)^2 + \frac{t_{tr}}{T_s}\frac{(1+A)^2}{3A}\right]^{-1} \tag{20}$$

where 1.3 is the rms to average current factor at BCM and t_{tr} is the ON–OFF transition time of the switch.

Fig. 10 plots the efficiency of (20) compared with the efficiency estimation of the GRSCC derived in (14) as a function of the voltage gain A. The figure shows the results for various loop resistances and operating frequencies. As can be observed, the main advantage of GRSCC is the ZCS operation that exhibits higher efficiency than the buck-boost at higher operating frequencies. This allows further enhancement of the power density of the GRSCC. For cases of higher conduction losses and lower switching frequency, utilization of a buck-boost converter is still preferred.

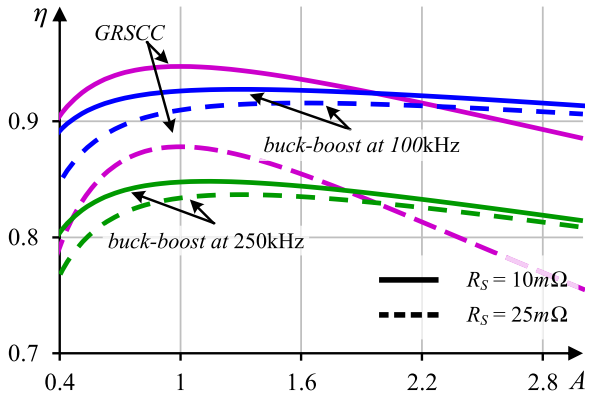

Fig. 10. Efficiency curves of GRSCC and buck-boost converters operating with the target parameters: $P_o = 100$ W, $V_o = 20$ V ($R_L = 4\ \Omega$), $t_{\rm tr} \times f_s = 0.02$.

TABLE IV
PARAMETERS OF THE EXPERIMENTAL PROTOTYPES

Parameter	Converter A		Converter B	
	Value	*Model*	*Value*	*Model*
C	0.26 μF	Polypropylene	10 ×0.1 μF	C4532C0G2A104J320KA
L	5.3 μH	ETD 34	0.5 μH	RM8/I-3F3
Q_1, Q_3	2×NMOS uni-directional	IRFP3077	PMOS	IXTP96P085T
Q_2, Q_4			NMOS	IXTP160N10T
C_L	1 mF	Electrolytic	5×10 μF	C5750X7SR1H106K
Drivers		MIC4427YN		MIC4427YN
MCU		dsPIC30F2020		dsPIC33F16GS502
R_S	130 mΩ		48 mΩ	
f_n	~100 kHz		~130kHz	
dead time	~180 ns		100 ns	
V_{in} (max)	55 V		30 V	
V_{out} (max)	70 V		30 V	
P_{out} (max)	200 W		100 W	

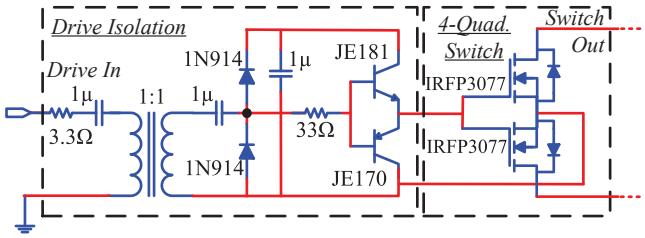

Fig. 11. Drive isolation for the switches in the type-A converter.

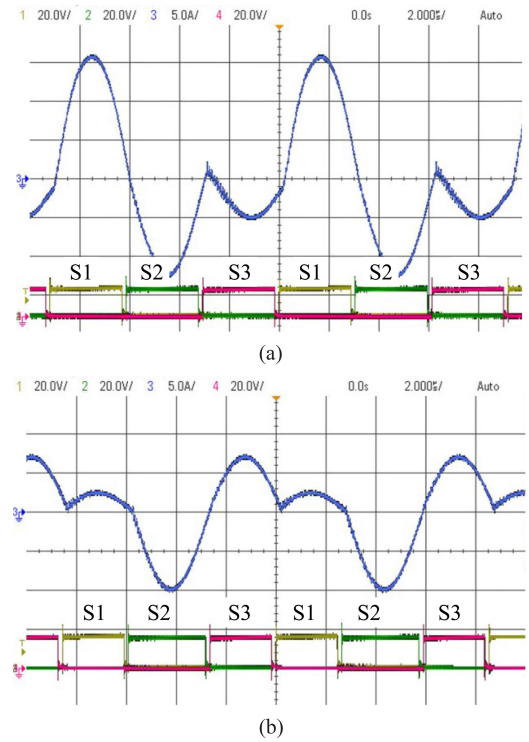

Fig. 12. Experimental waveforms: (a) in a step-up operation mode and (b) in a step-down operation mode. Upper trace—inductor current (5A/Div.). Lower traces—S(1,2,3) gate signals. Horizontal scale: 2 μS/Div.

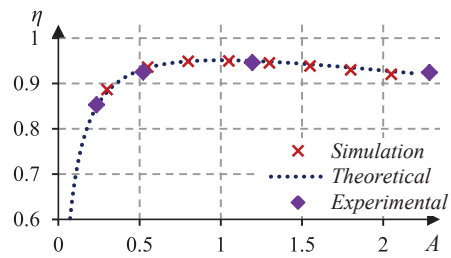

Fig. 13. Gyrator efficiency as a function of voltage gain, A.

VII. EXPERIMENTAL VERIFICATION

To demonstrate the operation of the newly developed converter and to verify the theoretical analysis, two sets of experimental test benches were constructed. In the first experiment, a converter of type-A that follows the generic topology of Fig. 3 was realized and examined for the fundamental characteristics of the gyrator converter and efficiency evaluation. In the second experiment, the converter was constructed as the bridge topology of Fig. 8 (type-B) and its performance as voltage regulator was evaluated. Table IV summarizes the parameters and lists the components of the two experimental prototypes.

In the type-A topology, the bidirectional switches were realized by two power MOSFETs connected back to back. Floating switch drives were implemented by applying isolation transformers as shown in Fig. 11 [37]. The system was tested under open-loop conditions, while the switching frequency and states switching periods were manually adjusted to obtain ZCS. Waveforms showing resonant, step-up, and step-down, ZCS operation are given in Fig. 12. Validation of the converter's high efficiency along a continuous voltage conversion range is depicted in Fig. 13, and was carried out by varying the input voltage, and load resistance, while keeping the output power to be constant of around 10 W. As can be observed, the experimental results tightly follow theoretical calculations as well as the results of cycle-by-cycle simulation. The efficiency was measured to be well above 90% for a wide operation range. The natural gyration ratio g_n of the converter as a function of voltage gain was evaluated by varying input voltage, while the output voltage was kept constant. This was done by varying R_L as V_1 changes. Theoretical calculations, simulations, and experimental results for this evaluation are presented in Fig. 14. The deviation of experimental results from the theoretical analysis at lower conversion ratios is primarily due to the higher conduction losses and consequently the lower efficiencies at these ratios as can be seen from Fig. 13. Another reason for the deviation is that the resonant characteristics of the three states were not identical, a

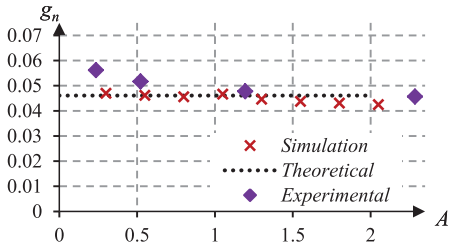

Fig. 14. Natural gyration ratio as a function of voltage gain, A.

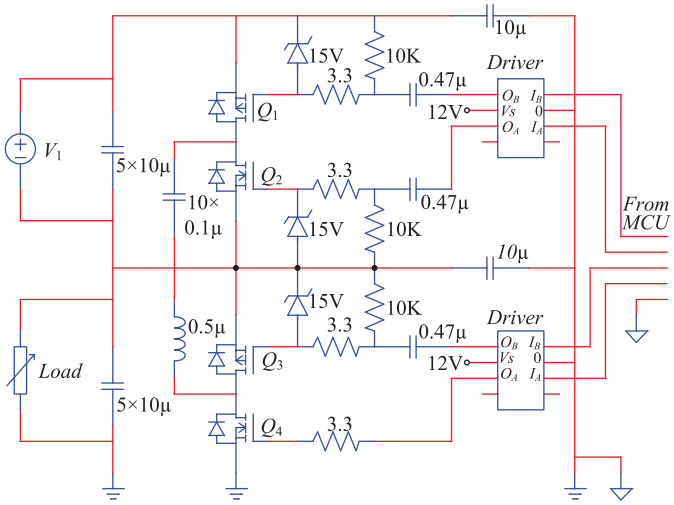

Fig. 15. Schematic of the type-B converter.

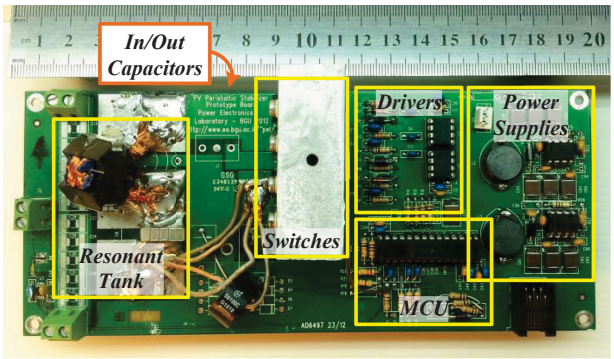

Fig. 16. Photograph of the PCB for the type-B converter.

fact that was not taken into account in theoretical derivation of g_n. In particular, as can be observed from Fig. 12(b), the discharge period (S2) is significantly longer than other states and will have a growing effect on g_n for smaller values of A (larger step-down ratios).

In the type-B topology of Fig. 8, the power MOSFETs Q_1 and Q_3 were implemented by PMOS and Q_2 and Q_4 by NMOS. As can be observed from Fig. 15, a capacitively coupled driver circuitry was used to pass the control signals from microcontroller to the MOSFETs that were untied from ground potential [19], [38]. Fig. 16 shows a photograph of the PCB used for the experiment. Zero cross detection was done automatically by the microcontroller, while the frequency adjustment to maintain the desired regulation was obtained manually. It should be

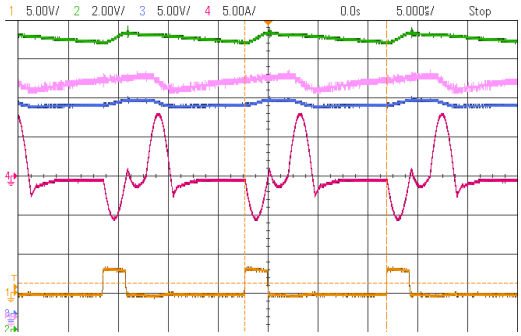

Fig. 17. Oscilloscope screenshot of a bridge gyrator converter, working at 70 kHz with $V_o = 15$ V, $A = 1.25$, $P_o \approx 22$ W, $\eta = 90\%$. Traces from top to bottom: V_2, V_1 (math function 5V/div), (V_1+V_2), I_C, $Q_{4,\mathrm{Gate}}$. The order of the states is S3-*discharge,* S1-*invert,* S2-*charge, delay*.

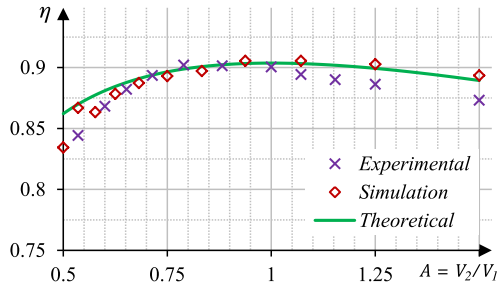

Fig. 18. Efficiency graph for the bridge gyrator as a function of A.

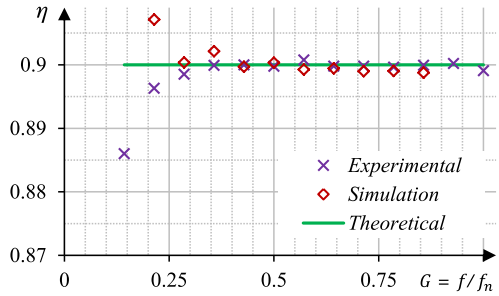

Fig. 19. Efficiency for the bridge gyrator as a function of the parameter G.

pointed out that unlike in the case of converter A that operates in open loop with constant frequency (f_n), converter B was operated with manual frequency adjustments to achieve the desired output voltage. Fig. 17 shows the steady-state operation of the converter at $f_s = 70$ kHz, $V_{\mathrm{in}} = 12$ V, $V_{\mathrm{out}} = 15$ V, and $P_{\mathrm{out}} = 22$ W. As one can see from the current waveform (second trace from the bottom), the converter is operated in a PFM mode; the switching frequency (f_s) is different from f_n, i.e., time delay is introduced to facilitate regulation. Efficiency evaluation of the converter for a range of voltage gains was carried out by changing the input voltage and compensating with the total time such that the output power and output voltage, 22 W and 12 V, respectively, were kept constant (see Fig. 18). The theoretically calculated characteristics were found to be in very good agreement with the experimental and simulation results. Fig. 19 presents the efficiency of the converter as a function of the control parameter G. The theoretically predicted constant efficiency behavior is well validated by the simulation and

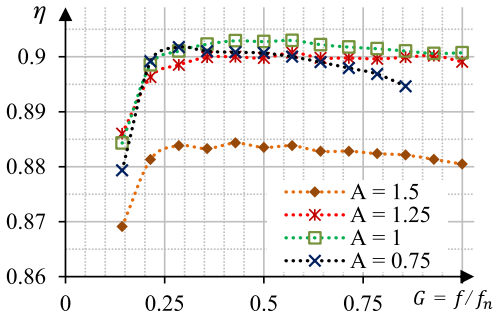

Fig. 20. Bridge Gyrator efficiency as a function of parameter G, voltage gain is a parameter.

experimental results for wide operation range. Some mismatches at lower G-s can be explained by the fact that at longer periods (lower G), the output voltage ripple increases as implied from (16), that is, larger voltage differences are present, and hence, higher peak (and rms) currents are required to sustain the output voltage at the desired value, ultimately reducing the system efficiency. Fig. 20 summarizes the experimental traces of converter efficiency for different power levels as a function of control parameter G, for several conversion ratios (different traces), and supports the claim that efficiency of the converter developed is primarily affected by the conduction losses.

VIII. Discussion and Conclusion

A novel resonant switched capacitor topology was introduced. The converter demonstrates losses characteristics that are independent, to a large extent, of the voltage gain which is a unique feature among the switched capacitor-based converters. This attribute, *resided thus far only in switched-inductor converters*, has been realized in this paper by RSCC technology. As a result, this topology has a wide, continuous input to output voltage ratio (lower and higher than unity) without sacrificing the converter's efficiency. This is an advantage over the switched capacitor's technology that overcomes the dependency of the efficiency on the gain. Finally, the converter has a gyrator-like behavior, which is an advantage in current sourcing applications.

A detailed analysis of the converter's characteristics that was carried out provided the fundamental static relationships for the gyration and conversion ratios and efficiency estimation. Expansion of the analysis has established the foundations for voltage regulation and extracted the gyration factor for PFM operation mode. The analysis was rigorously verified by simulations and two independent experimental test benches. Very good agreement was obtained of all results.

The analysis revealed that the losses of the converter are primarily due to conduction losses, which are affected by the loop resistances and rms current in each subcircuit. It was also found that similarly to PWM converters, the gyration ratio can be considered constant for wide operation range, provided sufficiently high efficiency of the converter (85%). In cases of operation at lower efficiencies (extreme conversion ratios), the gyration ratio is expected to deviate from its constant value. Furthermore, for a given finite efficiency, the gyration factors (g_n and g_n^{-1}) of (6) may hold different values. This deviation between the two values depends on the conversion type (step up or step down).

It should be noted that the main goal of the GRSCC is to extend the operation range of the conventional RSCCs without sacrificing the system efficiency or dimensions. That is, to allow high-efficiency operation in the range of the target voltage of the converter rather than in a singular point. This is evident from the theoretical analysis and the experimental validation where the high-efficiency range of a 1:1 RSCC has been extended to the range of 0.5–2. At higher voltage gains, the higher circulating current through the tank, required for charge balance, results in reduced efficiency. Further efficiency comparison against buck-boost configuration has demonstrated the GRSCC superiority when operating at higher switching frequencies within and beyond the area of the target range.

A method for voltage regulation that has been introduced employs time delay between cycles of operation. By doing so, the amount of charge that is transferred to the output may be controlled. With the addition of control feature, the converter operation resembles to discontinuous-mode PFM of any switched-inductor converter, and may be treated as such. The unique advantage of the new gyrator converter is that it merges the virtues of both worlds: wide operation range with high efficiency (from switched-inductor converters) and reduced volume (from SCC). A family of topology derivatives was also presented, which provides general, all-purpose, converters and simplified versions for specific modes of operation or conversion types. One attractive realization that will be further detailed in subsequent publications is the bridge configuration that may be a good candidate in replacing buck-boost converters, in battery, capacitor, and photovoltaic system balancing. Another subject that requires further exploration is the possibility to integrate the charge balancing mechanism in RSCCs with multiple *LC* tanks.

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