Multiple Conversion Ratio Resonant Switched-Capacitor Converter With Active Zero Current Detection

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***Abstract*—This paper introduces an active method for zero current switching for resonant switched capacitor converters (SCC) with wide dynamic range. The method is demonstrated on a binary SCC that features wide range of conversion ratios. Due to the resultant high efficiency of the converter operating under soft-switching conditions, it is applicable for higher power levels up to the medium power range (100 W). The resonant operation is achieved with a single air core inductor and precise commutation at zero current. The sensing signals of the resonant currents are obtained from the flying capacitors rather than form element in which the current includes a dc component. The zero detection method developed is capable of compensating for both the processing delays (from detection to switching action) and for the large variations of the resonant characteristics (due to transition between subcircuits), and for any other component variations. A 100 W prototype with maximum input voltage of 100 V and up to 19 conversion ratios has been built and tested experimentally. The current sensing has been implemented with a simple, cost-efficient, passive sensor. For proper construction of a higher power experimental prototype with desired target efficiency, a set of design considerations for the selection of the power stage components, based on an expanded equivalent resistance concept for multiple subcircuits converter, has been delineated. In addition, a simple and efficient isolated gate driver circuitry is presented.**

***Index Terms*—Binary codes, DC-DC power converters, soft switching, switched capacitor circuits, switched-mode power supply, zero current switching.**

I. Introduction

SWITCHED capacitor converters (SCCs) are becoming an attractive alternative in many applications ranging from low to high power. These include voltage regulators for mobile electronic systems, voltage equalizers for batteries and capacitors, for photovoltaic (PV) modules, and for automotive applications [1]–[7].

The efficiency of an SCC linearly depends on the proportionality between the output voltage and the target voltage $V_o/V_{\rm Target}$ [8]–[11], were $V_{\rm Target} = MV_{\rm in}$ and M is the no-load voltage transfer ratio. High efficiency can be reached if M is widely controllable with high resolution. The generic equivalent circuit model for SCC [12], [13], describes the losses by an equivalent resistance connected at the output of the SCC—$R_{\rm eqT}$, i.e., $\eta = V_o/V_{\rm Target} = R_o/(R_o + R_{\rm eqT})$.

An effective way to realize many target voltages is the binary/Fibonacci SCC that exhibits a widely controllable conversion ratio [10]. The benefits of resonant operation with this converter have been demonstrated in [14].

Soft switching in resonant converters can be obtained by switching the transistors at zero current. Given that the resonant frequency depends on the tank's physical parameters—*C*, *L*, and *R*, the switching times can be either calibrated in advance to match the resonant frequency, or a control circuit can be implemented to identify zero crossing. For the case of conventional resonant converters, zero current switching (ZCS) operation and its implementation have been widely demonstrated [15]–[19]. For the case of resonant SCC however, few topologies have been proposed, e.g., [2]–[7]. A methodological approach to obtain ZCS for the entire dynamic range of the SCC has not been reported hitherto.

The main problem of precalibrating resonant SCCs for ZCS is that the physical parameters of the system are prone to drifts throughout the operation range. This is particularly crucial in resonant SCC circuits since the inductance is often implemented by the stray inductance of the circuit which may vary by design and from one subcircuit to another while the capacitance values drift as a function of bias voltages and temperature. Hence, an active zero current cross detection circuitry is required to compensate for all inaccuracies and uncertainties of the parameters, and to assure ZCS operation.

Another challenge for sensing the current in resonant SCC is the dc component of the resonant current. In this case, the signal is not centered around zero and requires additional processing for zero detection. This can be done using rather costly active sensors or by resistive elements alongside with very high gain-bandwidth op-amps [20]–[23].

The objective of this study is to introduce an active ZCS method for resonant SCC, and to apply it on a resonant binary/Fibonacci SCC. The resultant converter has a wide range of conversion ratios with high efficiency that can be applied in higher power applications. The diagram of Fig. 1 shows the system configuration of the active ZCS converter. A resonant binary/Fibonacci SCC is implemented by adding an inductance at the output of the converter. The converter is capable for either step-up or step-down conversions depending on the source-load orientation. That is, step-up conversion can be obtained by swapping the input and output.

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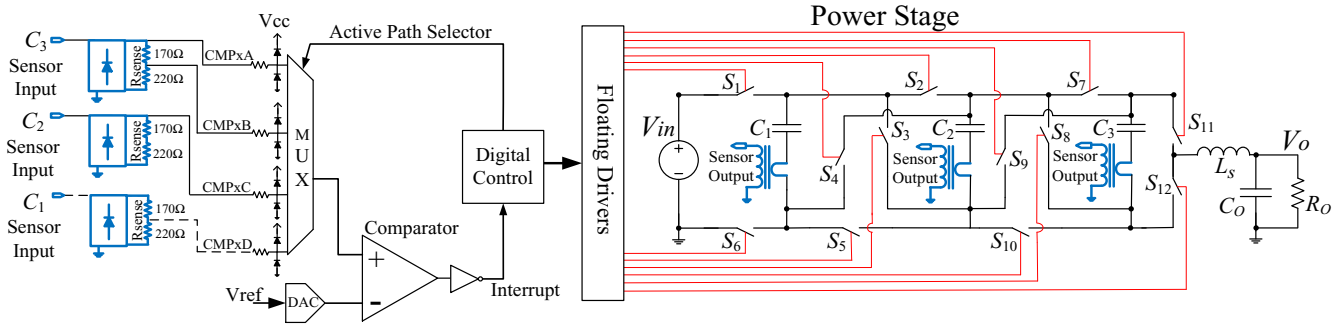


Fig. 1. Resonant SCC scheme showing the current sensors and analog comparator for zero cross detection.

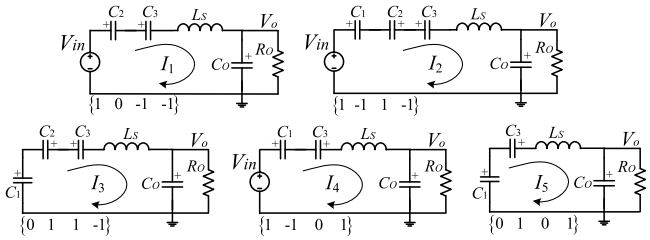


Fig. 2. Resonant SCC subcircuits configured from the EXB codes of $M = 5/8$.

TABLE I
SOLUTIONS OF THE AVERAGE CAPACITOR CURRENTS FOR VARIOUS RATIOS

	Proportional Coefficient				
M	k_1	k_2	k_3	k_4	k_5
1/8	1/8	1/8	1/4	1/2	–
3/8	–1/8	3/8	1/2	0	1/4
5/8	1/4	3/8	–1/8	0	1/2
7/8	1/2	1/4	1/8	1/8	–

For simplicity and without losing generality, the active ZCS method is demonstrated and explained for binary SCC case.

II. Resonant Binary/Fibonacci SCC

The precursor of the converter of Fig. 1 is the hard-switched binary/Fibonacci step-down SCC [8]–[10], which is capable of generating multiple fractional conversion ratios with binary and/or Fibonacci resolution. For a case of three flying capacitors ($n = 3$), the converter is capable of producing 19 levels of conversion ratios with high efficiency [10]. To achieve a desired fractional conversion ratio, a specific switching sequence that interconnects the flying capacitors with summing or subtracting action to the source and the output, is applied. For example, a conversion ratio of $M = 5/8$, requires extended binary (EXB) codes that are translated to five subcircuits as illustrated in Fig. 2. Following the switching sequence, the average voltages across the flying capacitors and the output voltage will adjust to: $V_{C1} = (1/2)V_{\rm in}$, $V_{C2} = (1/4)V_{\rm in}$, $V_{C3} = (1/8)V_{\rm in}$, $V_{Co} = (5/8)V_{\rm in}$. Since solution is unique [9], control is not required to assure that the capacitors have stabilized at their nominal voltages. The voltages of the flying capacitors hold the same average value for any conversion ratio available using the EXB code.

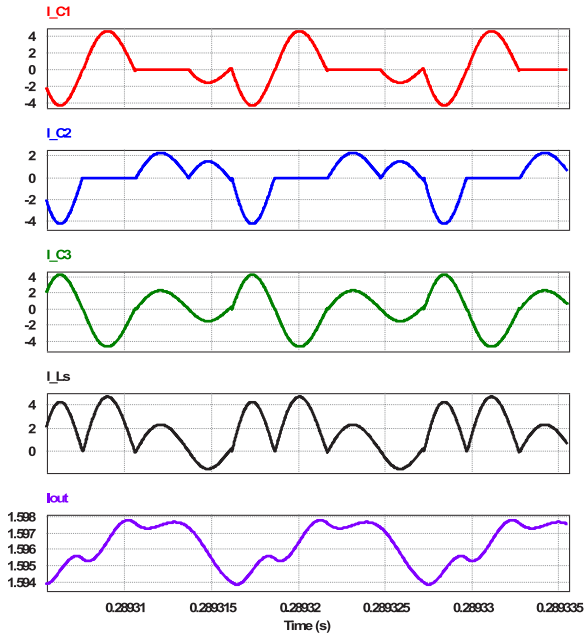
Resonant operation with sinusoidal current can be obtained by relying on the stray inductances that exist in the conduction path of each subcircuit. This approach may be impractical in applications where the switching frequency is limited (by the generator or drive losses) [2]–[7]. A more practical approach that is applied in this study is to introduce a single air-core inductor, $L_{\rm s}$, in series to the output stage [2]–[7], [14]. By doing so, the same (dominant) inductance is affecting all subcircuits (see Fig. 2). Transition between switching states (subcircuits) under ZCS conditions can be carried out either by manual timing of the switching period of each state, or by an active ZCS, that is, measuring the resonant current, detecting a zero current level, and then toggling the switches to the next subcircuit sequence. Since the resonant characteristics, i.e., the natural frequency and quality factor, of the subcircuits may vary significantly because of different interconnections of the capacitors, as well as stray inductances, an active method is essential to assure ZCS. This approach also compensates for any parameter variations or drifts due to changes in the operating conditions.

The contribution of each flying capacitor to the average output current (for $M = 5/8$) may be derived from the equivalent RCL circuits of Fig. 2. Under steady-state operation, charge balance of all capacitors is satisfied (i.e., average current equals zero). The sum of the currents for each state I_1–I_5, and the sum of all currents, can be expressed as

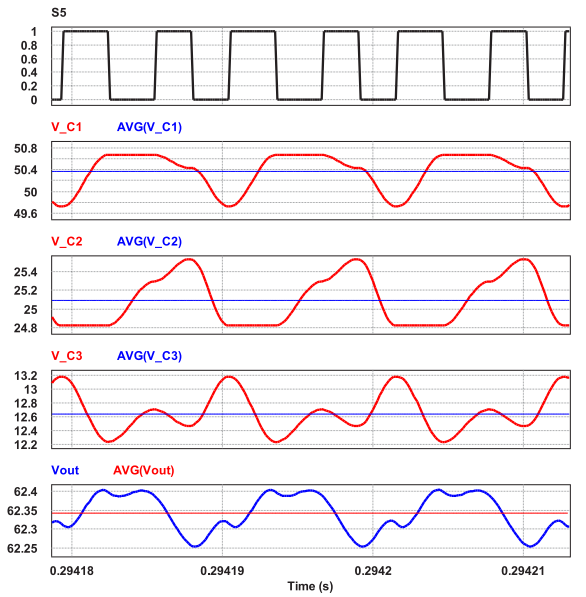
$$\begin{cases} 0 - I_2 + I_3 - I_4 + I_5 = 0; C_1 \\ -I_1 + I_2 + I_3 + 0 + 0 = 0; C_2 \\ -I_1 - I_2 - I_3 + I_4 + I_5 = 0; C_3 \\ I_1 + I_2 + I_3 + I_4 + I_5 = I_o; \end{cases}, \quad M = 5/8 \qquad (1)$$

where the currents I_j are average currents of each subcircuit (averaged over the entire switching period).

Table I summarizes the expected currents for various conversion ratios that were obtained by solving a set of equations similar to (1). In each case, k_j is the proportional coefficient between the average current of the flying capacitor and output current for state j, namely, $I_j = k_j I_{\rm out.}$ Duality can be observed between ratios 1/8 to 7/8, and 3/8 to 5/8.



(a)



(b)

Fig. 3. Resonant binary SCC (a) capacitors and output stage current waveforms. (b) Capacitors and output voltages waveforms. PSIM simulations set-up at: $M = 5/8$, $V_{\rm in} = 100$ V, $P_{\rm out} = 100$ W, $L_s = 200$ nH, all flying capacitors $C_j = 9.4$ μF, and $f_s = 90$ kHz.

The results of Table I indicate that for a given subcircuit the average currents vary considerably between the switching state and in some cases, negative current may exist in one of the states. This implies however, that for some conversion ratios, one of the states, in fact, discharges the output capacitor. The extra circulating current will of course increase the losses. The variability of the average currents between the states adds extra burden to the zero detection circuitry.

To illustrate the operation of the resonant SCC, typical currents and voltages waveforms, are depicted in Fig. 3 for the case of $M = 5/8$. It can be observed that the average currents of the flying capacitors is zero, their voltages are stabilized, and that the dc output current is built up by the contribution of all subcircuits that, in turn, are connected to the load for half a resonant period. The portion of negative current is also observed.

III. Practical Implementation

To realize cost-effective resonant operation for the SCC of Fig. 1, that is, to obtain soft-switching of *all switches for all transitions between subcircuits*, the following challenges need to be addressed.

- The seemingly natural current sensing point, the series inductance to the output, contains a dc component.
- The resonant characteristics (natural frequency and quality factor) are considerably different from one subcircuit to another. This is due to different interconnections of the flying capacitors according to the EXB code (e.g., Fig. 2).
- Uncertainties and variations of the parameters (inductance and capacitance) may be very large. Especially for different operating conditions (conversion ratio and power levels).
- The average and the peak current are not constant for each subcircuit and for a given state at different power ratings.
- Zero current detection at the crossing point is impractical due to poor signal-to-noise ratio (SNR) and the time delay from detection to commutation of the switches. Selection of the reference depends on the aforementioned arguments.
- Gate drive circuitry to assure operation of large number of floating switches.
- Considerations for components selection based on the expected losses of the system.

To overcome these challenges, a zero current detection and control circuitry was developed in this study and is schematically described in Fig. 1. It includes a current sensor for each of the flying capacitors, comparator module, microcontroller, and decoders. The transition between switching states of the EXB code is governed by comparing the resonant currents to specified references. These are discussed in this section which also addresses issues of limiting the inrush current, stabilizing the capacitors' voltages after startup, and the realization of simple and efficient floating gate drivers of the power switches.

A. Current Sensing and Zero Crossing Detection

To eliminate the need for a rather costly, active current sensing circuitry that accommodates dc current, passive magnetic current transformers are placed on all three flying capacitors.

Since the aim of the current sensing is the detection of the zero crossing point rather than regulation, the dc component of the current is not of interest. The reason for the apparent redundancy in the current measurements is that there is no single capacitor that participates in all the states for all voltage ratio configurations. In the example shown in Fig. 2 of 5/8, C_3 participates in all the states, but for other ratios such as 2/8 it is omitted. By having three sensors, current can be read from any active capacitor.

A conventional passive magnetic sensor has been utilized for zero detection. This exemplary practice may seem against the original concept for using SCC technology to avoid magnetic

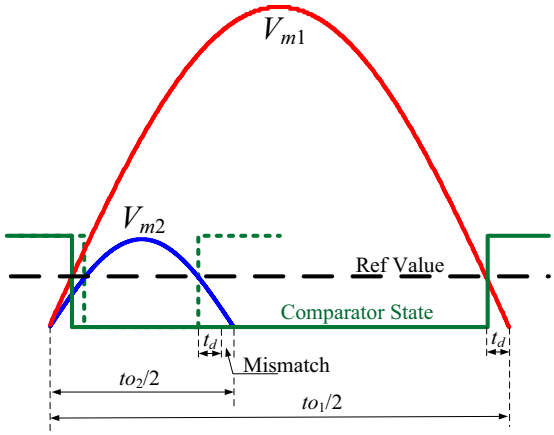


Fig. 4. Worst-case conditions of state current variation and the mismatch of the switching instance due to fixed reference settings.

components. Fortunately, since the current sensing is aimed purely for detection of the current zero crossing point, only the shape of the current signal in the vicinity of zero is of interest. This implies that a weakly coupled, i.e., coreless, sensors may be employed [24].

A comparator module that is integrated in a microcontroller was utilized in this paper for current detection. Since the comparator is a part of the IC and prohibits negative voltages, the sensed current was first rectified and then converted to a proportional voltage using a resistor R_{sense}. To protect the I/O ports of the digital controller and since only the information in the vicinity of zero current is of interest, the rectified signal is clamped to the voltage rails by diodes. The series resistor is used to limit the current to the controller. By taking these measures of precaution, the resistor R_{sense} can be selected to the worst-case for the state of the lowest current.

At steady-state, switching command is initiated by the analog comparator module. The comparator output triggers an auxiliary interrupt upon zero detection in which the switching state of the next subcircuit is applied on the transistors, and if required, changes the path selector of the MUX for next state.

B. Reference Voltage

As mentioned earlier, the comparator reference voltage cannot be zero since finite response time, t_d, exists in the control system—i.e., delay time from detection to actual switching action. The reference voltage is set to compensate for t_d and for the slope of the sensed current [25]. Fig. 4 shows typical difference between two state pulses being sensed. Assuming a high-quality factor ($Q > 3$), the reference voltage, as a function of the resonant peak and time duration can be expressed as

$$V_{\text{ref}j} = \frac{I_{mj}}{n} \sin\left(2\pi\left[\frac{1}{2} - \frac{t_d}{t_{oj}}\right]\right) R_{\text{sense}} \tag{2}$$

where n is the current transformer winding ratio, I_{mj} is the flying capacitors currents, t_{oj} is the resonant period, and $j \in \{1, 2, 3, 4\}$ is state indicator. The peak value of the sensed signal is translated into voltage by $V_{mj} = (I_{mj}/n)R_{\text{sense}}$.

The slope of the sensed current depends on the circuits' resonant frequency and peak currents, and varies from one subcircuit to another. Variable reference voltage would assure accurate ZCS at every switching instance. However, this requires an extremely fast control loop to obtain the information of the state current on-the-fly [26]. To avoid this complexity, a compromise is made based on the expected variations in the currents due to the operation in different subcircuits and parameters variations. It allows setting of a constant reference voltage with the penalty of mismatch in the switching with respect to the zero crossing point. Considering an extreme worst-case slope variation as depicted in Fig. 4 of 400% increase in peak current and 200% increase in resonant period, and that t_d is approximately 0.1 t_{oj}, the ratio between the worst-case reference (V_{ref1}) and the nominal reference voltage (V_{ref2}) can be obtained using (2), that is

$$\frac{V_{\text{ref1}}}{V_{\text{ref2}}} = \frac{\frac{4I_{m1}}{n} \sin\left(2\pi\left[\frac{1}{2} - \frac{0.1t_{o1}}{2t_{o1}}\right]\right) R_{\text{sense}}}{\frac{I_{m1}}{n} \sin\left(2\pi\left[\frac{1}{2} - \frac{0.1t_{o1}}{t_{o1}}\right]\right) R_{\text{sense}}} = 2.1 \tag{3}$$

which translates into an absolute maximum mismatch in the switching time of 0.1 t_{oj}. Provided that the operation of each subcircuit is in the range of microseconds, the result of (3) implies a small deviation from the true zero crossing point, allowing the use of a fixed reference voltage.

In this paper, the reference voltage and the sensing gain are selected such that the true ZCS is obtained at higher power levels (higher states' currents), and the small mismatches in the ZCS will be at lower power levels. To allow operation in wide range of power levels and input voltage variations and still work in the vicinity of ZCS, a coarse tuner to switch between operation ranges is realized. The scaling of the sensing gain is implemented by voltage dividers branching out to the MUX (see Fig. 1).

Another consideration when setting a low reference value is the need to avoid the ground noise caused by imperfect switching at nonzero, common-mode, etc., that may result in erroneous triggering of the comparator. This is overcome by a blanking period of the comparator after switching action, as done in many commercial current sensing oriented applications.

C. Stabilizing the Flying Capacitors Voltage on Startup

The design of the active ZCS method and circuitry assumes that the voltages of all capacitors have stabilized to their nominal values (binary fractions). Applying the above zero detection method (demonstrated in detail in the next section), assures that at steady-state ZCS is realized for all conversion ratios and over a wide operation range of input voltage and power levels. In a practical turn on situation, the capacitors' voltages are zero. This results in high inrush currents if the converter is allowed to operate in the vicinity of the steady-state resonant frequency. Moreover, relying on the comparator to trigger commutation is impractical since the inrush current profile may not be of a resonant nature. To remedy this, a voltage-stabilizing and current-limiting sequence is required to limit the flying

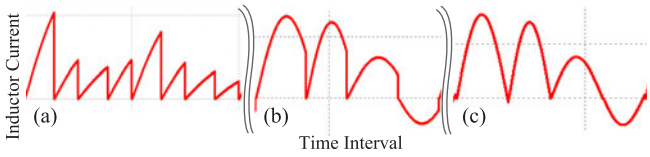


Fig. 5. Conceptual operation of the soft start sequences for $M = 3/8$ (resonant current): (a) high-frequency switching; (b) estimated resonant values; and (c) active ZCS method.

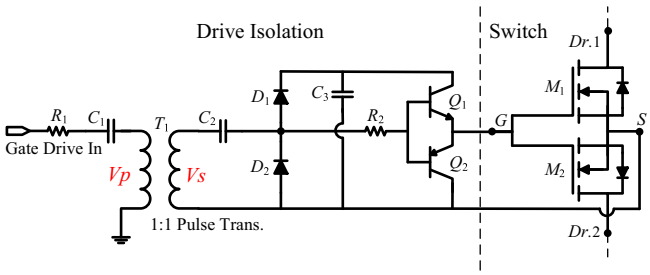


Fig. 6. Isolated gate driver and four-quadrant switch using N-channel power MOSFETs.

capacitors current to a safe value and to bring the flying capacitors voltage to their steady-state value.

In this study, as shown in Fig. 5, a voltage-stabilizing and current-limiting method that is based on the operation of the binary converter is applied. The concept is to rely on the EXB codes to assure stabilization of the capacitors' voltages to the correct values, and to limit the inrush current by controlling the switching frequency, this is done as follows: At startup the switching times are made significantly shorter than the resonant period such that the peak current does not exceed a set maximum value. This is done for few cycles until the voltage across the capacitors has stabilized. Then, a second switching sequence that is adjusted to the estimated resonant values is applied for few cycles to ease the transition to active current sensing. At the end of this phase, the ZCS circuitry is activated and transition between subcircuits is governed by the comparator output.

D. Switches and Isolated Gate Drivers

To facilitate all the interconnections of the flying capacitors as prescribed in the EXB codes [8]–[10] for all conversion ratios, the converter includes 12 four-quadrant switches (see Fig. 1). Each switch is realized by two N-channel power MOSFETs with the gate and sources interconnected as depicted in Fig. 6.

Isolated gate drivers are required to allow high input voltage operation. As depicted in Fig. 6, the gate driver structure used in this study consists of a 1:1 pulse transformer for isolation, a dc blocking capacitor C_1 to prevent the dc content of the gate drive from passing through the pulse transformer, C_2 and D_2 to restore the dc level at the secondary side, capacitor C_3 that acts as independent floating supply, and NPN and PNP transistors connected in a push–pull configuration.

Assuming that the voltages across C_2 and C_3 are stable, the operation of the gate driver may be described as follows: at turn on Vp is positive which turn on Q_1, partially discharging C_3 upon C_{GS}, to turn on the MOSFET. Once D_1 starts conducting, C_3 recharges through C_2 and D_1. The independent supplier C_3 provides a quick charging of C_{GS} and therefore, the rise time is relatively fast. At turn off Vp is negative, D_2 is forward biased, C_2 now charges in the opposite direction through D_2. C_{GS} discharges through Q_2 that is saturated, turning off the MOSFET. R_2 damps potential overshoots that may occur due to stray inductances.

For construction and component selection of the isolated gate driver of Fig. 6, the following procedure is suggested.

- Given a power transistor with specified gate charge requirements (Q_{gate}) and provided the turn on/off transition time t_r, the required peak current of the low-side driver can be estimated as

$$I_{pk} = \frac{Q_{\text{gate}}}{t_r}. \tag{4}$$

- The effective magnetic area, A_e, for the isolation transformer is calculated based on the maximum flux density that is allowed, $B_{\max}$, resulting from the maximum on time t_{on}, that is defined by the resonant period of the system. To comply with the specification sheets of commercial compact pulse transformers, the voltage–time product has been defined as the target parameter as

$$nA_e B_{\max} = V_{GS} t_{\text{on}} \tag{5}$$

  where V_{GS} is the applied gate voltage and n is the number of turns at the secondary winding.
- Resistors R_1 and R_2 (optional) are selected to damp oscillations and avoid high peak currents that may appear due to the stray inductances and the total gate capacitance. Typically applied using manual trim.
- The dc blocking and restoring capacitors C_1 and C_2 are selected to sustain the average drive voltage per switching cycle.
- Capacitance C_3 is required to be sufficiently high to allow charging of C_{GS} while sustaining the required gate voltage, that is

$$C = \frac{I_{av}}{\Delta V \cdot f_s} \tag{6}$$

  where I_{av} is the average capacitor current, and ΔV is the voltage ripple of the capacitor.
- Q_1 and Q_2 are selected to sustain the gate peak current with the repetitive rate of switching frequency.

The components values used in the experimental prototype are: $C_1 = C_2 = C_3 = 1\ \mu$F, $R_1 = 3.3\ \Omega$, $R_2 = 33\ \Omega$. The operation of the experimental floating drivers has been verified at switching frequency in the range of 30–350 kHz, wide duty cycle range of 0.1–0.9, and rise and fall times of approximately 200 ns.

E. Equivalent Resistance—Considerations for Components Selection

The primary contributor of losses for the ZCS resonant binary/Fibonacci SCC under study is the conduction losses in each subcircuit. When combined together, the total equivalent

resistance is a good tool to predict the system efficiency based on the system parameters. Examination of the losses based on the generic equivalent modeling approach of [12] and [13] adds a practical insight to determine the size of the power transistors (on resistance) and required characteristic impedance (capacitance–inductance ratio). There, the equivalent resistance is represented as a function of the resonant characteristics of the system. In this study, the methodology presented in [12] and [13] for a simplistic case of a unity converter has been adapted to estimate the equivalent resistance of the resonant binary/Fibonacci SCC that includes multiple subcircuits per operation cycle.

Given that each stage for all EXB/signed Fibonacci representation (SFN) codes consists of four dual switches in the conduction path, without loss of generality, the total parasitic loop resistance for every subcircuit ($R_{\mathrm{loop}j}$), is approximated to $8R_{\mathrm{DS(on)}}$ (neglecting the ESR and other stray resistances). The total equivalent resistance R_{eqT} in its generic form can be expressed as a function of the subcircuits' quality factors Q_j [13] by summation of the equivalent resistances in all subcircuits, that is

$$R_{\mathrm{eqT}} = \sum_{j=1}^{n} k_j^2 \frac{2\pi \cdot Q_j^2 \cdot R_{\mathrm{loop}j}}{\mathrm{df}_j \sqrt{4Q_j^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_j^2 - 1}}\right) \quad (7)$$

where $\mathrm{df}_j = f_s/f_d$, is the ratio between the switching frequency, f_s, to the damped resonant frequency, f_d, for each subcircuit, and *j* is the subcircuit index.

Since the case under study involves multiple subcircuits with different number of serially connected capacitors which results in different values of Q_j (as can be observed from the subcircuits of Fig. 2), direct calculation of (7) based on the system specific values has several degrees of freedom and therefore is quite complex. To achieve a more convenient representation of (7), the following manipulations are applied: 1) R_{eqT} is normalized to R_{loop_j} (which is assumed to be identical for all subcircuits); 2) Q_j is represented as a function of the lowest possible quality factor of all subcircuits (defined as Q_{j_low}). The value of Q_{j_low} is obtained from the subcircuit with smallest number of serially connected capacitors; 3) df_j is represented by the df of the subcircuit from which Q_{j_low} is obtained (defined as $\mathrm{df}_{j\_\mathrm{low}}$). These mathematical relationships significantly reduce the complexity of (7) to two degrees of freedom (Q_{j_low} and $\mathrm{df}_{j\_\mathrm{low}}$) and can be used to represent the worst-case design conditions from which the maximum losses can be estimated, per conversion ratio.

To exemplify the normalization procedure and plot the resultant R_{eqT}, consider the case of M = 5/8, in which $C_{t1} = C_{t4} = C/2$, $C_{t2} = C_{t3} = C/3$, and $L_{tj} = L_s$. This leads to $Q_{j\_\mathrm{low}} = Q_1$, $Q_2 = \sqrt{3/2} \cdot Q_1$ and $\mathrm{df}_{j\_\mathrm{low}} = \mathrm{df}_1$, $\mathrm{df}_2 = \sqrt{2/3} \cdot \mathrm{df}_1$, and (7) can be rewritten in the normalized form as

$$\frac{R_{\mathrm{eqT}}}{R_{\mathrm{loop}j}} = k_1^2 \frac{2\pi \cdot Q_1^2}{\mathrm{df}_1 \sqrt{4Q_1^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_1^2 - 1}}\right) + k_2^2 \frac{3\pi \cdot Q_1^2}{\sqrt{2/3} \cdot \mathrm{df}_1 \sqrt{6Q_1^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{6Q_1^2 - 1}}\right) + k_3^2 \frac{3\pi \cdot Q_1^2}{\sqrt{2/3} \cdot \mathrm{df}_1 \sqrt{6Q_1^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{6Q_1^2 - 1}}\right) + k_4^2 \frac{2\pi \cdot Q_1^2}{\mathrm{df}_1 \sqrt{4Q_1^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_1^2 - 1}}\right). \quad (8)$$

Following the same procedure, the worst-case total equivalent resistances for several conversion ratios (M = 1/8, 3/8, 5/8, 7/8) have been obtained and were numerically plotted as a function of Q_{j_low} for several values of $\mathrm{df}_{j\_\mathrm{low}}$ and are shown in Fig. 7. It can be observed that the normalized R_{eqT} asymptotically reaches a constant value for Q_{j_low} values higher than 3. This implies that the lowest possible losses can be obtained even with fairly small inductances, thus allowing the use of stray inductance or a coreless element. It can also be observed that quality factor lower than unity increases R_{eqT}. This can be explained by the fact that when $Q < 1$, the operation is no longer resonant and the rms value of the circulating current significantly increases. Another observation from Fig. 7 is that a higher value of df_j (less damped circuit) is preferable to obtain lower conduction losses.

Based on the aforementioned observations and mathematical extraction, the following design procedure is proposed and demonstrated on a case of three flying capacitors.

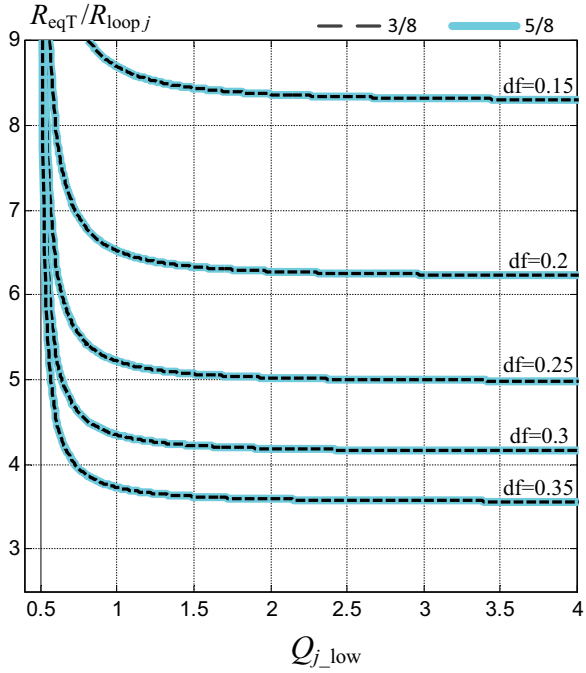
- For the highest expected conversion ratio (smallest fraction), select a worst-case Q_{j_low} and $\mathrm{df}_{j\_\mathrm{low}}$ for the subcircuit with the smallest number of serially connected capacitors.
- From Fig. 7, extract R_{eqT}. Alternatively, use (7) and the aforementioned order reduction procedure.
- Given a desired target efficiency, extract the upper boundary for $R_{\mathrm{DS(on)}}$ according to the efficiency expression, that is

$$\eta = \frac{R_o}{(R_o + R_{\mathrm{eqT}})} \rightarrow R_{\mathrm{DS(on)}} = \frac{R_o}{8\alpha}\left(\frac{1}{\eta} - 1\right), \quad \alpha \approx \frac{R_{\mathrm{eqT}}}{8R_{\mathrm{DS(on)}}}. \quad (9)$$

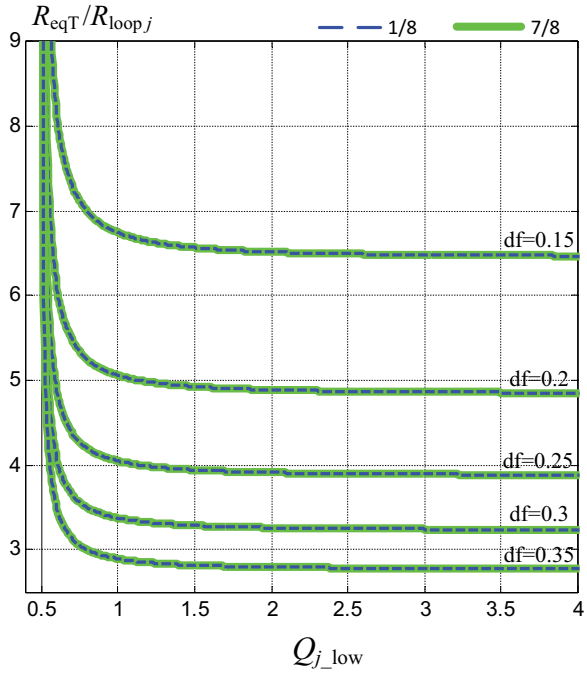
- For a reduced volume design, choose an inductance value sufficiently small that can be realized by the parasitics or without a magnetic core.
- Calculate the required capacitance to satisfy the worst-case Q_{j_low}.
- In case that the resultant resonant frequency (equals to the switching frequency thanks to the active ZCS) exceeds a practical value either due to drive losses or driver realization, recalculate *L* and *C* by iterating the two previous steps.
- Once the power transistors have been selected, the gate drive losses can be estimated as

$$P_{\mathrm{gate\_loss}} = V_{GS} Q_{\mathrm{gate}} f_s \quad (10)$$

where V_{GS} is the gate driver voltage, f_s is the switching frequency, and Q_{gate} is the total gate charge of the selected MOSFET.



(a)



(b)

Fig. 7. Worst-case plot of the normalized equivalent resistance as a function of Q_{j_low}, for conversion the ratios: (a) $M = 1/8, 3/8$, and (b) $M = 5/8, 7/8$ for df_j in the range of 0.15–0.35 (0.05 step each iteration in df_j). The curves were extracted numerically using MATLAB.

TABLE II
CONVERTER PARAMETERS

Component	Part No.	Value
	Power Stage	
Input capacitor	C5750X7R2A475K	$6 \times 4.7\ \mu$F/100 V
Output capacitor	C5750X7R2A475K	$10 \times 4.7\ \mu$F/100 V
Flying capacitor	C5750X7R2A475K	$3 \times 4.7\ \mu$F/100 V
MOSFETs ($R_{DS\,on}$)	IPA030N10N3	2×3 mΩ
Inductor	Air core	2.1 μH
Microcontroller	dsPIC33FJ16GS502	
Current Transformer	FXC -TN16/9.3/6.3 (Ferrite toroid)	1:100
	Digital Section	
Microcontroller	dsPIC33FJ16GS502	16 bit, 40 MIPS
Decoder	MC745HC139A	
	Floating Driver	
Driver	MIC4427	
Pulse Transformer	GT03-111-110-A	1:1
Transistor (Q_1)	JE181	
Transistor (Q_2)	JE170	
Diodes (D_1, D_2)	1N914	

IV. EXPERIMENTAL RESULTS

To demonstrate the performance of the resonant binary SCC and the operation of the active ZCS, a 100 W prototype has been built and tested experimentally. Summary of the system components can be found in Table II. The generation of the EXB codes has been realized on a dsPIC33F series microcontroller. Due to the large number of I/O ports required for the power switches, an auxiliary decoder is used. The microcontroller selected includes an analog comparator module and a multiplexer to allow selection of the input feed. The comparator module features high-speed operation with a typical delay of 20 ns and a typical offset voltage of ± 5 mV. However, a typical delay of the zero detection system, from comparator detection until the time that an interrupt is triggered was measured to be 500 ns. The total processing time (from comparator to switches commutation) was found to be approximately 1 μs. Following the design guidelines above, the worst-case resonant frequency (highest value) per state is set to 180 kHz to allow sufficient processing time. The reference voltage to the comparator is set to 1.65 V to compensate for the processing time delay and improve the SNR of the detection. Performance of the system and the ZCS method developed is demonstrated on operation with the conversion ratios of 1/8, 3/8, 5/8, and 7/8 to cover the entire operation range. For each of the conversion ratios, the capability of the method to lock the switching frequency to the resonant frequency is verified for wide range of line (30–80 V) and load variations (20–130 W). For the conversion ratios of 3/8 and 5/8, the current has been sensed from C_3 that is active at all subcircuits and the peak currents from one state to another are of the same order. For the case of 1/8, the current levels significantly vary between subcircuits, therefore, the feed to the comparator has been switched between C_3 and C_2. A larger R_{sense} is chosen for C_2 to successfully detect the zero crossing point at lower currents. For 7/8, to cover the full power range of 130 W, the current is sensed from top of the resistive ladder (390 Ω) of C_3 for lower power range (up to 70 W), and is then switched manually to the voltage division point (220 Ω) to measure higher power levels up to 130 W. The measurement circuitry (sensors, dividers, etc.) is detailed in Fig. 1. The gate drive losses were measured to be in the range of 1 to 2 W for all conversion ratios.

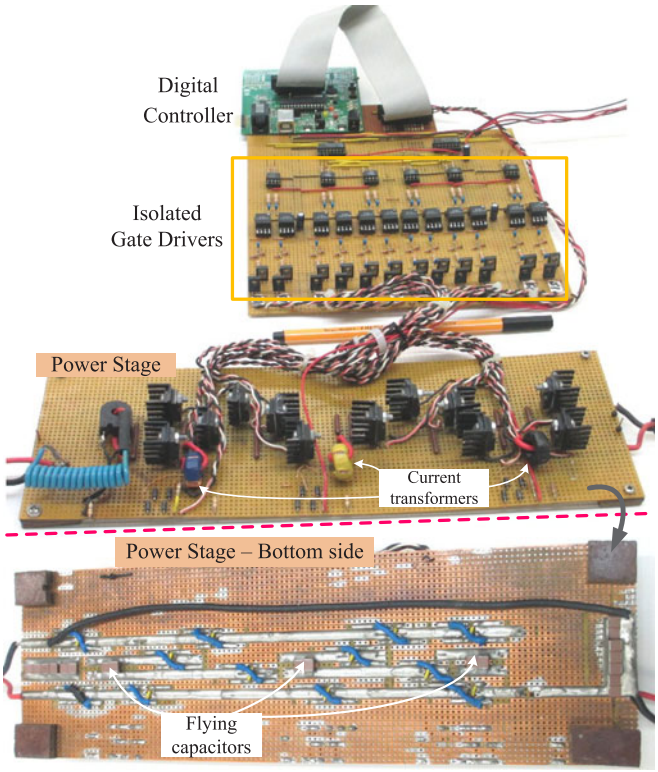


Fig. 8. Prototype of the resonant binary SCC.

A photograph of the vector-board-based experimental prototype is given in Fig. 8.

Fig. 9 shows exemplary snapshots of the system operating at steady state with active ZCS for four conversion ratios tested. As described in the practical implementation section and can be observed from Fig. 9, large differences exist between the subcircuits in the peak currents, quality factors, and the signals' slopes at the vicinity of zero current. Minor glitches in the current shapes are the result of small deviations between the estimated reference voltage and the experimental signal.

To verify the operation of the active ZCS method, two sets of experiments have been carried out. In the first experiment, the load resistance is kept constant while the input voltage varied from 30 to 80 V. Active ZCS is obtained for the entire operation range and all conversion rations. Fig. 11 shows the efficiency curves of the converter as a function of the output power for each of the conversion ratios. It can be observed that, as expected from the theory of SCC, the efficiency is virtually constant for a given load resistance.

The strength of the active ZCS is highlighted in Table III, which summarizes the average values of equivalent resistance and efficiency, and the deviation (in percentage) of the duration of each subcircuit. As described earlier and can also be observed Fig. 9, the conduction time of the subcircuit varies from one to another, this is primarily due changes in the overall capacitance. Moreover, Table III indicates that the duration of a specific subcircuit may also vary considerably due to changes in components values for different operating conditions, strongly promoting the necessity of an active method for zero detection. The largest variations in components' values are expected in

TABLE III
MEASUREMENTS WITH ACTIVE ZCS FOR CONSTANT

M	R_{out} [Ω]	$R_{\mathrm{eq}T}$ [Ω]	η_{AV}	ΔV_{in} [V]	ΔI_{out} [A]	Δt_{s1} [%]	Δt_{s2} [%]	Δt_{s3} [%]	Δt_{s4} [%]
1/8	2.5	0.37	0.847	56.8	2.37	28.6	25	23.2	13.8
3/8	16	1.05	0.925	58.6	1.27	25	2.5	2.4	21.5
5/8	29.3	1.01	0.958	36.5	0.74	1.4	30	10	1.4
7/8	36.5	0.42	0.979	24.1	0.57	7.7	25	3.2	14.3

Δx—indicates the amount of variation in a measured variable x value throughout the experiment.

wider conversion ratios such as 1/8. There, larger rms currents are needed per-unit of transferred power which affects the capacitance and inductance within a subcircuit. The larger rms currents are also the reason for the somewhat lower efficiency in spite of the lower equivalent resistance obtained for this ratio.

The variable resonant period and the variations in the sensed signal slope are experimentally demonstrated in Fig. 10(a)–(c) for the case of $M = 1/8$. It can be observed in Fig. 10(a) that while the resonant period significantly varies between $k = 1/2$ and $k = 1/8$ (due to the different number of serially connected capacitors in each state), the slope in the vicinity of zero is virtually fixed. The minor glitches in the current shapes are due to the minor difference of the slopes as explained in Section III-B. Fig. 10(b) and (c), depict the variations due to different power levels. The extended period at higher power levels are due to component variations which reduces the effective quality factor of the subcircuits. Fortunately, since the initial Q is designed to be of a moderate value (based on Section III-E), the reduction in Q extends the resonant period sufficiently such that the variation of the slopes of the resonant currents near zero are negligibly small.

In the second experiment, the input voltage is kept constant at 80 V while varying the load. Active ZCS is obtained for the entire operation range and all conversion rations. Fig. 12 shows the efficiency curves of the converter as a function of the output power for each of the conversion ratios. Similarly to the previous experiment, the efficiency is nearly constant for a wide operation range. It should be noted however, that in the case of 1/8, a narrower power range is examined due to practical constraints on the stress of the components. The power range for each conversion ratio that is covered in this experiment has been intentionally limited due to practical restrictions. That is, the experiment is conducted such that the maximum current stress on the flying capacitors does not exceed 4 A_{rms}.

The startup sequence that was described earlier is also demonstrated on the experimental setup. Fig. 13 shows the three operation modes used limit the inrush currents and stabilize the capacitors' voltages, that is, operation with EXB code at: (a) high frequency, (b) estimated times, (c) activating the active ZCS mode and locking the switching frequency to the resonant frequency.

The loss estimation method was found to be in very good agreement with the experimental measurements. Given an estimated R_{loop_j} value 170 mΩ (based on measured conduction path), the calculated R_{eqT}, according to (7) were 0.94 Ω (df $\approx$ 0.23, $R_{\mathrm{eqT}}/R_{\mathrm{loop}} \approx 5.5$) and 0.46 Ω (df $\approx$ 0.35,

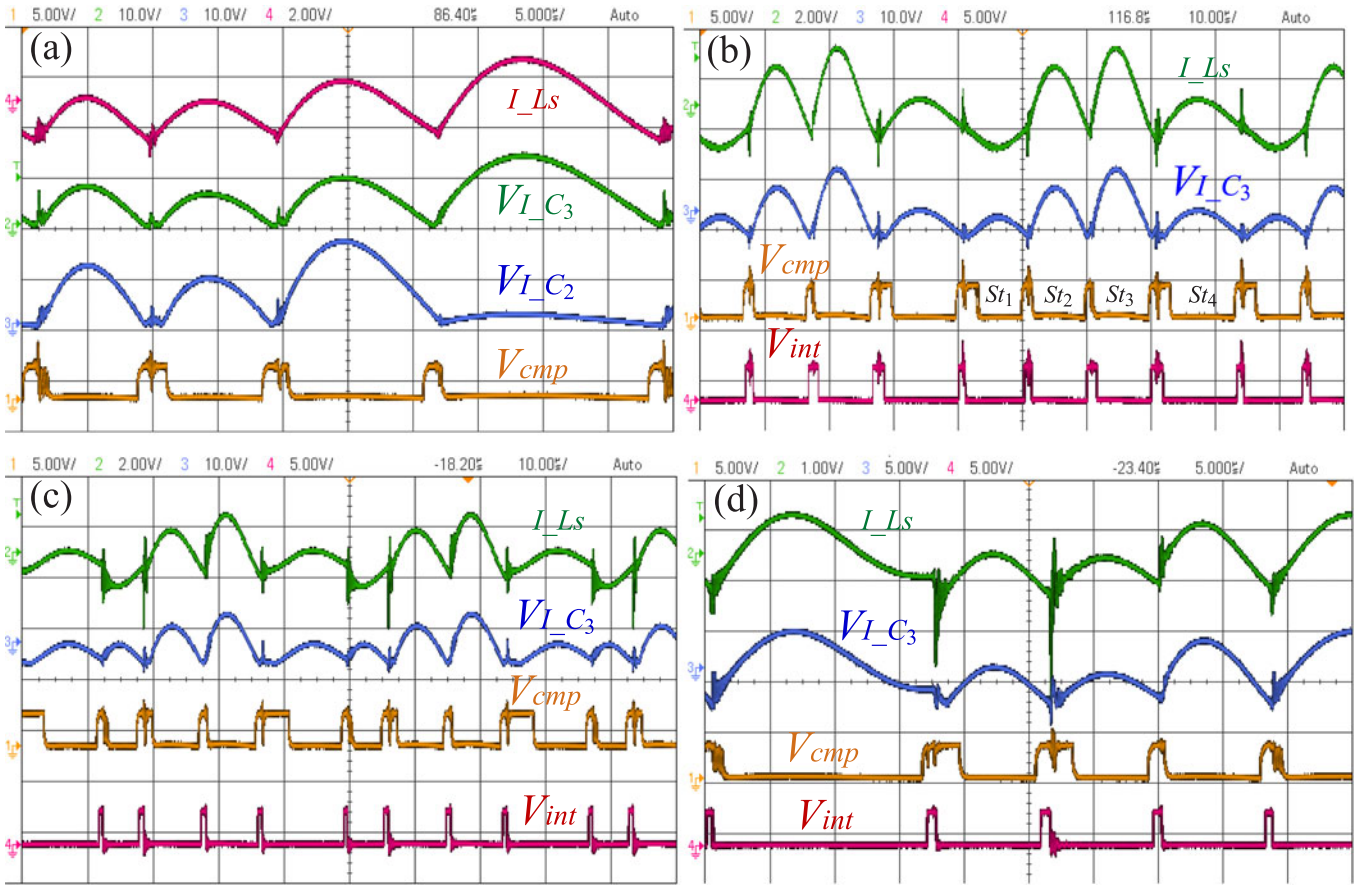


Fig. 9. Experimental result of the binary converter operating in active ZCS mode for various conversion ratios. (a) $M = 1/8$, $V_{in} = 80$ V, $P_{\rm out} = 31.3$ W, $\eta = 0.85$; traces top to bottom: inductor current I_{Ls} (0.8 A/div), rectified sensed voltage resulting from Ic_3, V_{Ic3} (10 V/div), rectified sense voltage resulting from Ic_2, V_{Ic2} (10 V/div), comparator output, $V_{\rm cmp}$ (5 V/div). Horizontal scale (5 μs/div). (b) $M = 3/8$, $V_{\rm in} = 100$ V, $P_{\rm out} = 76.5$ W, $\eta = 0.92$; traces top to bottom: I_{Ls} (0.8 A/div), V_{Ic3} (10 V/div), $V_{\rm cmp}$ (5 V/div), interrupt status $V_{\rm int}$ (5 V/div). Horizontal scale (10 μs/div). (c) $M = 5/8$, $V_{\rm in} = 80$ V, $P_{\rm out} = 73$ W, and $\eta = 0.95$. Traces and horizontal scale: as in (b). (d) $M = 7/8$, $V_{\rm in} = 80$ V, $P_{\rm out} = 131.7$ W, and $\eta = 0.99$. Traces top to bottom: I_{Ls} (0.4 A/div), V_{Ic3} (5 V/div), $V_{\rm cmp}$ (5 V/div), $V_{\rm int}$ (5 V/div). Horizontal scale (5 μs/div).

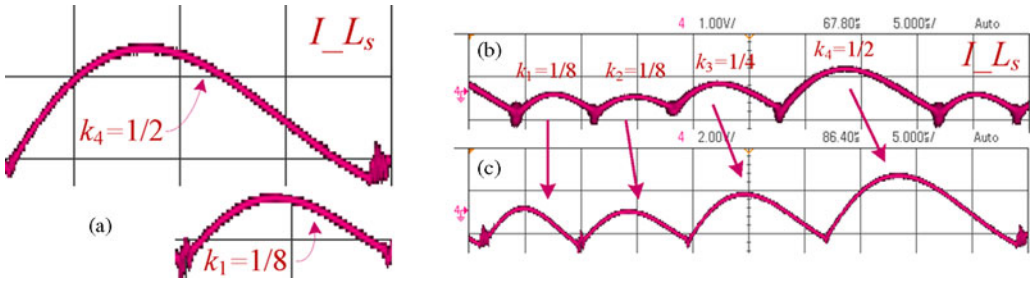


Fig. 10. (a) Slope difference between the highest and the lowest current pulses at fixed output power: 31.3 W, $I_o = 3.6$ A. (b) and (c) Slope differences between pulses at wide output power range, $P_o = 5$ W, $I_o = 1.7$ A and $P_o = 31.3$ W, $I_o = 3.6$ A, respectively.

$R_{\rm eqT}/R_{\rm loop} \approx 2.7$) for 3/8 and 1/8, while the measured $R_{\rm eqT}$ were 1 and 0.37 Ω, respectively. It should be noted that the discrepancies are due to asymmetrical layout of the subcircuits.

V. Discussion and Conclusion

An active ZCS method that allows resonant operation of binary and Fibonacci step-up/down switch-capacitor converter was developed and tested experimentally. For high-frequency resonant operation, the stray inductances of the circuit can be used. To lower the frequency of operation a single air-core inductor in series to the output stage was added. Consequently, the workload requirements from the digital processor are eased, and a realization with a simple, low-cost controller is feasible.

The active zero current cross detection was found to accurately adjust the switching times for four different RCL subcircuits dictated by the EXB/SFN codes. The current sensing

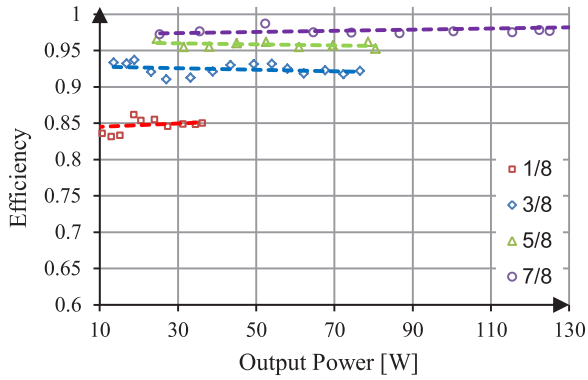


Fig. 11. Measured efficiency, M = 1/8–7/8, constant R_o, $V_{\rm in}$ = 30–80 V.

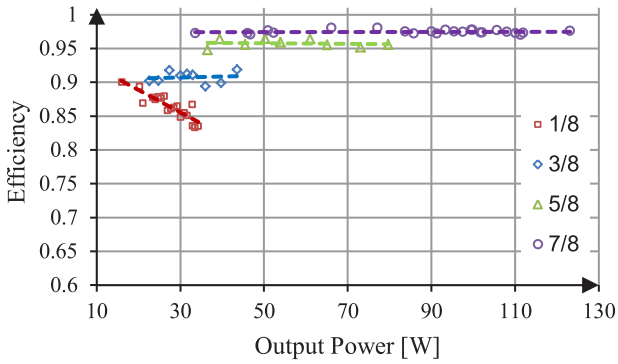


Fig. 12. Measured efficiency, M = 1/8–7/8, constant $V_{\rm in}$ = 80 V.

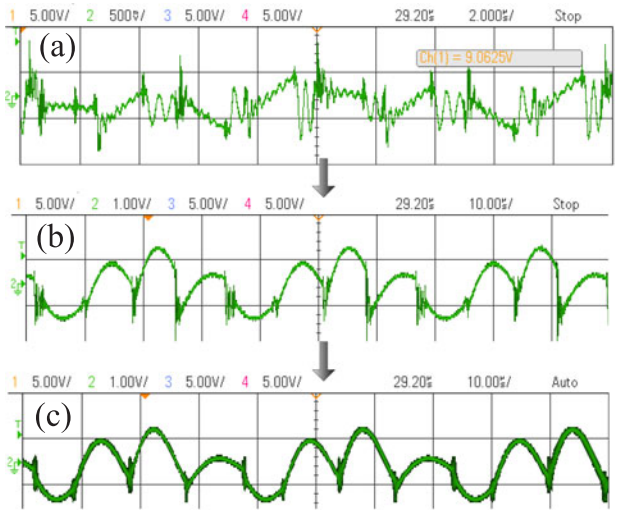


Fig. 13. Experimental results of the inductor current for the soft-start method for M = 3/8: (a) High switching frequency; (b) estimated resonant values; and (c) active ZCS method.

mechanism was implemented using three current transformers strategically mounted after the capacitors to avoid measurement of the output current that includes a dc component.

The major challenge in the design of a resonant binary SCC is the significant variation in switching times that is required for soft-switching operation. This variation is present when switching between one subcircuit to another which may involve different number of capacitors in series, and therefore, changes the resonant period. Another source for different resonant periods is that the capacitance and inductance values are strongly dependent on the operating conditions. This means that the time period of a given subcircuit is not constant for variations in the power level or the input voltage, and rules out any non-instantaneous ZCS or pre-calibrated resonant operation. The experimental validation confirmed that conjecture and highlighted the advantages of an active method. It revealed that the changes in the resonant period within a subcircuit are significant and may vary up to 30% for the operation range tested. It has also been established that although the resonant periods vary considerably, the slope of the sensed current in the vicinity of the zero crossing point is less prone to variations. Therefore, for the case of the binary SCC, the method can be further simplified by fixed reference voltage settings. This eliminates the need for additional fast compensation loop to vary the reference voltage.

The experimental results also support the need for a dynamic wide-range reference voltage in order to compensate for processing delay and different current levels of each subcircuit. Since a reasonable SNR is required, the reference to the comparator was kept constant (well above zero) and the reference was changed by the effective sensing gain. This was done by resistor dividers of the sensed signal and may be useful for implementation in other resonant switch capacitor topologies.

Study on the efficiency was carried out. It was found that although the calculated [12] equivalent resistance is the lowest at the ratio of 1/8, that ratio provides the poorest efficiency. Moreover, the efficiency increases for smaller conversion ratios (larger fractions). This behavior is intuitively explained by the fact that higher ratios (such as 1/8, 3/8) have higher rms current for a given transferred power and hence the power losses will be higher. This can be illustrated by rewriting the well-known SCC efficiency expression as a function of the output current, i.e., $\eta = V_o/V_{\rm in} = (V_o/I_o)/(V_o/I_o + R_{\rm eqT})$. This implies that for a given power level, the load resistance of larger ratios (smaller fractions) such as 1/8 is significantly smaller the efficiency is expected to drop per-unit of transferred power. Another observation on the efficiency and the expected equivalent resistance is made by the current waveforms and from the solution for the average currents for each subcircuit. It shows that for some conversion ratios, there might be a subcircuit in which the current is negative. This phenomenon can be explained from a charge-balance perspective and is given in Section II. However, from efficiency and $R_{\rm eqT}$ point of view, that means that for that particular subcircuit, current flows from the output into the system which may affect the estimations of $R_{\rm eqT}$ and the expected efficiency. A detailed analysis of this topic is beyond the scope of this paper and will be detailed in subsequent publications.

The method presented in this study has been verified to successfully operate resonant binary SCC and to accommodate wide and dynamic operation range, and therefore can be applied to other multiphase SCC topologies that involve number of subcircuits and wide operation range.

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