Modeling and Analysis of Resonant Switched-Capacitor Converters With Free-Wheeling ZCS

Eli Hamo, *Student Member, IEEE*, Michael Evzelman, *Student Member, IEEE*, and Mor Mordechai Peretz, *Member, IEEE*

***Abstract*—This paper introduces a unified modeling methodology to describe and explore the loss mechanism of resonant switched-capacitor converter (SCC) operating in a self-commutation zero current switching (ZCS) mode. The conventional equivalent resistance concept, which assumes a single conduction path of the resonant current, is generalized and extended to model the losses in cases where the resonant current is divided across several conduction loops. The new modeling concept is compatible to describe the losses resulting from resistive elements as well as P–N junction devices, offering a solution for the equivalent resistance. Verification of the concept has been carried out by simulations and experiments on 3–30 W unity, double gain and multiphase Fibonacci resonant SCC with free-wheeling ZCS. A very good agreement is obtained between the theoretical calculations, simulations, and experimental results, well demonstrating model capability to identify the loss contributors in each conduction path.**

***Index Terms*—DC-DC power converters, modeling, soft switching, switched capacitor circuits, switched-mode power supply, zero current switching.**

I. Introduction

IN RESONANT switched-capacitor converters (RSCC), zero current switching (ZCS) is mandatory to achieve high power conversion efficiency and reliability. ZCS can be achieved by employing an active monitoring and control of the resonant current [1], [2] which requires complex control scheme and circuitry. Alternatively, ZCS can be obtained by unidirectional switches, e.g., inserting a diode in series to the active switch. In this case, ZCS is assured by simple means at the cost of increased conduction losses. To overcome the deficiencies of these methods, a simple and efficient self-commutation concept as illustrated in Fig. 1 has been presented in [3]–[5]. It consists of a transistor that conducts for the majority of the resonant cycle, and a parallel diode that acts as a free-wheeling element such that turn off occurs at zero current. This method exhibits both advantages of inherent ZCS and overcomes the deficiencies of previous methods such as high conduction losses and complex control hardware. However, due to a divided conduction path (DCP) of the resonant current (see Fig. 1), the conventional equivalent resistance method for loss evaluation [6]–[9] cannot be applied directly in this case.

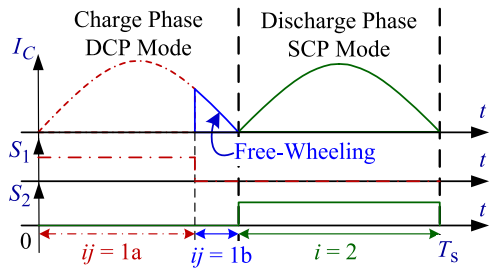

Fig. 1. Typical resonant current waveforms during a: charge phase—DCP operation, discharge phase—SCP operation.

The objective of this paper is to describe and explore the loss mechanism of resonant SCC operating in a self-commutation ZCS mode.

The new modeling methodology extends the modeling concept employed in [6]–[18], to take into account the DCP of a single charge/discharge state.

The deliverables of this modeling approach are on both theoretical and practical realms; it provides a streamlined procedure to design a reliable and low-cost soft-switched SCC, as well as an insight into the dominant contributors of losses in DCP operation mode.

The rest of this paper is organized as follows: Section II details the terminology and basic definitions to the approach of this study; the modeling methodology is delineated in Section III; Section IV derives the loss contributors; Section V provides a rigorous validation of the modeling concept, and finally, this paper is concluded in Section VI.

II. Basic Terminology and Definitions

Throughout this paper, the modeling concept will be explained on a unity gain resonant SCC (see Fig. 2). Even though the exemplary circuit is not the best candidate to showcase the strength of ZCS, it highlights the mechanism of DCP operation and is therefore selected.

Resonant SCC that operates in open loop can be represented by an equivalent circuit [19]–[29], which consists of a target voltage source V_T that represents the no load output voltage of the converter, and a series equivalent resistance R_e that stands

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The authors are with the Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 8410501, Israel (e-mail: eliham@post.bgu.ac.il; evzelman@ee.bgu.ac.il; morp@ee.bgu.ac.il).

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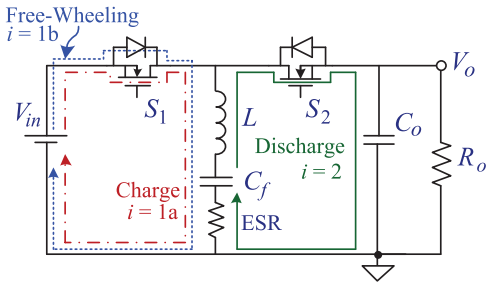

Fig. 2. Unity gain SCC with free-wheeling ZCS of the charge state.

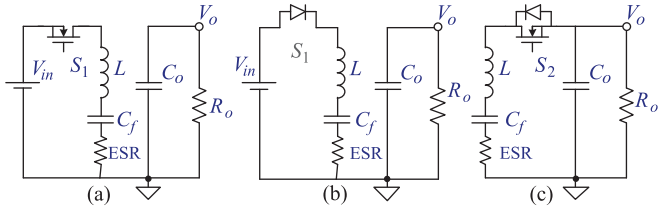

Fig. 3. Operation states of unity gain SCC (see Fig. 2): (a) charging substate $ij = 1\text{a}$, (b) charging substate $ij = 1\text{b}$, and (c) discharging state $i = 2$.

for the conduction losses caused by the current flow in the series resistances of the capacitor's charge/discharge path.

Self-commutated unity gain SCC (see Fig. 2) operates in two phases. The charging phase is split into two substates, as marked in the timing diagram in Fig. 1. First, the switch S_1 is turned on, and the capacitor C_f is charged resonantly. Next, approaching the end of half-resonant cycle, S_1 is turned off, and the free-wheeling diode conducts until the current reaches zero. The second phase starts by turning S_2 ON, and C_f resonantly discharges onto the output.

To facilitate systematic analysis, the following definitions and terminology are used: *phase*—relates to a time period of half-resonant cycle, e.g., *charging phase* or *discharging phase* (see Fig. 1), denoted by a numerical index $i = 1, 2 \ldots$; *substate*—a portion of a *phase*, denoted by an alphabetical index $j = a, b \ldots$; *single conduction path* (SCP)—a *phase* that includes one *substate* only; DCP—a *phase* that includes more than one *substate*. For example, substate "a" at phase 1 (red lines marked with dashed-dot in Figs. 1 and 2) will be denoted as $ij = 1\text{a}$.

III. Modeling Approach

The generic approach to extract the equivalent model of a resonant SCC operating in the particular case of SCP has been presented in [6]–[9]. Generalization of the model to include a DCP operation requires the following steps: first, based on the switching sequence applied to the SCC, each phase is described by one or more substates according to the operation mode (SCP or DCP). Given the example on hand, the operation of SCC in Fig. 2 is represented by three subcircuits, that is, a charging substate by the transistor conduction [see Fig. 3(a)], a charging substate by the free-wheeling diode [see Fig. 3(b)], and a discharge phase [see Fig. 3(c)].

Second, each of the subcircuits is simplified to a lumped *RLC* circuit as shown in Fig. 4. This circuit is used to describe the

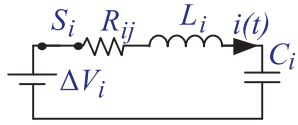

Fig. 4. Basic and generic instantaneous *RLC* subcircuit.

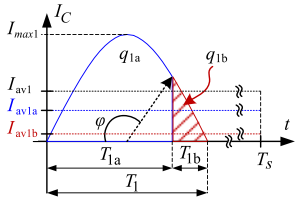

Fig. 5. DCP switching phase current waveform.

operation of each subcircuit in its relevant conduction time, where ΔV_i is the initial voltage difference between the charging/discharging source and the resonant tank voltage, R_{ij} is the total loop resistance (switch resistance R_{Si}, inductor resistance R_{Li} and capacitor ESR), and C_i and L_i are the total capacitance and inductance of the loop, respectively.

The next step applies the calculation of the power loss P_{ij} due to the series resistances R_{ij} of each substate, and expressing it as a function of the average capacitor current I_{avi}. The average capacitor current of each phase is linearly proportional to the average output current [6], [23], [24]. By doing so, the power dissipated in each phase is referenced to the output current, using the proportionality factor k_i. The equivalent resistances of each substate R_{eij} are then extracted from the dissipated power P_{ij}. It should be noted that by addressing the model calculation from the average current domain, the calculation of ΔV_i, which primarily depends on the capacitors value and the operating frequency, is eliminated [6]–[8].

The general case of DCP applies a free-wheeling mode that is realized by the diode conduction. Since the dominant loss contributor of the diode is the average current, an additional proportionality factor is required to relate the average substate current to the total average current of the phase in which it exists (see Fig. 5). In this study, this factor is referred as ρ_{ij}, and the relationship between the average currents can now be expressed as follows:

$$I_{av1\text{a}} = \rho_{1\text{a}} \cdot I_{av1}; \quad I_{av1\text{b}} = \rho_{1\text{b}} \cdot I_{av1}, \tag{1}$$

where $I_{\text{av}1}$ is the phase current, which equals to the sum of the average capacitor currents during each substate $I_{\text{av}1\text{a}}$ plus $I_{\text{av}1\text{b}}$. The relationship between the average currents to the output current is obtained by substituting $I_{\text{av}1} = k_1 I_{\text{out}}$ in (1), that is

$$I_{\text{av}1\text{a}} = \rho_{1\text{a}} k_1 \cdot I_{\text{out}}; \; I_{\text{av}1\text{b}} = \rho_{1\text{b}} k_1 \cdot I_{\text{out}}, \tag{2}$$

where k_1 is the proportionality factor of the charge phase.

It should be noted that the averaging method applied here considers the contribution of the substate average current on the entire switching period, that is

$$I_{\text{av}i} = \frac{q_i}{T_s}; \quad I_{\text{av}ia} = \frac{q_{ia}}{T_s}, \tag{3}$$

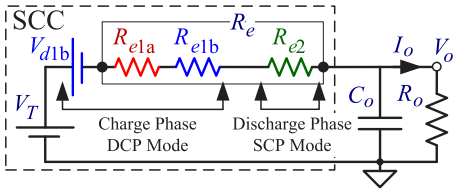

Fig. 6. SCC generic average equivalent circuit that shows the contribution of the partial subcircuits equivalent resistances R_{ei} to the total equivalent circuit resistance R_e. For the unity gain SCC example of Fig. 2, R_{e1a} is the loss contribution of charge substate 1a, R_{e1b} and V_{d1b} are the resistive and diode loss contribution of the free-wheeling sub-state, respectively, and R_{e2} is the loss contribution of discharging phase.

where q_i is the total charge of the *i*th phase, q_{ia} is the charge of the substate "a" while commutated at the angle $\varphi_i = \pi \cdot T_{ia}/T_i$ (see Fig. 5). Therefore, the diode loss contribution can be represented as a function of the phase current, i.e., by a voltage source V_{dij} that takes into account the partial average current in the substate as follows:

$$V_{dij} = k_i \cdot \rho_{ij} \cdot V_{Fij}, \tag{4}$$

where V_{Fij} is the average voltage drop across the diode due to current through it at substate, *j*, in phase, *i*.

Finally, the model is constructed by considering a series connection of the equivalent resistances R_{eij} and the voltage source V_{dij} between the target voltage and the output port. As a result, the SCC in Fig. 2 operating in DCP mode is represented by the average equivalent model circuit of Fig. 6.

IV. Extraction of Equivalent Resistances and Equivalent Average Voltage Drop

Following the modeling methodology described earlier, the equivalent resistance value is extracted in this section. It is assumed that each *RLC* substate (see Fig. 4) operates under ZCS conditions, and the quality factor Q_{ij} is sufficiently high ($Q_{ij} > 5$).

The peak currents I_{pkij} of the substates are considered equal to the charge phase peak current I_{pki}. For the case of the circuit in Fig. 2, this applies the following:

$$I_{pki} = I_{pkia} = I_{pkib}, \tag{5}$$

where I_{pki}, I_{pkia}, and I_{pkib} are the potential peak currents that are, or could be developed given the conditions of the switching phase *i*, or the substate *j*, *i*a, and *i*b, respectively.

A. Equivalent Resistance Calculation

The energy E_{ia} dissipated in the subcircuit due to the loop resistance R_{ia} (see Fig. 4) and the current during the time interval T_{ia} (see Fig. 5) is derived by integrating the instantaneous power $p(t) = {i_C}^2(t) \cdot R_{ia}$($i_C(t)$ is the capacitor current) over the substate time interval, T_{ia}:

$$\begin{aligned} E_{ia} &= R_{ia} \cdot (I_{pki})^2 \cdot \int_0^{\varphi_i/\omega_{0ia}} [\sin(\omega_{0ia}t)]^2 \, dt \\ &= R_{ia} \cdot (I_{pki})^2 \cdot \frac{(\varphi_i - \cos(\varphi_i)\sin(\varphi_i))}{2\omega_{0ia}}, \end{aligned} \tag{6}$$

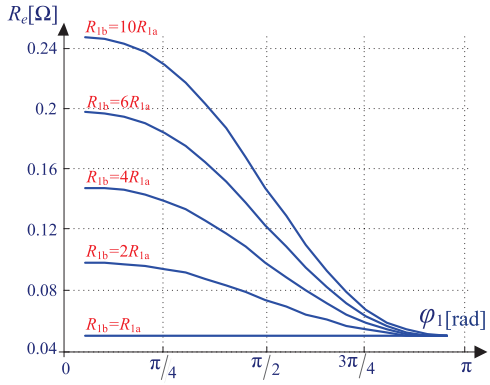

Fig. 7. Variation of R_e as a function of φ_1 for different ratios of loop resistances between R_{1a} and R_{1b}. In the example above, $R_{1a} = R_2 = 10$ mΩ.

where $\omega_{0ia} = 2\pi f_{0ia}$ is the natural resonant frequency of the phase *i*, substate "a." The relationship between the peak current and the average current of phase, *i*, can be expressed as follows:

$$(2/\pi) \cdot I_{pki} = I_{avi} \cdot (2 \cdot \mathrm{df}_i), \tag{7}$$

where $\mathrm{df}_i = f_s/f_{0i}$ is the ratio between the switching frequency and the natural frequency of the resonant network [6].

Substituting (2) and (7) into (6), and after some manipulations, the power loss of the substate can be expressed as a function of the average output current I_o by

$$P_{ia} = (I_o)^2 \cdot k_i^2 \frac{\pi \cdot R_{ia}}{4 \cdot \mathrm{df}_i} \cdot (\varphi_i - \cos(\varphi_i)\sin(\varphi_i)). \tag{8}$$

To comply with the equivalent model (see Fig. 6), the equivalent resistance of the substate, *i*a, is extracted from (8) to be:

$$R_{eia} = k_i^2 \frac{\pi \cdot R_{ia} \cdot \varphi_i}{4 \cdot \mathrm{df}_i} (1 - \sin c(2\varphi_i)). \tag{9}$$

Fig. 7 shows various curves of (9) for different ratios of loop resistances between substates 1a and 1b, demonstrating the change of R_e as a function of charge phase commutation angle φ_1. The losses per a DCP phase (either charging or discharging) are inversely proportional to the commutation angle, i.e., decreases with the reduction of the free-wheeling substate. From an efficiency point of view, this provides an insight into the practical commutation angles that may be used to assure ZCS without a significant increase in the conduction losses. As can be conjectured from Fig. 7, a good practical commutation angle would be in the range of 0.85π, which is satisfactory for wide range of loop resistances. The results of Fig. 7 may also assist in the selection of the transistors, given a target efficiency of the practical converter.

In a similar manner, all the equivalent substate resistances can be extracted using the steps described above. Alternatively, for the case of a complementary free-wheeling action, the equivalent resistance can be derived by substituting the commutation angle φ_i, by the complementary one $(\pi - \varphi_i)$.

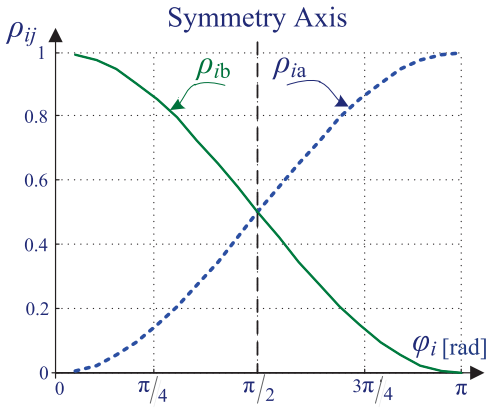

Fig. 8. Distribution of the charge through paths *i*a and *i*b as a function of the commutation angle φ_i.

Naturally, for the particular case of SCP (discharging phase, $i = 2$), the calculations are carried out with $\varphi_i = \pi$, that is

$$R_{ei} = k_i^2 \frac{\pi^2}{4 \cdot \mathrm{df}_i} R_{ia}. \tag{10}$$

As can be observed, expression (10) derived using the generalized approach of this study is in agreement with the SCP modeling methodology previously reported in [6]–[9].

B. Equivalent Average Diode Voltage-Source Calculation

Following Fig. 5, the proportionality factor, ρ_{ia}, that represents the ratio between the charge transferred via substate *i*a, and the total charge via phase *i*, can be derived as follows:

$$\rho_{ia} = \frac{q_{ia}}{q_i} = \frac{I_{pkia} \int_0^{\varphi_i/\omega_{0i}} \sin(\omega_{0i} t)\, dt}{I_{pki} \int_0^{\pi/\omega_{0i}} \sin(\omega_{0i} t)\, dt} = \sin^2(\varphi_i/2). \tag{11}$$

The complementary proportionality factor in the case of two substates in one phase is $\rho_{ib} = 1 - \rho_{ia}$. As can be seen from Fig. 8, symmetry exists in the charge distribution through paths *i*a and *i*b below and above the point of $\varphi_i = \pi/2$.

In the general case of multiple phases with free-wheeling diodes, the effective average equivalent voltage drop V_d can be obtained by summation of (4) for all the contributing substates, and expressed as follows:

$$V_d = \sum_{i,j=1,\mathrm{a}}^{m,n} k_i \cdot \rho_{ij} \cdot V_{Fij}, \tag{12}$$

where *m* is the total number of switching phases, and *n* is the total number of substates per phase *i*.

Another potential contributor to losses in resonant SCC is the time delay between consecutive phases, i.e., the time duration between the current zero crossing of the free-wheeling diode and the initiation of the next phase. Ideally, the next commutation phase is to start immediately when the current is zero; otherwise, a zero current period exists that influences the total efficiency of the system [1]. The model presented in this study is well-suitable for quantifying this effect by employing the ratio factor df, which represents the ratio between the switching frequency and the natural frequency of the resonant network [6]. This implies

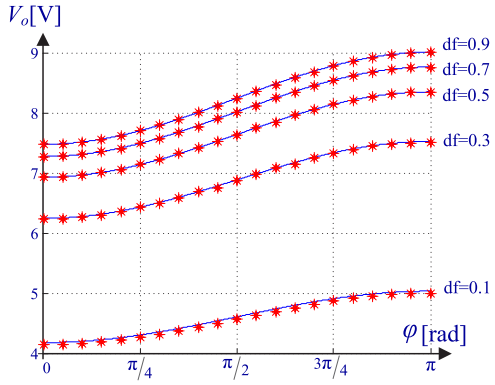

Fig. 9. Output voltage of a unity gain SCC as a function of the commutation angle φ. Model calculation—solid trace, simulation—asterisk marks. $V_{\mathrm{in}} = 10$ V, $V_F = 1.7$ V, $R_{\mathrm{DS(on)}} = 100$ mΩ, $R_o = 5\ \Omega$, $Q \approx 30$, and $f_0 \approx 5$ kHz.

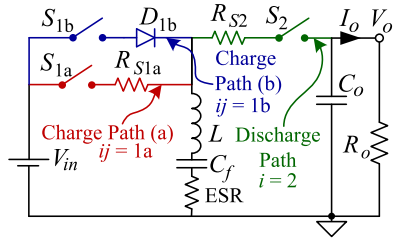

Fig. 10. Unity gain SCC switching circuit, with charge phase operated in a DCP mode. (Switch $S_{1\mathrm{b}}$ blocks undesired conduction paths).

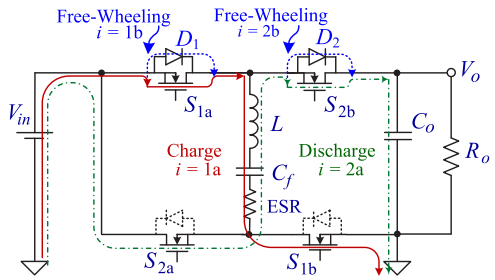

Fig. 11. Voltage doubler converter topology with free-wheeling diodes D_1, D_2. Charge phase: $S_{1\mathrm{a}}$, $S_{1\mathrm{b}}$—ON, discharge phase: $S_{2\mathrm{a}}$, $S_{2\mathrm{b}}$—ON.

that the losses due to the time delay are inversely proportional with df. An application example of this factor in the model is presented in Fig. 9, which shows the curves of the expected output voltage as a function of the commutation angle φ_i for several time delay settings. As expected, the output voltage is lower with the increase of the zero current period added between the phases.

V. Simulation and Experimental (Model Validation)

To validate the proposed model, two experimental prototypes were constructed. In the first prototype, a unity gain RSCC depicted in Fig. 10 was evaluated to confirm the analytical derivation. The second experiment demonstrated strength of the modeling methodology by considering a voltage doubler RSCC configuration, as shown in Fig. 11. For both configurations, the proportionality factors were $k_{1,2} = 1$, and the frequency ratio $\mathrm{df}_{1,2}$ was 1.

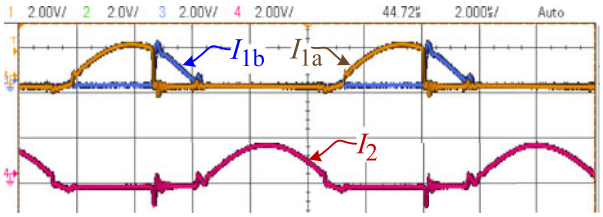

Fig. 12. Experimental waveforms obtained from a unity gain resonant SCC operating in DCP mode with $\varphi_i \approx 126°$. Upper traces—charge substates currents, bottom trace—discharge current. Scale: vertical—2 A/div, horizontal—2 μs/div.

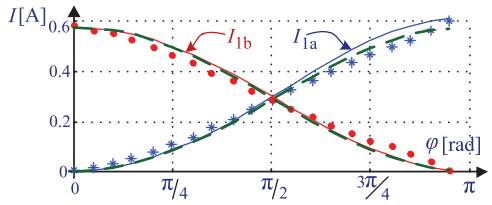

Fig. 13. Average currents at paths 1a and 1b. Model calculation—solid trace, simulation—dashed line, and experimental results—(I_{1a}) asterisk marks and (I_{1b}) circle marks.

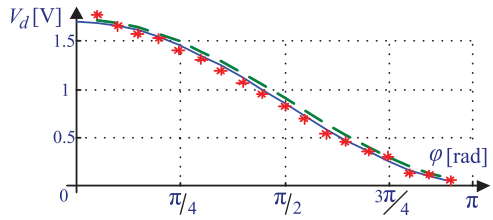

Fig. 14. Equivalent average diode voltage drop, V_d, as a function of the commutation phase φ. Model calculation—solid trace, simulation—dashed line, and experimental results—asterisk marks.

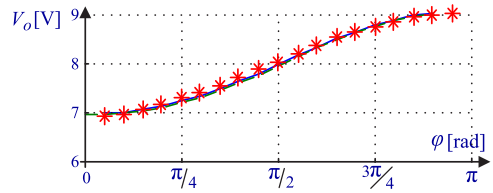

Fig. 15. Output voltage as a function of the commutation phase φ. Model calculation—solid trace, simulation—dashed line, and experimental results—asterisk marks.

A. Unity Converter

The experimental setup and simulation test bench parameters were: quality factor of the resonant tank was maintained above 20, and output power range was between 3 and 30 W. Fig. 12 shows typical waveforms of the substate currents demonstrating DCP operation. As can be observed, the phase current is commutated between two substates.

Three sets of experiments were carried out. In the first experiment, extraction of the equivalent resistance following the procedure detailed by expression (9) is verified. In this experiment, the free-wheeling diode, D_{1b}, was omitted, and replaced by additional resistive conduction path using the transistor, S_{1b}, (the ratio of R_{1b}/R_{1a} was approximately 10) (see Fig. 10). Fig. 13 shows the experimental results of the average currents at paths 1a and 1b as a function of the commutation phase φ, and the agreement to the theoretical calculations and the simulation derived results.

In the second experiment, the capability of the model to include diode losses was evaluated by implementing D_{1b} (see Fig. 10) using two diodes connected in series. The total average forward voltage drop V_F of the two diodes at nominal current was estimated to be 1.7 V. Furthermore, to emphasize the voltage drop effect, all other loss contributors were made negligibly small. Fig. 14 shows results of the average equivalent diode voltage drop, V_d, as a function of the commutation angle, φ, obtained from model calculations, simulations, and experimental measurements.

The third experiment summarizes the validity of the modeling methodology by considering both diode as well as resistive losses. This is done by changing the free-wheeling loop to include two diodes, as well as loop resistance R_{1b} (R_{1b}/R_{1a} was approximately 10) such that both elements contributed approximately equal amount of losses. Fig. 15 shows the values of the output voltage predicted by the model, simulation results, and experimental measurements.

B. Voltage Doubler SCC

The experimental and simulation results were obtained for several values of quality factors, commutation angles, φ_i on both the charge phase ($i = 1$) and the discharge phase ($i = 2$), average voltage drop, V_F, and loops resistances. Also added in this experiment is a case of a voltage doubler with self-commutation (DCP mode) in both the charging and discharging phases. Figs. 16–18 show an example of the charge and discharge substates current waveforms, demonstrating DCP operation of the converter. The output voltage ripple remained constant throughout the experiments and was measured to be around 200 mV. The experimental parameters and comparison of the results to the one obtained from the modeling methodology are summarized in Table I, where charge/discharge substates that include diodes are marked by the index "b." The model used to predict the output voltage value for this experiment is depicted in Fig. 19. A very good agreement was found between the values predicted by the model and the experimental results (deviation of less than 1%). It should be noted that the reason for the relatively high inductance value that has been used for the experiments is to allow model validation by the insertion of nonnegligible series resistances to the loop while maintaining sufficiently high quality factor as required by the assumptions of the modeling approach. For practical application with lower on-resistance switches, the values of the passive components will comply with the commonly used values.

C. Multiphase Fibonacci Resonant SCC

To further demonstrate the strength of the modeling methodology to predict the origin of the conduction losses, a multiphase Fibonacci-type resonant SCC [23] has been examined by simulation and compared to the results of the presented model. The converter in Fig. 20 includes four conduction phases to build

TABLE I
VOLTAGE DOUBLER CONVERTER—SUMMARY OF EXPERIMENTAL RESULTS AT $V_{\rm in} = 10$ V, $C_i = 440$ nF, $L_i = 46$ μH, $C_o = 100$ μF, AND $f_s = 35$ kHz

Parameters \ φ_i [degrees]	$\varphi_1 = 103$ $\varphi_2 = 139$	$\varphi_1 = 149$ $\varphi_2 = 139$	$\varphi_1 = 90$ $\varphi_2 = 90$	$\varphi_1 = 90$ $\varphi_2 = 131$	$\varphi_1 = 123$ $\varphi_2 = 131$	$\varphi_1 = 150$ $\varphi_2 = 134$	$\varphi_1 = 90$ $\varphi_2 = 90$	$\varphi_1 = 139$ $\varphi_2 = 139$
$R_{\rm loop1a}$, $R_{\rm loop2a}$ [mΩ]	100	100	370	370	370	370	700	700
$R_{\rm loop1b}$, $R_{\rm loop2b}$ [mΩ]	100	100	100	100	100	100	100	100
$Q_{\rm 1a,2a\_}$ (worst case)	102	102	27	27	27	27	14.6	14.6
V_F (D_1, D_2) [V]	1.7	0.85	1.7	1.7	1.7	1.7	1.7	1.7
R_o [Ω], P_o [W]	30, 11.4	50, 7.7	30, 10	30, 10.6	30, 10.9	30, 11.3	30, 9.5	30, 10.2
Efficiency	0.91	0.96	0.86	0.88	0.89	0.91	0.83	0.86
V_o (DC) Simulation [V]	18.83	19.63	17.61	18	18.31	18.54	17.14	17.65
V_o (DC) Experimental [V]	18.7	19.76	17.5	18	18.24	18.5	17	17.63
V_o (DC) Model [V]	18.79	19.65	17.62	18.18	18.36	18.46	17.12	17.67

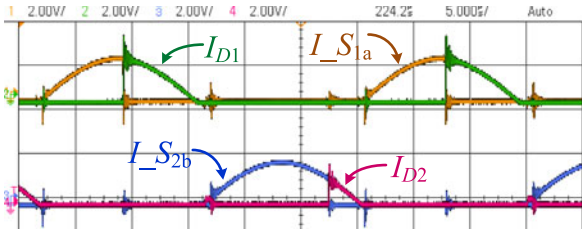

Fig. 16. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\varphi_1 \approx 96°$, $\varphi_2 \approx 139°$, $V_{\rm in} = 10$ V, $R_{\rm loop1a,2a} = 370$ mΩ, $R_{\rm loop1b,2b} = 100$ mΩ, $V_{\rm F1,2} = 1.7$ V, $P_{\rm out} = 10.6$ W. Upper traces—charge substates currents, bottom trace—discharge substates currents. Scale: vertical—2 A/div, horizontal—5 μs/div.

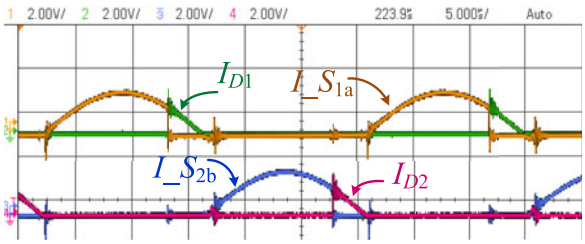

Fig. 17. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\varphi_1 = \varphi_2 \approx 139°$, $V_{\rm in} = 10$ V, $R_{\rm loop1a,2a} = 370$ mΩ, $R_{\rm loop1b,2b} = 100$ mΩ, $V_{\rm F1,2} = 1.7$ V, and $P_{\rm out} = 11.13$ W. Upper traces—charge substates currents, bottom trace—discharge substates currents. Scale: vertical—2 A/div, horizontal—5 μs/div.

the output voltage up by eight times the input voltage. To obtain free-wheeling ZCS operation, each commutation phase includes a DCP mode as can be observed from the current waveforms in Fig. 21.

The transistors have been assigned with identical on-resistances, yielding the following per-phase resistances: $R_{\rm loop1} = 2R_{\rm DSon}$, $R_{\rm loop2} = 3R_{\rm DSon}$, $R_{\rm loop3} = 4R_{\rm DSon}$, and $R_{\rm loop4} = 4R_{\rm DSon}$. The proportionality factors are $k_1 = 4$, $k_2 = 2$, $k_3 = k_4 = 1$, and the frequency ratio df_{1-4} is 1.

Validation of the model is carried out by simulation considering both the diode as well as resistive losses. Fig. 22 shows the values of the output voltage predicted by the model compared with the results of a cycle-by-cycle simulation. The target parameters of the multiphase Fibonacci SCC simulations are as follows: $V_{\rm in} = 5$ V, $V_{\rm F1-4} = 1.7$ V, $R_{\rm DS(on)} = 10$ mΩ, $R_o = 50$ Ω, $L_{\rm S} = 2.1$ μH, $C_i = 10$ μF, and $f_s \approx 24$ kHz. Very good

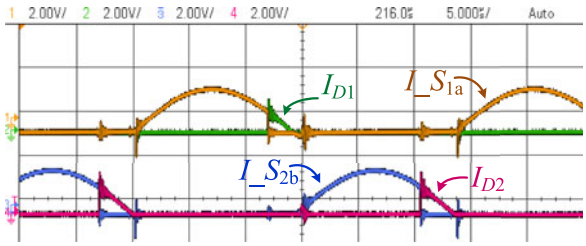

Fig. 18. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\varphi_1 \approx 148°$, $\varphi_2 \approx 139°$, $V_{\rm in} = 10$ V, $R_{\rm loop1a,2a} = 370$ mΩ, $R_{\rm loop1b,2b} = 100$ mΩ, $V_{\rm F1,2} = 1.7$ V, and $P_{\rm out} = 11.3$ W. Upper traces—charge substates currents, bottom trace—discharge substates currents. Scale: vertical—2 A/div, horizontal—5 μs/div.

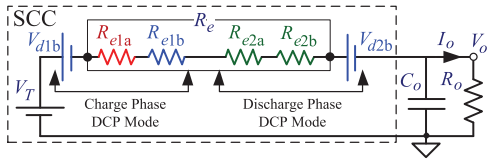

Fig. 19. SCC generic average equivalent circuit that shows the contribution of the partial subcircuits equivalent resistances R_{ei} to the total equivalent circuit resistance R_e. (For the doubler SCC example of Fig. 11, R_{e1a} is the loss contribution of charge substate 1a, R_{e1b} and V_{d1b} are the resistive and diode loss contribution of the free-wheeling substate, respectively. R_{e2a} is the loss contribution of the discharge substate 2a, R_{e2b} and V_{d2b} are resistive and diode loss contribution of the free-wheeling discharge substate, respectively).

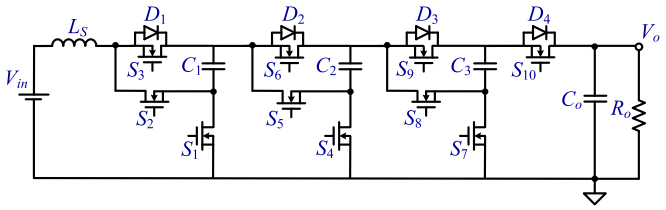

Fig. 20. Multiphase Fibonacci resonant SCC topology with free-wheeling diodes D_{1-4}. Phase 1: S_1, S_3—ON, Phase 2: S_2, S_4, S_6—ON, Phase 3: S_2, S_5, S_7, S_9—ON, Phase 4: S_2, S_5, S_8, S_{10}—ON.

agreement has been found between the values predicted by the model and the simulation results (maximum deviation of 1.5%). The results in Fig. 23(a) and (b) show the contribution of losses, separated to resistive and voltage drop parts.

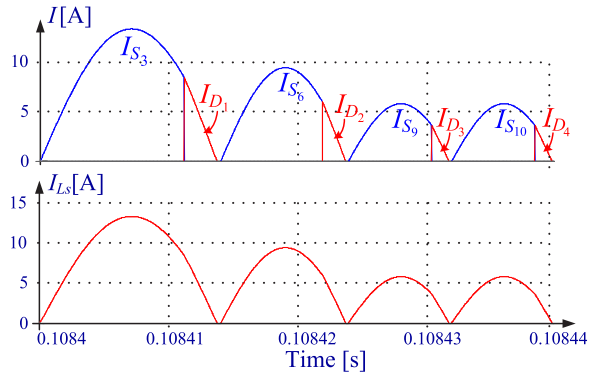

Fig. 21. Simulation waveforms obtained from a resonant Fibonacci SCC operating in DCP mode with $\varphi_i \approx 144°$.

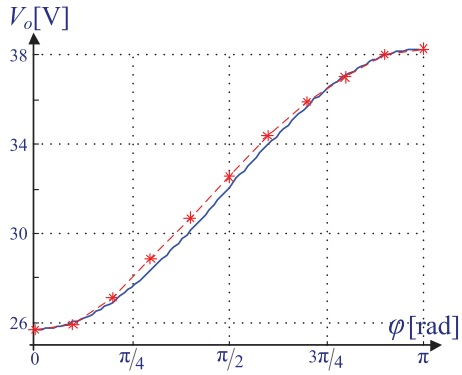

Fig. 22. Output voltage of the DCP operation mode of a resonant Fibonacci SCC as a function of the commutation angle φ. Model calculation—solid trace, simulation—asterisk marks.

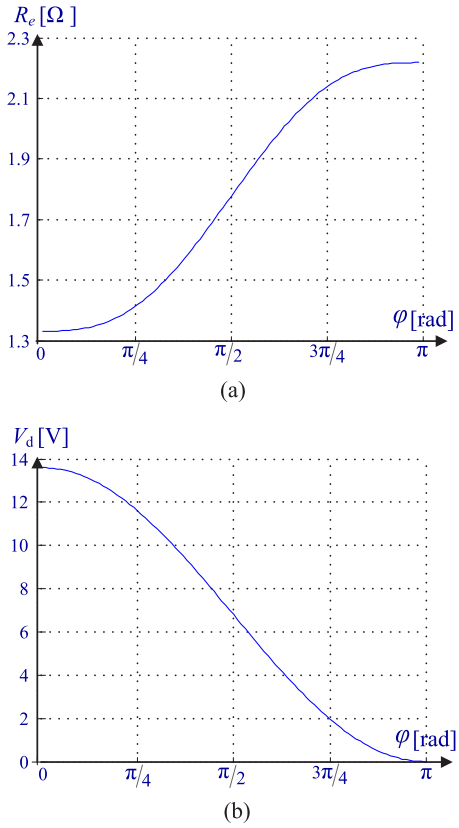

Fig. 23. Contribution of conduction losses of the resonant Fibonacci SCC operated in DCP mode. (a) Equivalent resistant R_e as a function of the commutation angle φ. (b) Equivalent average diode voltage drop V_d as a function of the commutation angle φ.

VI. Conclusion

This paper presented a modeling approach of resonant SCC that is applicable to both the conventional resonant operation as well as for converters that operate in the more general case of a DCP ZCS. The modeling concept applies representation of the resistive losses by partial equivalent resistance and losses originated from P–N junction devices, all with respect to the output current of the converter. Although rigorously demonstrated on a relatively simple case of two conduction paths, the modeling methodology is well-qualified to extract the behavior of a resonant SCC with any number of split current loops such as a resonant Fibonacci converter, exemplified in Section V-C. The resultant model is limited, however, within the assumptions specified, to resonant networks with relatively high quality factor, i.e., sinusoidal resonant current.

The experimental study confirmed the validity of the modeling method to distinguish between losses types (resistive and voltage drop) with excellent agreement between the analytical derivations, simulations, and experimental results. It was found that while the partial equivalent resistances are extracted as a function of the rms currents and the related commutation phase, the equivalent average diode voltage source depends primarily on the ratio between the substates charges (proportionality factor, ρ).

The overall efficiency in circuits operated in a DCP mode is highly dependent on the loss amount in each of the conduction paths. It is assumed throughout this work that switches with a resistive behavior, i.e., MOSFETs have lower conduction losses than devices based on a P–N junction, which is the case in modern power components for low and intermediate voltage conversion applications. Hence, there exists a tradeoff between the target efficiency and the component tolerances. Wider component variance from their nominal values results in higher uncertainty of the zero crossing point and longer duration of diode conduction path, which translates into higher losses. It should also be noted that from an efficiency point of view, the lossy diode-based conduction path is to be activated in the vicinity of zero current, so its contribution to the losses is minimized.

A self-commutation approach may not be compatible with all converter configurations, for example, converters where the voltage difference between input and output is higher than the forward voltage drop of the free-wheeling diode. Under these conditions, undesirable current paths may appear. It should be noted that the presented modeling methodology focuses on the dominant part of the contributing losses in resonant SCC and omits the discussion on other issues such as EMI effects, gate drive losses, etc.

The DCP operation mode can significantly simplify the control effort and eliminate the additional circuitry that is required to achieve ZCS in resonant converters and in particular for resonant SCC that require active zero current detection to improve the power conversion efficiency.

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Eli Hamo (S'12) was born in Ashdod, Israel, in 1978. He received the B.Sc. degree in electrical engineering from the SCE College of Engineering, Ashdod, in 2009, and is currently working toward the M.Sc. degree at the Ben-Gurion University of the Negev, Beer-Sheva, Israel.

His areas of interests include switch-capacitor dc–dc converters, modeling and resonant power conversion systems.

Michael Evzelman (S'09) received the B.Sc. degree in electrical and electronics engineering from the Samy Shamoon College of Engineering, Beer-Sheva, Israel, in 2006, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from Ben-Gurion University of the Negev, Beer-Sheva, in 2009 and 2014, respectively.

He is currently a Postdoctoral Researcher in the Department of Electrical and Computer Engineering, Utah State University, Logan, UT, USA. His work centers on analysis, management, and optimization of renewable dc sources and energy storage components. His areas of interests also include switched-capacitor converters, high-voltage low-power converters, and general modeling and simulation of switched-mode power circuits.

Mor Mordechai Peretz (S'05–M'12) was born in Beer-Sheva, Israel, in 1979. He received the B.Tech. degree in electrical engineering from the Negev Academic College of Engineering, Beer-Sheva, in 2003, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from Ben-Gurion University, Negev, Israel, in 2005 and 2010, respectively.

From 2010 to 2012, he was a Postdoctoral Fellow in the Laboratory for Power Management and Integrated SMPS, University of Toronto, Canada. In 2012, he joined the Department of Electrical and Computer Engineering, Ben-Gurion University, where he is currently the Director of the Center for Power Electronics and Mixed-Signal IC.

Dr. Peretz serves as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS: SPECIAL ISSUE ON LED DRIVES. His research interests include digital and smart control methods for efficient energy processing, SMPS miniaturization, mixed-signal IC design of SMPS, modeling and computer-aided design, applications of nonlinear magnetics, and renewable energy systems.