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Optimal design of a class-E resonant driver

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Abstract: In many applications of class-E converters, custom-made design of the isolation resonant network is impractical; instead, off-shelf products are used. In this case, matching the target output parameters to the converter component stresses requires an additional passive matching network. The design of this network has a tedious optimisation routine and may pose a considerable engineering challenge. This study introduces an optimisation method based on a behavioural modelling for class-E resonant converters, which significantly simplifies the component selection procedure. The method reduces the number of unknowns during simulation assisted parameter optimisation search. Successful implementation of the optimisation process is demonstrated on an off-line, digitally controlled class-E, piezoelectric transformer-based AC/DC converter, where the main inductor and the matching capacitance are the parameters to be optimised.

1 Introduction

Class-E converters are famous for being a simple and effective solution for consumer electronic products, radio-frequency power amplifiers and very high-frequency converters [1]. The advantages of class-E converter such as single low-side switch and soft-switching operation, maintain the popularity of this topology [2–7]. In addition, if isolation is required, it could be introduced by either a magnetic transformer [8, 9] or alternatively by a piezoelectric transformer (PT). PTs are advantageous in some power electronic applications because of their relative small size, high insulation properties and potentially low cost. PT applications include battery chargers [10, 11], drivers for high-side insulated gate bipolar transistor and metal–oxide semiconductor field effect transistors [12], feedback isolation [13], fluorescent lamps [14, 15] and light-emitting diode drivers [16]. Although to integrate a PT into a class-E converter may seem to be simple and cost-effective solution, it is extremely challenging to match the target output to the stress requirements of the converter and the PT. For example, a class-D PT driver [17] and a class-E PT driver [18] are both implemented with no matching network, and investigated using a state-space averaging technique. Several previous studies found in class-E converter analysis literature are based on waveform inspection techniques. These techniques require complex derivations of a set of differential equations [18–23]. For design and optimisation purposes, a numerical simulation approach offers a faster and more cost-effective alternative.

The example being used throughout this paper is an off-line PT-based power supply that applies a class-E converter (Fig. 1). If an application of a custom-made PT [24, 25] is impractical from an economical point of view, one may consider incorporating a matching network [24, 26] to use commercially available PT units. However, the design of the matching network and the redesign of the converter elements may pose a considerable engineering challenge because of the interaction between the converter, matching network and PT.

The objective of this paper is to develop a simulation-assisted optimisation approach that eases the design procedure for isolated class-E resonant drivers. A novel optimising procedure is applied that saves simulation time by reducing the number of unknowns rather than using an exhaustive, multi-parameter, trial and error simulation [27]. By doing so, the resultant optimisation procedure is more engineering-oriented and allows a clear definition of the physical constraints of a system. Without any loss of generality, the method demonstrated in this paper is applicable for other converters where several optimisation variables and constraints exist.

2 Optimisation strategy – reducing the number of unknown variables

The objective of class-E matching network design optimisation procedure is to find the values of two independent parameters L and C_{Div} so that the input voltage to the PT will not exceed the maximum rated voltage, the switch voltage will not exceed a given maximum value and the converter can maintain soft-switching and nominal output power over the expected input voltage range. The optimisation procedure can be simplified if the search is reduced to one parameter rather than the original two independent variables L and C_{Div}. Reduction of the number of variables is accomplished by a simulation model developed in this paper (Fig. 2) where one of the unknowns (C_{Div} in this case) is adjusted automatically and independently during the search. This is realised by applying a model of a voltage controlled variable capacitor similar to the method described in [28], which is adjusted by a closed feedback loop in order to maintain the required output current (Fig. 2). The simulation-ready model includes the class-E stage, a variable capacitor block, a PT model [29], a rectifier, an output filter capacitor and the load. The variable capacitor is controlled by a feedback loop that comprises an error amplifier and a compensator, which limits the bandwidth and assures stability of the loop during simulation as explained in Section 3.2. This feedback loop varies the parameter C_{Div} such that the output power is at the desired level. The optimisation is done under the assumption that the system (Fig. 1) is frequency controlled while the duty ratio is fixed at every operating point [30]. Since only one parameter is varied, the overall control of the system is simplified. The main drawback of a variable-frequency control is the potential loss of soft-switching. However, since a matching network exists, zero voltage switching (ZVS) can be assured for a wide operation range while the frequency is adjusted to obtain a regulated output. In addition, the downside of a fixed duty ratio is that the

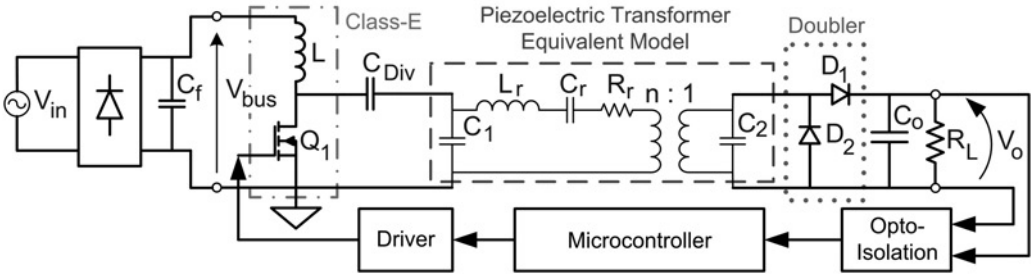

Fig. 1 *Class-E converter with PT represented by its equivalent model*

maximum switch voltage is a function of the bus voltage. The concept outlined below can be adopted to optimise the elements' values for both frequency and duty cycle control.

3 Modelling and control of a simulation compatible variable capacitor

3.1 Simulation compatible variable capacitor model

A variable capacitor is required for the design procedure described in this paper. Unfortunately, this element is generally absent from the majority of simulation software packages. To overcome this, a generic and straightforward variable inductor implementation method, as described in [28], is reevaluated and adjusted here to implement a variable capacitor.

The basic concept of the proposed variable capacitor model is to reflect the behaviour of a linear capacitor through a non-linear 'transformer'. As suggested in [28], a non-linear transformer is implemented using two dependent sources: a voltage-dependent voltage source referred to as E1 and a voltage-dependent current source referred to as G1. Fig. 3 presents the implementation of the variable capacitor by reflection via a non-linear 'transformer' in OrCAD PSpice. The sources E1 and G1 are defined by

$$\begin{aligned} E1 &= \frac{V_{\text{sec}}}{K} = V_{\text{pr}} \\ G1 &= I_{\text{pr}} = I_{\text{sec}} \end{aligned} \tag{1}$$

where K is the gain coefficient and V_{sec} and I_{sec} are the voltage and current at the transformer's secondary side, respectively. Although V_{pr} and I_{pr} are the voltage and current at the primary side of the transformer, respectively. The impedance, X_{C_1}, of the original constant value capacitance $C1$ equals the ratio between its voltage and its current. Although taking into account the transformer behaviour as described in (1), the impedance reflected to the primary side, $X_C{}'$, results in

$$X_C^{'} = \frac{V_{\text{pr}}}{I_{\text{pr}}} = \frac{(V_{\text{sec}}/K)}{I_{\text{sec}}} = \frac{1}{K} \cdot X_{C1} \tag{2}$$

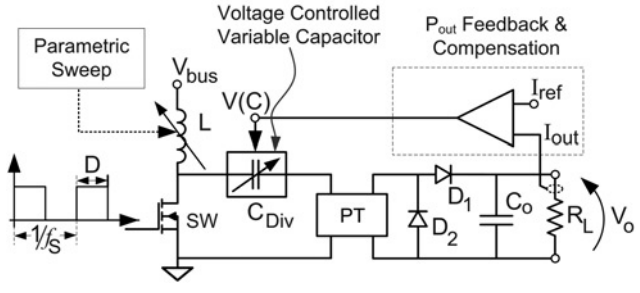

Fig. 2 *Simulation scheme used to lower the number of unknowns from two to one*

Consequently, the capacitance C' reflected to the primary side has the adjustment parameter K and equals

$$C' = K \cdot C1 \tag{3}$$

If K is made dependent on some voltage in the circuit (the output $V(C)$ of a compensator in this case), the setup will dictate reflected capacitance to the primary side of the transformer, and in the case of the model in Fig. 3, it will also emulate a voltage-dependent variable capacitor between the nodes 'cap1' and 'cap2'. The resistor R_{conv} (Fig. 3) is added to avoid convergence problems in the numerical simulation.

3.2 Automatic control of variable capacitor

The automatic search for the value C_{Div} in order to keep the output current constant is accomplished by a closed-loop setup as illustrated in Fig. 4. The controlled variable is the output current, S_{O}, which is compared with the reference value, S_{ref}. The resultant error signal, S_{e}, is fed into a compensator which produces a control command signal S_{C}. The role of the compensator is to allow the output current to converge into the desired value governed by the reference value. The compensation signal, S_{C}, is fed into a block named 'Variable Capacitor'. This block is a linear unit translator from S_{C} to C. S_{C} may be in volts or a unit-less variable and C represents Farads (coded into voltage for simulation purposes). Finally, the power stage comprises three inputs: constant duty cycle D; inductance value L, which is a sweep variable as will be explained in Section 4.2; and the capacitance C that is automatically adjusted by the feedback loop.

It should be noted that in order to regulate the output power at its nominal value, the required control variable is the output power. However, because of the resistive load configuration (Fig. 1), output power control can be obtained by regulation of the output current.

4 PT driver optimisation

4.1 Selecting the initial values

The system's operating frequency range is positioned to the left of the natural PT resonance frequency. The initial maximum

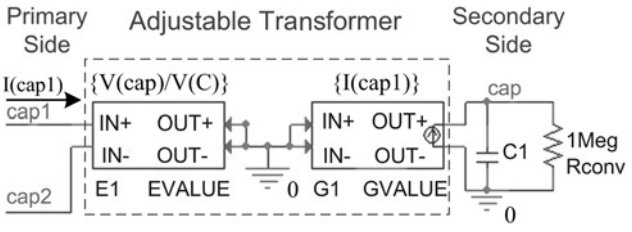

Fig. 3 *Variable capacitor implementation in OrCAD PSpice*

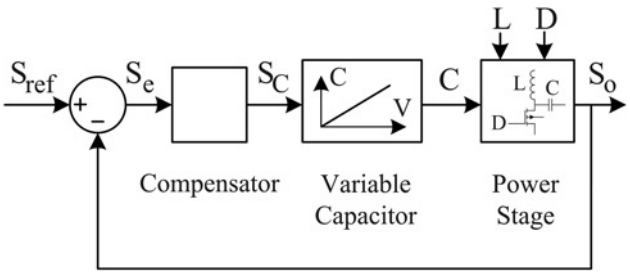

Fig. 4 *Automatic capacitance adjustment control diagram*

switching frequency is set according to the transfer function of the bare PT. To avoid operation at resonant frequency, the maximum frequency is selected to be at a transfer ratio point which is 5–10% lower than the peak transfer ratio. The initial duty cycle is set to 50%. Since C_{Div} and the input capacitance of PT form a capacitive voltage divider, the simulation-based search boundaries were chosen to be a decade above and decade below the PT input capacitance value. The inductance is a sweep parameter in the simulation. The inductance sweep range is set to be around the value that will resonate with C_{Div} at the PT resonant frequency. Transient simulation run time is set such that the value of the variable capacitor is allowed to converge and stabilise.

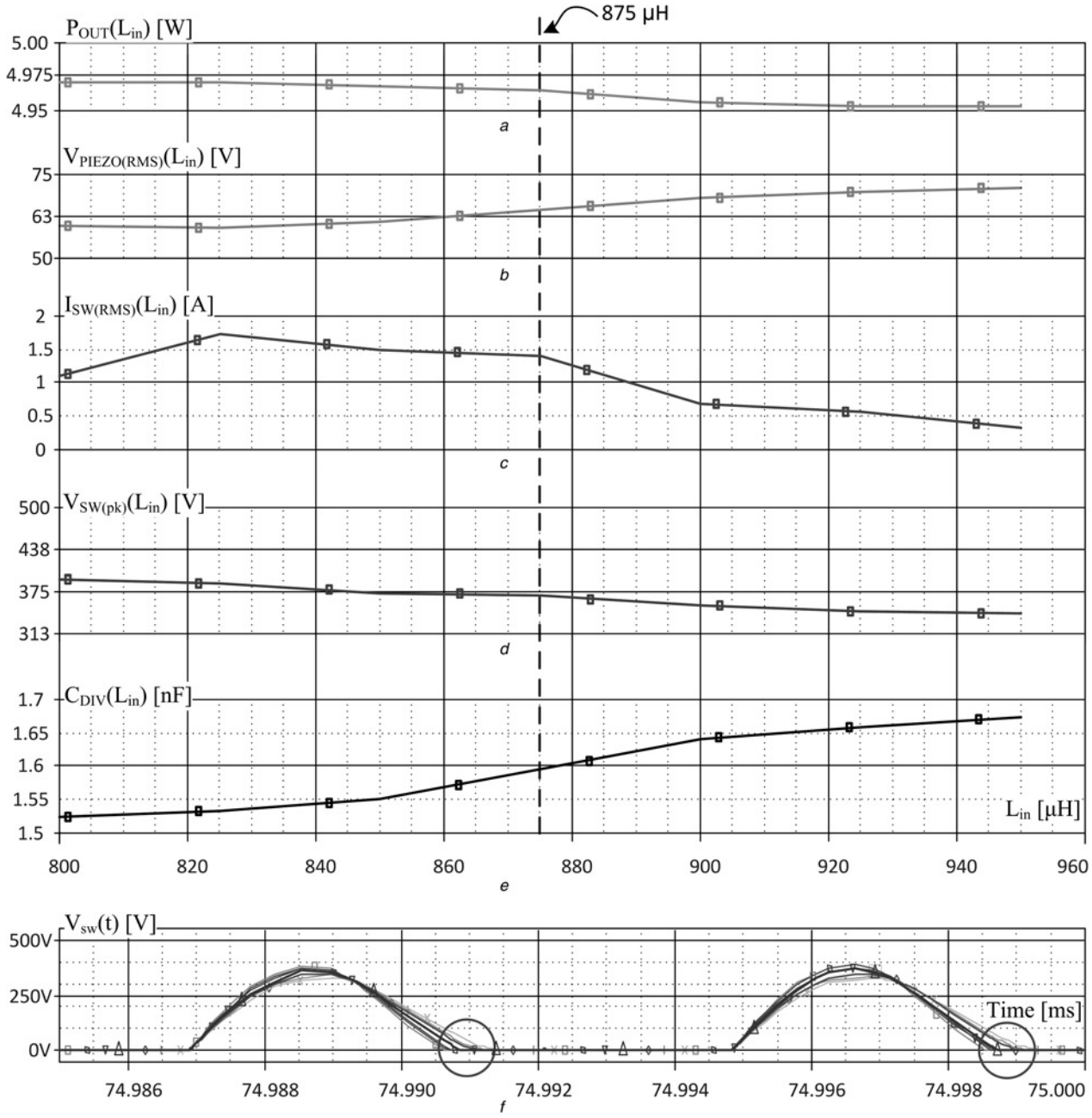

Fig. 5 *Simulation results of driver optimisation procedure. Performance analysis (x-axis is an inductor value)*

a Output power
b Maximum RMS voltage at the piezo input terminals
c Maximum RMS current through the switch
d Maximum voltage stress across the switch
e Capacitance value of C_{Div}, as converged by the automatic capacitor search feedback loop
f Time waveform: voltage across the switch (multiple traces obtained from parametric sweep simulation (inductance as the sweep variable), bold trace is the system performance with 875 µH inductor)

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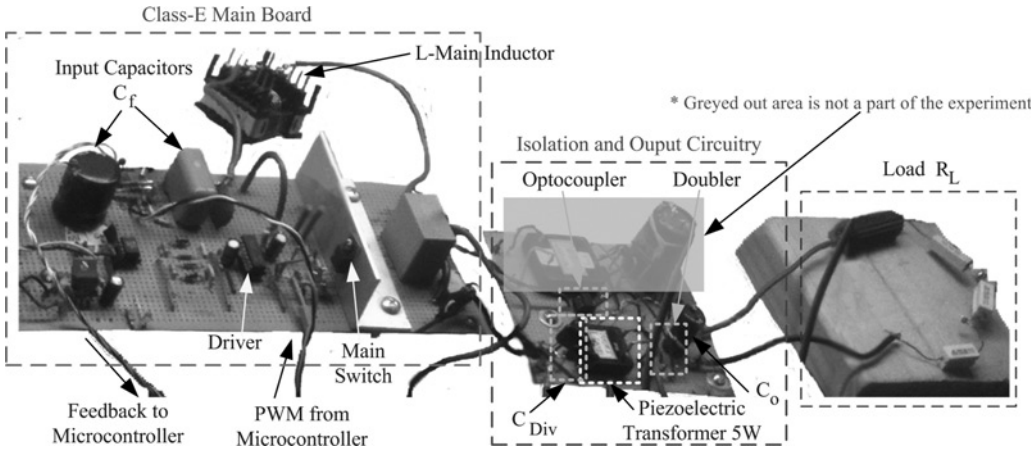

Fig. 6 *Experimental prototype*

4.2 Simulation procedure

The simulation begins by testing the 'worst case' boundary. This is done by setting the input voltage to the minimum and the switching frequency to the maximum values. Transient simulations are run in parametric mode, sweeping the inductor's value. Performance analysis option (in PSpice) is used to examine the maximum voltages across the switch, ZVS condition and the maximum voltage on the PT. Since the chosen control is based on a fixed duty cycle, the maximum voltage across the switch is approximately proportional to the input voltage. Therefore the observed maximum voltage on the switch, for simulations with low input voltage, should not exceed the value of the specified maximum switch voltage divided by the ratio of maximum to minimum input voltages

$$V_{\mathrm{sw(max)}}^{\mathrm{Low}} = V_{\mathrm{sw(max)}}^{\mathrm{High}} \cdot \frac{V_{\mathrm{bus}}^{\mathrm{Low}}}{V_{\mathrm{bus}}^{\mathrm{High}}} \tag{4}$$

The upper script defines lower/higher live voltage limits and the subscript defines the measurement point, either 'bus': the bus voltage or sw(max): the maximum voltage across the switch. If there are no points fulfilling these conditions, the 'ON' time of the switch is reduced, and the simulation is run again. This procedure is repeated until an inductor–capacitor pair and the 'ON' time satisfy the requirements for ZVS, maximum voltage across the switch, maximum PT voltage and nominal output power.

Following the initial stage outlined above, a simulation of the transfer ratio of the system as a function of the switching frequency is carried out. It should be noted that the system's response and peak location could be significantly different from that of the bare PT. Even so, the maximum operating frequency should always be chosen around the peak response of the PT to ensure high efficiency [29]. The more accurate transfer function can then be used to reselect the maximum switching frequency. Typical simulation results are shown in Fig. 5.

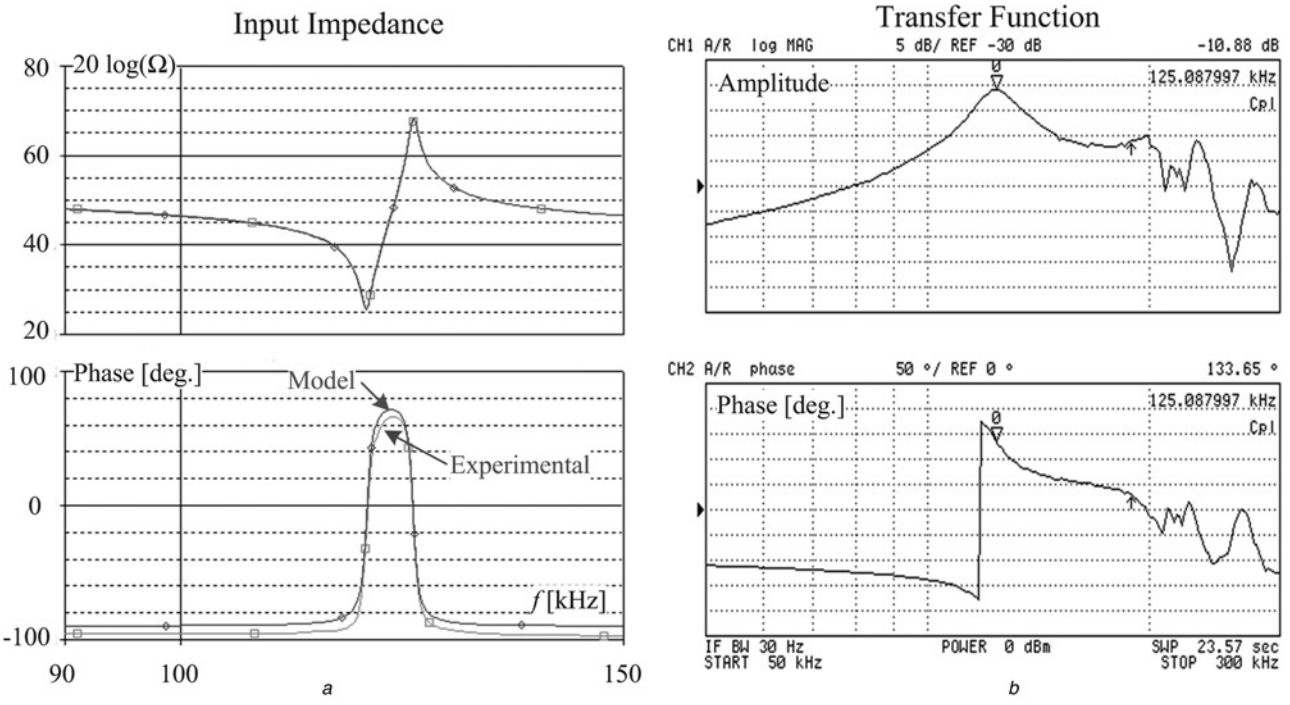

Fig. 7 *Experimental results – response of the bare PT element*

a Input impedance of bare PT element
b Transfer function of the bare PT element

5 Simulation and experiment

The proposed computer-aided design and optimisation method was tested on a laboratory prototype depicted in Fig. 6, which follow the schematics presented in Fig. 1. The approximate parameters of the PT (PTA005010, Konghong Co. Ltd., China) equivalent circuit model were determined by the method described in [31], and found to be: $L_r = 2.544$ mH, $C_r = 792$ pF, $R_r = 31\ \Omega$, $C_1 = 3.6$ nF, $C_2 = 75$ nF and $n = 5.6$. The response of both the bare PT element and the derived model is demonstrated in Fig. 7. Fig. 7*a* is the input impedance. Please note that the predicted amplitude from the model lies practically on top of the experimental result. The small phase lag from the experimental result is because of the delay of the excitation amplifier. Fig. 7*b* is the transfer function of the PT while it was loaded on the secondary side with an approximate nominal load of 100 Ω, as measured by HP 4395A Network Analyser.

The output circuit components consisted of: a C_O of 470 µF, a nominal load R_L of 80 Ω and two Schottky diodes (MBR340) D_1 and D_2. The input rectification stage and filter capacitor C_f were designed to supply V_{bus} with a maximum ripple of 5 $V_{p\text{-}p}$ under the nominal load. The main switch (IRFIB6N60A) had an $R_{ds\text{-}on}$ equalling 0.75 Ω. Output voltage was controlled to be 20 V and the nominal output power was 5 W.

The circuit optimisation procedure was implemented to comply with the requirements of the system, as summarised in Table 1, and the results are presented in Fig. 5. As observed, the compensation network adjusts the variable capacitor so that the output power is close to the targeted 5 W throughout the simulation range (Fig. 5*a*). The second optimisation constraint is the maximum allowable root-mean-square (RMS) PT input voltage. According to the system requirements found in Table 1, it needs to be below 65 V, that is, the maximum inductance is below 880 µH (Fig. 5*b*). Figs. 5*c* and *d* show the expected RMS current through the switch and the peak voltage across the switch. Both are evaluated with respect to the system requirements. The maximum allowable voltage is 600 V, but this voltage will appear at the higher end of the input voltages range. At the lower end, the limit according to (4) was calculated to be 353 V. According to Fig. 5*d*, the inductance required to satisfy the performance goals should be larger than 870 µH.

Given the set of constraints outlined above, the optimal value of the inductor was found to be $L = 875$ µH. The inductance selection is highlighted with a bold dashed vertical line in Fig. 5. The paired capacitance extracted from Fig. 5*e* is $C_{Div} = 1.6$ nF. ZVS can be evaluated from the time-domain switch waveform of Fig. 5*f*. The correct trace for the selected inductor is highlighted in bold (Fig. 5*f*), and the relevant ZVS evaluation area is marked with bold circles. The duty cycle required to assure proper operation over the input line voltage range was evaluated to be about 35%. The final operation range was found to be 126 kHz for $V_{bus} = 110$ V and 120 kHz for $V_{bus} = 187$ V. The control task was implemented by TI's ultra-low power microcontroller MSP430F2013.

Fig. 8 presents experimental waveforms of the laboratory prototype and the capability of the system to comply with the full input voltage range as expected from a 110 V grid. There are three results, ranging from lowest grid voltage limit of 80 V_{rms} to the highest grid voltage limit of 132 V_{rms}. The intermediate voltage is represented by the nominal grid voltage of 110 V_{rms}. Fig. 8*a* illustrates the operation under the lowest input voltage and highest switching frequency conditions. ZVS can be observed, and the maximum voltage across the switch is about 350 V as calculated above. The operation at nominal conditions is shown in Fig. 8*b*, where again ZVS could be confirmed. Operation under the highest voltage stress is depicted in Fig. 8*c*. In this case, the line voltage is

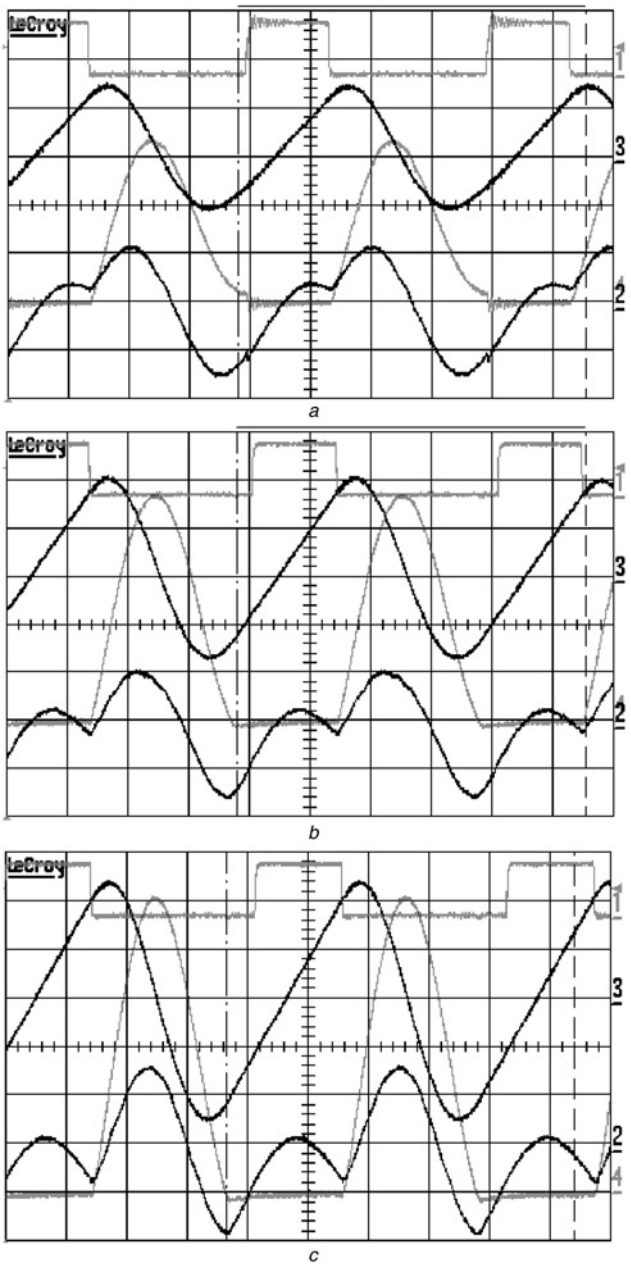

Fig. 8 *Experimental results; bus voltage condition*

a Lowest
b Nominal
c Highest; time 2 µS/Div; traces (from bottom to top): (channel 2; black) PT input voltage 50 V/Div; (channel 4; grey) switch voltage – V_{sw} 100 V/Div; (channel 3; black) I_L 0.2 A/Div; (channel 1; grey) switch gate signal

Table 1 Design example: system requirements

V_{in}, V_{rms}	V_{bus}, V	V_o, V	P_o nominal, W	V_{sw} (max), V	f_s, kHz	V_{PT} (max), V_{rms}
80–132	110–187	20	5	600	100–150	65

RMS voltage value relates to the first harmonic of PT input voltage waveform.

Table 2 Experimental results: efficiency

Parameter	Utility voltage limit		
	Lowest voltage	Nominal voltage	Highest voltage
switching frequency, kHz	126	123	120
standalone PT efficiency, %	85	84	80
class-E converter efficiency, %	91	82	79
overall system efficiency, %	77	69	63

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situated at its allowed maximum value and the switching frequency is reduced to the lower limit. The maximum switch voltage is around the allowed limit that was specified, and ZVS is still maintained. Class-E converter, standalone PT and overall system efficiencies for the three cases of lowest, nominal and highest input voltages are summarised in Table 2.

6 Discussion and conclusions

A computer-aided design of an off-line, class-E PT driver was implemented by applying a new simulation approach. The proposed advanced simulation procedure simplifies the search of unknown parameters by reducing the number of unknowns from two to one. This is accomplished by an auxiliary feedback loop used during the simulation, which adjusts the value of one of the unknowns (a capacitor in the illustrated case) to maintain the desired output power. A step-by-step simulation procedure is then used to determine the optimal value of the unknown parameter (the value of an inductance in the present case) so that the design objectives are met. The converter prototype which was designed using the proposed method was found to comply with the requirements of ZVS operation and delivery of nominal power while still maintaining safe switch and PT voltage over a grid range of 80 to 132 V_{rms}. It should be noted that operation of a class-E converter over a wide input voltage range will create higher-RMS currents at higher input voltages. This consequently will lower overall system efficiency, but efficiency optimisation is a separate issue, which is not covered in this paper. Even though, demonstrated on the special case of a class-E PT driver design, the proposed method of variable elimination could be useful in other designs based on simulation.

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