Resonant Switched-Capacitor Voltage Regulator With Ideal Transient Response

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***Abstract*—A new, small and efficient voltage regulator, realized using a resonant switched-capacitor converter technology, is introduced. Voltage regulation is implemented by means of simple digital pulse density modulation. It displays an ideal transient response with a zero-order nature to all disturbance types. The newly developed topology acts as a gyrator with a wide range of voltage conversion ratios (below as well as above unity) with constant efficiency characteristics for the entire operation range. The operation of the voltage regulator is verified on a 20 W experimental prototype, demonstrating ideal transient recovery without over/undershoots in response to load and line transients. Simple design guidelines for the voltage regulation system are provided and verified by experiments.**

***Index Terms*—Digital control, ideal transient recovery, pulse density modulation (PDM), switched-capacitor converters (SCCs), switch-mode power supplies, voltage regulation.**

I. Introduction

FOLLOWING the recent proliferation of portable electronics, there has been a sharp increase in interest and demand for more compact, light, energy efficient and economical power sources [1]. As this trend continues, the requirements become more and more challenging. Tighter output voltage regulation, faster response times to load and input voltage changes and lower volume are of major concern in the design of present-day switch-mode power supplies and pose a bottleneck in the advancement current technology.

State-of-the-art voltage regulators apply switched-inductor converters (SICs) combined with advanced nonlinear controllers [2]–[9] to minimize size and maximize the power processing efficiency. The main limiting factor of this general concept is the presence of a relatively large inductor that prohibits, to a large extent, miniaturization and power on-chip integration. Resonant-mode converters [10]–[15] allow volume reduction of the magnetic element by allowing higher frequency operation and lower energy storage requirements. Thanks to the soft-switching capabilities, the overall power conversion efficiency is not compromised due to the higher operating frequency [12], [13]. Another attractive feature that can be achieved by resonant converters has been demonstrated in [15] and [16] which is the capability of facilitating very high rejection ratio to variations in the line or load.

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Present-day switched-capacitor technology has become an attractive alternative for volume-sensitive applications, featuring high efficiency and economical implementation [17], [18]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited. These limitations stem primarily from the fact that the efficiency of switched-capacitor converters (SCCs) depends linearly on the voltage gain [19]–[22].

A recently developed gyrator mode resonant switched-capacitor converter (GRSCC) presented in [23] and [24] has demonstrated a unique potential for efficient voltage regulation over a wide range of conversion ratios and power levels, and can be used as the main building block of a voltage regulator.

The objective of this study is to explore and demonstrate the operation of a small and efficient voltage regulator that is realized by the GRSCC and a simple pulse density modulation (PDM) control scheme (see Fig. 1). The new voltage regulator exhibits an ideal response to load and line transients, i.e., with zero over/undershoot over the full operation range, as well as a constant efficiency profile over a wide range of voltage gain and power levels.

The main quality of the new GRSCC presented in Fig. 1 is that it disengages the efficiency of the system from the voltage gain. This is achieved by introducing an additional switching phase to balance any charge mismatch between the input and the output and, as a result, a conventional SCC topology is transformed into a voltage-dependent current source, i.e., a gyrator converter. Output voltage control is enabled by a comparator-based PDM, where the charge transfer rate to the output is controlled such that a desired voltage level is maintained. The new voltage regulator combines the virtues of both worlds: wide operation range with high efficiency at high frequencies (from resonant SICs) alongside reduced volume and potential chip-integration (from SCC).

II. RSCC Principle of Operation

The new gyrator converter presented in [25] has evolved from the conventional soft-switched resonant SCC configuration [26]–[28]. As in the classical design, it includes two switches and a resonant tank. Additionally, a switch, Q_3, is added to introduce an alternative resonant path of the current to balance the residual charge of the flying capacitor, i.e., restores the flying capacitor voltage to its original state by reversing its polarity. The mechanism of polarity reversal (charge balancing) lays the foundations to break the rigid connection of input/output voltage and efficiency dependence. Controlling the sequence of the switches governs the power flow direction, hence bidirectional step-up/down operation.

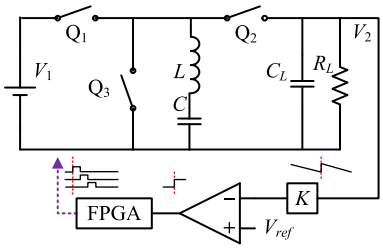

Fig. 1. Proposed voltage regulator. A new gyrator resonant SCC and feedback loop.

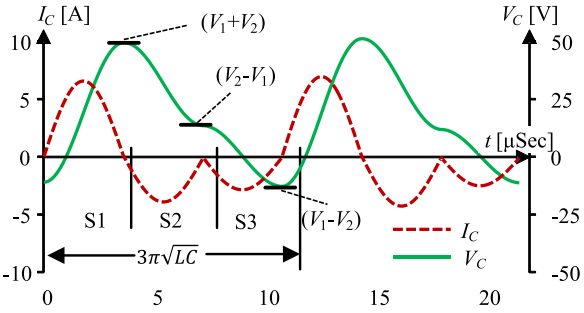

Fig. 2. Typical waveforms (obtained from simulation) of the flying capacitor voltage and current. Circuit parameters are as follows: $V_1 = 20$ V, $V_2 = 31$ V, total series resistance $R_s = 0.15\ \Omega$, $L = 5.2\ \mu$H, and $C = 0.25\ \mu$F.

The operation of the converter shown in Fig. 1 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 2 that illustrates the capacitor voltage V_C and the resonant tank current I_C for the case of a nonunity step-up conversion. By turning Q_1 ON, a charge state (S1) is commenced, which resonantly charges the flying capacitor from the input V_1. At zero current, Q_1 is turned OFF and Q_2 is turned ON (state S2). At this point, the flying capacitor resonantly discharges onto the output capacitor. Since the input voltage, V_1, and the output voltage, V_2, are of different values, only a portion of the charge is delivered to the output which results in V_C that is different from its voltage at the starting point of S1. The amount of this voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning Q_3 on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.

The order of the sequence governs the power flow direction, i.e., from V_1 to V_2 or from V_2 to V_1. To deliver power from V_1 to V_2, the sequence will be (S1, S2, S3). That is, *charge* from V_1, *discharge* on V_2 and *reverse* the flying capacitor polarity. In the case of power to be delivered from V_2 to V_1, the sequence will be changed to (S1, S3, S2). The duration of each switching state is half the resonant period and hence the switches operate at zero-current switching (ZCS).

A. Gyration Ratio and Power Conversion Efficiency

Voltage regulation is obtained by introducing a time-delay between consecutive sequences, i.e., PDM [29]–[32]. Assuming identical resonant characteristics for all states, that is, a 1/3 of the operation cycle for each state, the average input and output currents (I_1, I_2) can be obtained and a gyrator relationship between the currents (I_1, I_2) and voltages (V_1, V_2) is formed as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \begin{cases} g = \frac{F_{\max}}{F} \frac{2}{3\pi Z} \\ Z = \sqrt{\frac{L}{C}} \end{cases} \quad (1)$$

where F is the operating frequency of the switching sequence, including the added delay. The maximum output current is obtained for zero time-delay between cycles. In this case, the converter operates at the maximum frequency $F_{\max}$ of three half-resonant cycles, that is

$$F_{\max} = (3\pi\sqrt{LC})^{-1}. \quad (2)$$

The relationship between the output current I_2 and the input voltage V_1 can be simplified and is given by

$$I_2 = 2V_1FC. \quad (3)$$

For given resonant parameters L and C, the power conversion efficiency η can be written as a function of the total series resistance R_s (seen in each state) and the overall voltage gain A [25]

$$\eta = \left(1 + \frac{\pi}{2}\frac{R_s}{Z}(A + A^{-1} - 1)\right)^{-1}, \quad A = \frac{V_2}{V_1}. \quad (4)$$

In the case of topology derivatives such as a voltage divider/multiplier [25], (4) would be modified using the normalized gain, $\tilde{A}$, instead of A, according to the base voltage gain, A_n

$$\tilde{A} = A/A_n. \quad (5)$$

For a natural multiplier, $A_n = 2$, while for a divider $A_n = 0.5$.

III. Voltage Regulation

To facilitate a dc output, an output capacitor C_L is added such that the average of the current is passed to the load (neglecting ripple). For a resistive load R_L, the output voltage can be expressed as follows:

$$V_2 = I_2R_L = 2R_LV_1FC. \quad (6)$$

If F is made controllable, the system is able to react and compensate for any changes in the input voltage, reference voltage or the load resistance such that the average output voltage is obtained without over/undershoot. This is due to the discontinuous-conduction mode (DCM)-like operation of the converter which naturally maintains per-cycle charge balance between the input and the output [30], which in the GRSCC case is facilitated with the addition of the third switching phase.

A more illustrative description to the voltage regulation concept using the GRSCC is shown in Fig. 3 and is assisted by the waveforms of Fig. 4. As described earlier in the previous section and can be observed from Fig. 2, the GRSCC operation is pulsed in its nature. Consequently, as a pulsed current source, I_g can be used to model its output characteristics. The current source, I_L, is used to model the current loading state. Voltage

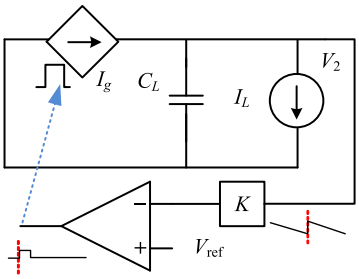

Fig. 3. Illustrative model of the GRSCC-based regulator. The GRSCC is modeled as an ideal pulsed current source I_g.

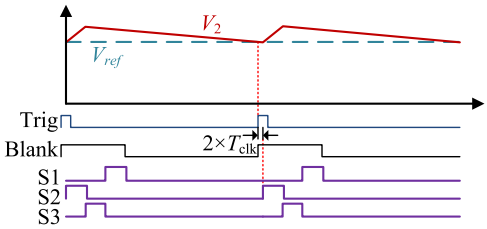

Fig. 4. Waveform relations between comparator inputs and the state signals for the proposed voltage regulator from Fig. 1. "Trig" is the signal received from the external comparator; "Blank" is an internal blanking signal to avoid overlapping if subsequent pulses are needed.

regulation is facilitated by triggering I_g to output a current pulse whenever the output voltage reaches the threshold level V_{ref}.

For a given load current I_L and assuming that no current is injected from the source, the voltage across C_L drops virtually linearly (by first-order approximation). Once the output voltage reaches V_{ref}, a comparator event triggers the pulsed current source, restores the charge on C_L, and resumes on the steady-state. This mechanism is maintained as long as the pulsed source contains sufficient energy to recover the voltage upon C_L. Compensation for changes in the loading current is inherent due to differences in the discharge gradient of C_L, which vary the pulse rate of I_g.

The PDM operation of the GRSCC, triggered by the comparator event, creates a switching sequence of (S2, S3, S1) and is then followed by a time-delay until the next comparator trigger. The order of the switching sequence is arranged such that after the time-delay, which allows the output voltage to drop down to V_{ref}, the discharge state (S2) is initiated first charge the output capacitor back to $V_{\text{ref}} + \Delta V_2/2$, preventing further voltage drop. Then, the other two states (S3, S1) are commenced to "*arm*" the flying capacitor, having the converter ready for a new cycle. As mentioned earlier, the rate F in which the switching sequence is activated depends on the slope and the amplitude of the voltage ripple, that is, on the load current and C_L.

The deviation of the instantaneous output voltage from the desired value is within the margins of the peak-to-peak output voltage ripple [25], ΔV_2, which depends on the operating conditions and inversely proportional to C_L as follows:

$$\Delta V_2 = 2V_1 \frac{C}{C_L}\left(1 - \frac{F}{3F_{\max}}\right). \tag{7}$$

In case that the output capacitor includes a significant series resistance, R_{CL}, the magnitude of the output voltage ripple can

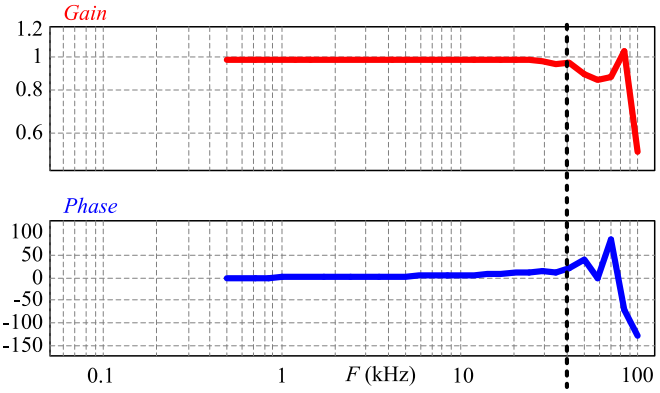

Fig. 5. Control-to-output frequency response. Top: output magnitude normalized to theoretical (ideal) output. Bottom: phase (degrees). The vertical line marks $f_s/2 = 35$ kHz.

be approximated to (assuming in-phase effect of *RCL* [33]

$$\Delta V_2 = 2V_1 \frac{C}{C_L}\left(1 - \frac{F}{3F_{\max}}\right) + R_{CL}\frac{V_1}{Z}. \tag{8}$$

The reference value is set to the lowest allowed voltage, taking into account the voltage ripple by

$$V_{\text{ref}} = V_2 - \Delta V_2/2. \tag{9}$$

Following the PDM method described here, the average output voltage is constant, within the ripple margins, and is independent of R_L and V_{in}. As can be observed from (7), the voltage ripple primarily depends on V_1, while changes in the load (which vary F) are up to 17% of the ripple value. In most cases, this deviation is negligibly small, and $\Delta V_{2,p-p}$ in (9) can be approximated to an averaged ripple amplitude. Since the average output voltage is maintained at all times, i.e., no transient time, the voltage regulator can be considered to constantly operate at steady-state, and the efficiency estimated in (4) is applicable. Furthermore, no-load protection is inherent since no triggering will occur.

Soft start in this realization is inherent; upon startup the voltage on C_L is zero (i.e., $V_2 < V_{\text{ref}}$) and the controller operates at $F_{\max}$ to increase V_2. C_L then charges in constant current until the desired voltage is obtained. To further limit inrush currents, V_{ref} can be made to slope up slowly. Due to the GRSCC's current sourcing nature, overload or short-circuit conditions would not damage the converter; however, voltage regulation is not guaranteed beyond the maximal output rate of $F_{\max}$.

IV. Validation of the Zero-Order Response

To verify the control-to-output zero-order response feature of the GRSCC, a frequency response simulation has been constructed in PSIM (Powersim, Inc.). The triggering algorithm has been implemented by a C-block generating a frequency-modulated (FM) control command with carrier frequency of 90 kHz and modulating signal (magnitude) of 20 kHz. Then, the rate of the modulating signal has been swept while measuring the ratio between the output current and the magnitude of the modulating signal. Fig. 5 shows the resultant frequency response; it can be observed that the control-to-output response is

virtually constant in magnitude with zero phase-lag over the entire operation range, i.e., up to half of the frequency of the lower sideband of the control command. This implies that the converter is capable of accommodating load transients with zero-order response up to the rate of $F_{\max}/2$.

V. Design Considerations

A. Resonant Network

The design procedure of a voltage regulator based on the GRSCC topology is described through an example of a 20 W step-down inverting voltage regulator with the target values of $V_o = 5$ V, $V_{\text{in}} = 8$–15 V, and $F_{\max} < 500$ kHz.

First, the values of *L* and *C* are derived by combining (2) and (3) and taking into account the worst case of $F_{\max}$, $V_{1,\min}$, and $I_{2,\max}$ as follows:

$$C = \frac{I_{o,\max}}{2V_{1,\min}F_{\max}}$$
$$L = [(3\pi F_{\max})^2 C]^{-1}. \tag{10}$$

The second step is to estimate the values of the rms current that circulates in the resonant tank. This is done for the selection of the switches as well as to determine the physical sizes of *L* and *C*. Considering (4) and after some manipulations, the rms current can be expressed as follows:

$$I_{\text{rms}} = \sqrt{V_2 I_2 \frac{\pi}{2Z}(A + A^{-1} - 1)}. \tag{11}$$

Finally, given a desired target voltage and defining the allowed voltage deviation, the output capacitor value and the reference voltage are calculated using (7) and (9), respectively.

Given the previous parameters, the inductance and capacitance are calculated by (10) to be $L = 0.1$ μH and $C = 0.56$ μF. These were chosen such that 20 W of power can be processed from the input range specified. Given a typical loop resistances of $R_S = 20$ mΩ, the expected efficiency is in the range of 85–92%. Similarly to switched-inductor PDM converters, the rms currents are relatively higher than conventional converters that operate in continuous conduction mode (CCM). As opposed to other PDM converters, no additional losses are present thanks to the resonant current and the resultant soft-switching operation. In this particular design, the rms current is estimated to be 12 A at maximum effort. The main problem with higher rms currents is the stress on the flying capacitor. This can be overcome by paralleling capacitors of smaller values.

The inductor, although having a small inductance value, has to sustain relatively high rms currents. However, in contrary to the magnetics design in SICs, the per-cycle energy that is stored in the inductor is zero. As a result, the main factor of the inductor sizing stems from the core losses, rather than saturation limits. A convenient way to estimate the volume of the magnetic element is by the area product A_p, which can be expressed as [34]

$$A_p = \frac{L\Delta I I_{\text{rms}}}{JK\Delta B} \tag{12}$$

where *L* is the desired inductance, ΔI is the maximum current variation through the inductor, ΔB is the maximum flux density variation due to ΔI, *J* is the current density that is allowed through the winding, and *K* is the fill factor.

TABLE I
Comparison of the Area Product A_p Between Various Converters Designed for Voltage Regulation

	Buck–boost		Buck	GRSCC	
	CCM	*BCM*[a]	*BCM*[a]	*Ferrite*	*Air*
$\tilde{A}_p$[b]	50	12	7	37	1
$\hat{B}$[T]	0.2	0.2	0.2	0.05	2
L [μH]	7	0.7	1.7	0.1	0.1

a. Boundary current mode.
b. Normalized to GRSCC with air core.

For the particular case of the GRSCC, after some manipulations, (11) can be rewritten as follows:

$$A_p = \frac{\max(V_1, V_2) I_{\text{rms}}}{3\pi JK\hat{B}F_{\max}} \tag{13}$$

where $\hat{B}$ is the allowed peak flux density. Using a ferrite core, the area product of the inductor needed for the GRSCC described in the example earlier is relatively large, comparable with an inductor for a buck–boost converter, designed according to the same specifications, operating in CCM. However, since the inductance value that is required for the GRSCC is quite low (0.1 μH), a ferrite-less (i.e. air core) construction is feasible. Consequently, higher $\hat{B}$ is allowed, resulting in a significantly smaller A_p. A normalized comparison between the required area products for various voltage regulator topologies and operation modes has been carried out and is summarized in Table I. A significant reduction of the inductor volume can be noticed for a GRSCC-based voltage regulator by one-order of magnitude, when compared to a buck of the same features.

The presented GRSCC regulator shares the same switch-count of other step-up/down realizations such as a noninverting buck–boost with comparable efficiency [23]. Nevertheless, specific comparison to step-down regulators implemented with SICs [35]–[40] demonstrates that although having more switches, the overall power density of the GRSCC is reduced considerably. This is accomplished by a coreless magnetic element and output filter that is sized to the voltage ripple requirements alone.

B. Output Filter and Output Voltage Measurement

Similar to other ripple-based voltage regulators, different types of output capacitors may affect the performance and the stability of the system [41]–[43]. This is a result of a more complex output impedance behavior than a single left-half-plane pole. Potential remedies to this problem have been widely covered in [41] by introducing a firm stability criterion to the structure of the output filter with respect to the on-time duration. In this study, the output filter design is limited to capacitors of the same type and the selection of the output capacitance value is obtained by the target ripple value employing (8).

Another issue that needs to be resolved is the selection of the target output voltage ripple that will satisfy both the load

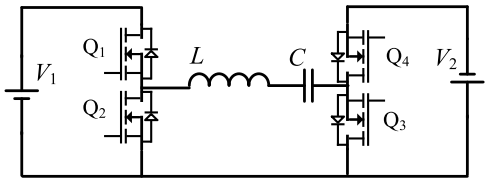

Fig. 6. Experimental inverting scheme, using four MOSFETs.

TABLE II
EXPERIMENTAL SPECIFICATIONS

Parameter	*Value*	*Model*
C	$10 \times 0.1\ \mu$F	C4532C0G2A104J320KA
L	0.18 μH	Air-winding
Q_1, Q_3	PMOS	IXTP96P085T
Q_2, Q_4	NMOS	IXTP160N10T
C_L	$5 \times 10\ \mu$F	C5750X7SR1H106K
Drivers		MIC4427YN
R_S	48 mΩ	
$F_{\max}$	~250 kHz	
Dead time	100 ns	
V_1	8–15 V	
V_2	5 V	
Rated power	20 W	

requirements and at the same time allow reliable measurement. A comparator-based measurement is inherently sensitive to noise, in particular due to the output capacitor's ESR in the presence of pulsating output current. From the comparator point of view, sufficiently high SNR is satisfied if the lower value of the target ripple exceeds the error measurement value of the comparator. A second measure of noise reduction can be obtained either by passive means using filter capacitors [36], [41], or by digital means employing a blanking period. The latter has been adopted in this study, which in addition to enforcing the $F_{\max}$ limit, accounts for the stability considerations presented in [43] and [44].

VI. EXPERIMENTAL RESULTS

To verify the operation of the converter as a voltage regulator and to demonstrate the ideal transient features of the system, a 20 W experimental prototype was realized using an inverting bridge configuration (see Fig. 6). The target parameters and the list of components used are summarized in Table II. A digital PDM controller was implemented on a field-programmable gate array (Altera Cyclone IV). The ZCS operation of the gyrator RSCC is sensitive to input voltage variations, but since the input range is moderate, satisfactory results were achieved by precalibration.

The controller was programmed to execute a pulse sequence for the drivers whenever a trigger from a comparator was sensed for two subsequent clock-cycles or more, as illustrated in Fig. 4. An internal blanking signal was added to dictate $F_{\max}$ and prevent overlapping between sequences during startup or overloads.

Fig. 7 shows the current and voltage waveforms upon the flying capacitor C, matching the theoretical waveforms from Fig. 2 as well as validating the operation under ZCS is. The

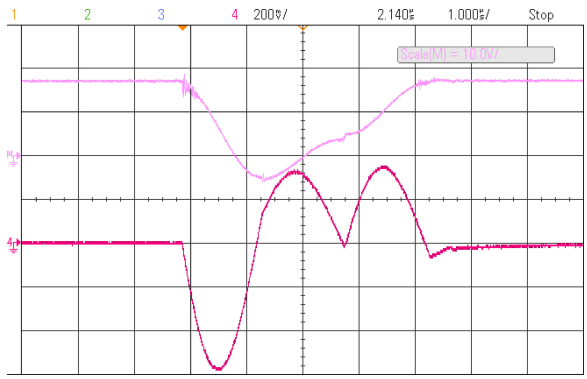

Fig. 7. Experimental waveforms of a discharge-invert-charge sequence, showing V_C (top, 10 V/div) and I_C (bottom, 9 A/div).

residual lagging current that follows the discharge phase is due to the discharge of drain–source capacitances. Fig. 8 demonstrates the ideal load transient response of the voltage regulator for both light-to-heavy and heavy-to-light modes for zero to nominal current (4 A) load transients and for 1–3.5 A.

The current waveforms in Fig. 8(b) and (c) include some parasitic effects of the experimental load stepping setup; a load resistance with stray inductance was switched in and out using an open-drain sink. The turn-on Fig. 8(b) rise-time matches well with the load inductive time-constant value, while the frequency of the oscillations in the turn-off current in Fig. 8(c) is well estimated by the load inductance–capacitance parasitics. The oscillations observed in V_2 are the result of relatively low common-mode rejection of the measurement.

The deviation of the output voltage from its average value is measured to be around 100 mV. A minor discrepancy is evident between the calculations of L and C for the effective operation range and is due to practical efficiency which is not taken into account in (10). This resulted in a slightly higher bound on the input voltage of 9 V instead of the original 8 V to deliver power of 20 W to the output. The measured efficiency of the converter at 25% load ranged between $\eta = 72\%$ ($V_1 = 15$ V) and $\eta = 83\%$ ($V_1 = 9$ V), matching the calculated efficiency.

Rigorous performance evaluation of the GRSCC for a wide range of operating conditions was carried out and is detailed in [23]. Fig. 9 shows the efficiency as a function of the voltage gain and loading conditions.

VII. CONCLUSION

A new, small and efficient voltage regulator based on resonant switched-capacitor technology has been developed. Detailed analysis of the new RSCC as well as design guidelines, in the context of voltage regulation, is provided and verified by simulations and experiments.

The results have demonstrated that upon a load transient within the nominal value of the design, the operating frequency can be immediately updated (in one switching cycle) to compensate and adjust to the changes. This is similar to SICs operating in DCM and controlled by pulsed FM. This is in contrast to CCM SICs where the inductor current has to build up/down to the new steady-state level, an action that takes several cycles to

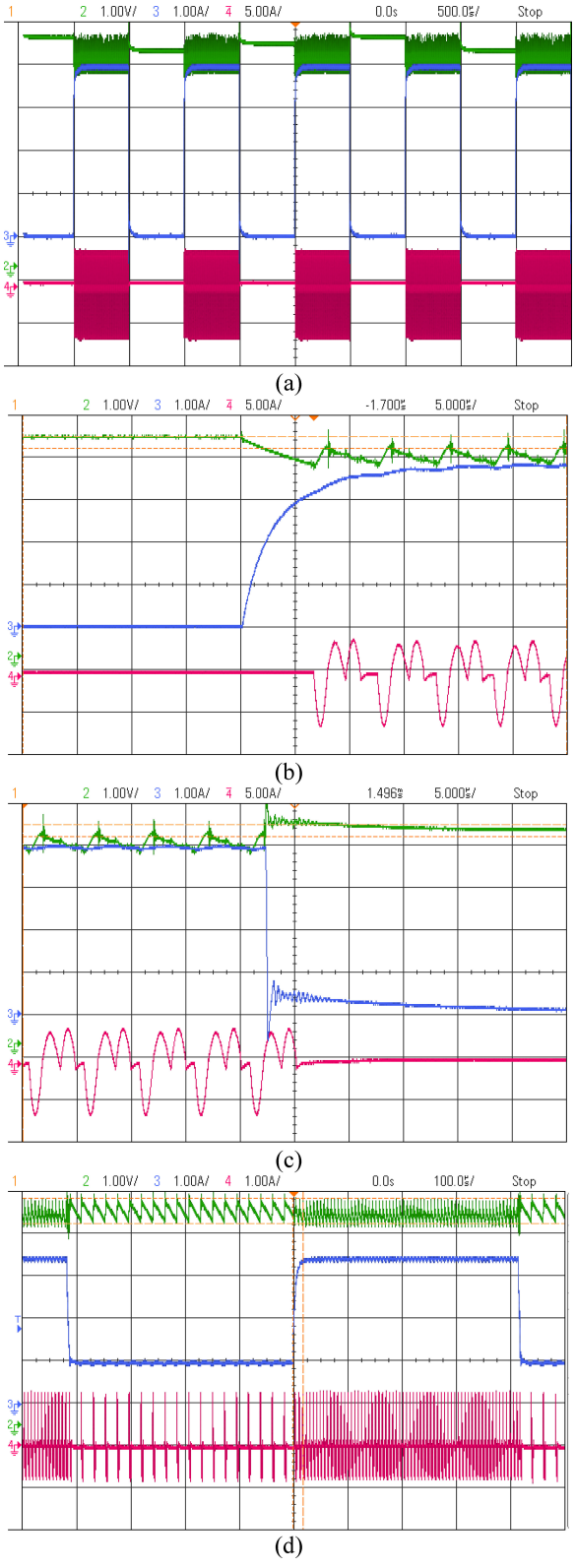

Fig. 8. Screenshots obtained from the experimental setup. $V_1 = 12$ V, $V_2 = 5$ V, $I_2 = \{0\,A, 4\,A\}$. Signals are: top-V_2, mid-I_2, bottom-I_C, (a) zoomed out view on voltage stabilization with full range of load step, $I_2 = \{0\,A, 4\,A\}$ switched repeatedly at 1 kHz, (b) light-to-heavy load step, $I_2 = \{0\,A, 4\,A\}$, (c) heavy-to-light load step, $I_2 = \{0\,A, 4\,A\}$ (d) mid-range load step variation, $I_2 = \{1\,A, 3.5\,A\}$ switched at 1 kHz.

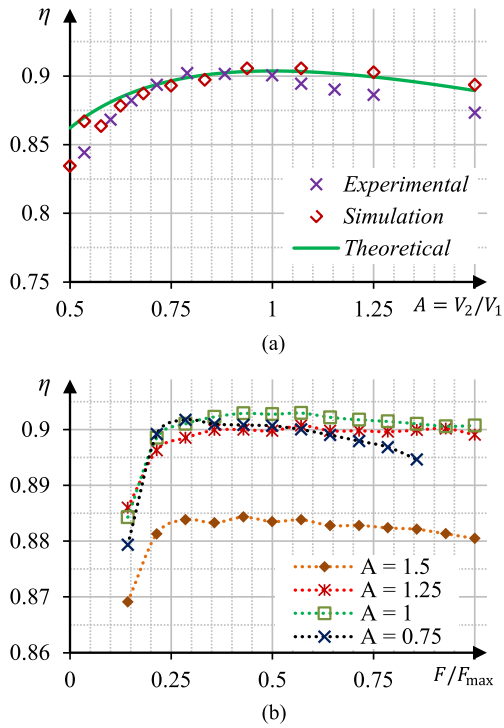

Fig. 9. GRSCC efficiency as a function of: (a) voltage gain and (b) load at different gain values [23].

complete. In the voltage regulator presented here, any transients (line or load) occurring at a rate lower than half of the maximal switching frequency, $F_{\max}/2$, can be compensated without any under/overshoot nor delay, i.e., a zero-order response.

A power density analysis has been carried out to estimate the expected volume of the magnetic element. It revealed that when considering a conservative design the required area product (volume) of the magnetic element is within the range of its comparable candidates (e.g., a buck–boost converter). However, due to the significantly lower inductance value that is required for the operation of the GRSCC, a ferrite-less design is feasible, which increases the power density of the voltage regulator at least one-order of magnitude.

Size estimation of the output capacitor has found that although the output filter has to be sized for a higher peak current, the fact that the voltage regulation can be obtained with zero-order response, i.e., continuous steady-state operation, significantly reduces the required capacitance value and size.

Combining the benefits of the relatively simple converter design, the virtually no-effort approach for voltage regulation presented, and high power density of the passive components, the GRSCC-based voltage regulator can be considered as an attractive candidate for voltage regulation applications that require high response rate. Furthermore, the possibility of a ferrite-less magnetic design increases the power density of the converter, and allows for the power supply to be fully integrated (omitting the output filter) on a chip. It should also be noted that in comparison to other switched-inductor ripple-based solutions, the presented approach is comparable in terms of efficiency and

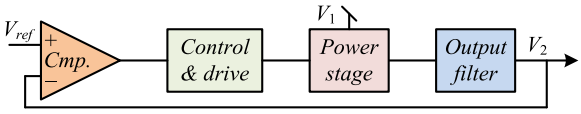

Fig. 10. Block diagram representing the closed-loop operation of a ripple-controlled regulator.

component count, in particular when step up/down or bidirectional capabilities are required.

Appendix A
Average-Behavioral Model (ABM) and Stability Analysis

Assuming that the GRSCC operates under ZCS, the behavior of the voltage regulator presented in this study is similar to ripple-based regulators with constant on-time [43] operating in DCM [44]. The general proof of stability for this type of regulators has been presented in [41] and [43]. However, the details on the behavior of the response to disturbances have not been widely covered. To evaluate the regulator's response and analyze the stability, a generic ABM has been developed and verified by simulations. Without losing generality, the model is directly applied on the GRSCC as the power converter.

As described in Fig. 1, a ripple-based regulator comprises a switch-mode power stage and an output filter that is fed to the inverting terminal of a comparator. The switching sequence to the power stage is triggered by the comparator event. This operation can be represented by the simplistic block diagram of Fig. 10.

The output filter behaves according to the values of C_L and R_L. The output impedance can be expressed as

$$Z_o = \frac{V_o}{I_2} = \frac{R_L}{1 + SC_oR_L}. \tag{14}$$

As mentioned in Section II, the GRSCC power stage that is applied in this study outputs a current I_2 as a function of the input voltage V_1 and the control command F. Assuming ZCS operation, (3) is valid, resulting in a control-to-output transfer function of the form

$$H_F = \frac{I_o}{F} = 2CV_1. \tag{15}$$

The comparator is modeled in this study by the resultant average behavior of the ripple regulator. In the context of the GRSCC, voltage comparison triggers the next charging cycle, effectively generating a frequency command. To analyze the behavior, a charge-based expression is derived as follows. The error between the output and the reference voltages $V_e = V_{\rm ref} - V_o$ corresponds to the missing charge at the output $Q_e = C_oV_e$. Subtracting this value from the charge obtained within a single pulse by the GRSCC, $Q_2 = 2CV_1$, yields the delivered charge from the regulator, Q_o as

$$Q_o = Q_2 - Q_e = 2CV_1 - V_e/C_o. \tag{16}$$

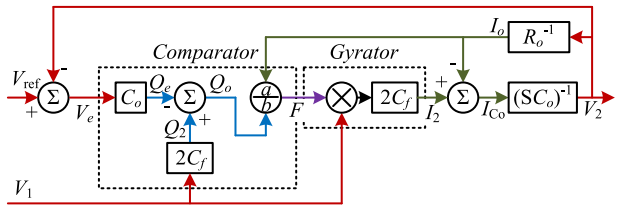

Fig. 11. ABM for the GRSCC voltage regulator.

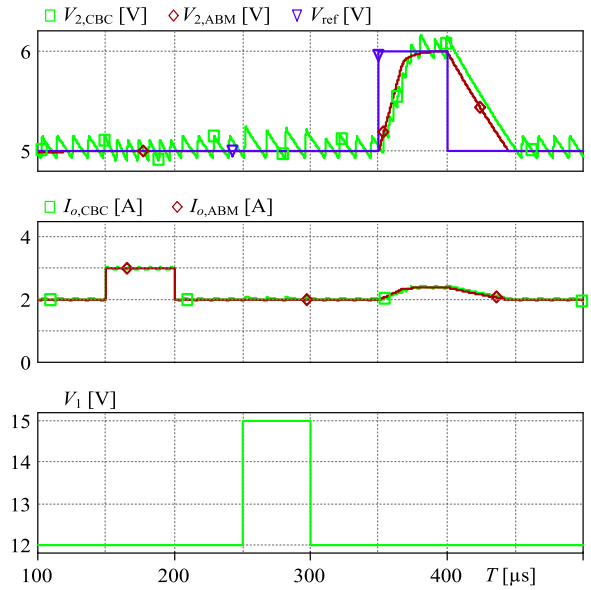

Fig. 12. PSpice simulation which demonstrates the transient behavior of the presented ABM in comparison to a cycle-by-cycle model. Operating conditions and values match those of Table II, with added 50 μs pulse disturbances of $\Delta I_o = 1$ A, $\Delta V_1 = 3$ V, and $\Delta V_{\rm ref} = 1$ V, distributed at 150, 250, and 350 μs accordingly.

The equivalent frequency of the GRSCC is obtained by the information of the load current as

$$F = \frac{I_o}{Q_o} = \frac{I_o}{2CV_1 - V_e/C_o}. \tag{17}$$

To model the physical limitations of the switching sequence, the following constraints are added: F is limited to $F_{\max}$ at under voltage/overload and forced zero at overvoltage. The resultant frequency can be rewritten as

$$F = \begin{cases} 0, & V_e < 0 \\ \dfrac{I_o}{2V_1C_f - V_e/C_o}, & \& \quad Q_o > 0 \\ F_{\max}, & F < F_{\max} \\ & \text{else.} \end{cases} \tag{18}$$

Fig. 11 shows an ABM of the GRSCC voltage regulator with the constraints of (18) omitted for clarity. This nonlinear model is applicable to any modern circuit simulator for both large and small signal analysis. In addition, the model is valid for examining disturbances in the reference voltage as well as in line or load conditions. To validate the model, it has been compared to a cycle-by-cycle simulation as depicted in Fig. 12, using PSpice (Cadence PSpice A/D V16.5). It can be seen that the

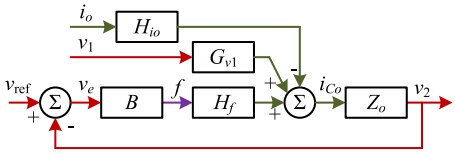

Fig. 13. Linear transfer diagram modeling the small-signal behavior of the GRSCC regulator.

response to line or load transients is immediate (within a single switching cycle) whereas the response to changes in $V_{\rm ref}$ is of first order with slew-rate limitation due to the constraints on F.

To extract the small-signal transfer functions for each of the individual blocks, linearization around an operating point is applied and then followed by a small-signal analysis; the resulting block diagram is shown in Fig. 13. The expressions for each of the blocks are as follows:

$$B = \left.\frac{f}{v_e}\right|_{\substack{i_o=0\\ v_1=0}} = \frac{C_o V_2}{(2CV_1)^2 R_L}$$

$$H_f = \left.\frac{i_{Co}}{f}\right|_{v_1=0} = H_F = 2CV_1$$

$$\frac{v_o}{i_{Co}} = Z_o = \frac{R_L}{1+SC_oR_L}$$

$$G_{v1} = \left.\frac{i_{Co}}{v_1}\right|_{\substack{v_e=0\\ i_o=0}} = -\frac{2I_oCC_o}{(2V_1C-V_eC_o)^2}V_e$$

$$H_{io} = -\left.\frac{i_{Co}}{i_o}\right|_{\substack{v_e=0\\ v_1=0}} = -\frac{C_o}{2V_1C-V_eC_o}V_e \qquad (19)$$

where f, v_e, i_{Co}, v_o, v_1, and i_o are the small signal perturbations around the operating points of F, V_e, I_{Co}, V_o, V_1, and I_o, respectively. Based on Fig. 13 and (19), the small-signal closed-loop transfer function can be expressed as follows:

$$v_o = \frac{BH_fZ_o}{1+BH_fZ_o}v_{\rm ref} + \frac{H_{io}Z_o}{1+BH_fZ_o}i_o + \frac{G_{v1}Z_o}{1+BH_fZ_o}v_1. \qquad (20)$$

Fig. 14 shows the frequency response of the system to perturbations in the reference, input and the loading conditions. The information of the regulator's stability can be directly obtained from (20). The system loop-gain, BH_fZ_o includes a single left-half-plane pole, which suggests the closed-loop response to changes in the reference is stable and of first order. Since the characteristic equation is identical to all the perturbations, the stability of the system to changes in the input voltage or the load depends on H_{io} and G_{v1} alone [45]. As can be observed from (19), H_{io} and G_{v1} are constants and therefore, stability is guaranteed. The response to changes in the line or load introduces relatively high rejection ratio (above 100 dB) which implies that the system is, in fact, immune to these perturbations, confirming the initial objective of the ideal-response voltage regulator.

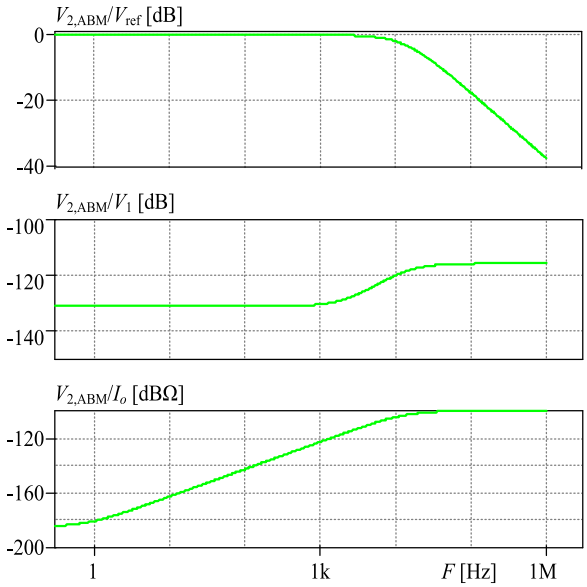

Fig. 14. PSpice frequency-response measurements of the presented ABM to small-signal perturbations at the reference, line and load.

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