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Vertical power MOS transistor as a thermoelectric quasi-nanowire device

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Nano-materials exhibit superior performance over bulk materials in a variety of applications such as direct heat to electricity thermoelectric generators (TEGs) and many more. However, a gap still exists for the integration of these nano-materials into practical applications. This study explores the feasibility of utilizing the advantages of nano-materials' thermo-electric properties, using regular bulk technology. Present-day TEGs are often applied by dedicated thermoelectric materials such as semiconductor alloys (e.g., PbTe, BiTe) whereas the standard semiconductor materials such as the doped silicon have not been widely addressed, with limited exceptions of nanowires. This study attempts to close the gap between the nano-materials' properties and the well-established bulk devices, approached for the first time by exploiting the nano-metric dimensions of the conductive channel in metal-oxide-semiconductor (MOS) structures. A significantly higher electrical current than expected from a bulk silicon device has been experimentally measured as a result of the application of a positive gate voltage and a temperature gradient between the "source" and the "drain" terminals of a commercial NMOS transistor. This finding implies on a "quasi-nanowire" behaviour of the transistor channel, which can be easily controlled by the transistor's gate voltage that is applied. This phenomenon enables a considerable improvement of silicon based TEGs, fabricated by traditional silicon technology. Four times higher *ZT* values (TEG quality factor) compared to conventional bulk silicon have been observed for an off-the-shelf silicon device. By optimizing the device, it is believed that even higher *ZT* values can be achieved. *Published by AIP Publishing.*
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I. INTRODUCTION

New alternative, renewable, energy resources enabling new technological developments and bringing the society one step closer to a cleaner environment are continuously being pursued. Thermoelectrics (TEs) is one of the emerging technologies for a direct conversion of waste heat into useful electricity, enabling the reduction of global reliance on fossil fuels as energy sources and therefore the reduction of automotive fuel consumption and CO_2 emissions.

The efficiency of thermoelectric (TE) materials, converting a heat or temperature difference ΔT into an electric potential difference, ΔV, is quantified using the dimensionless figure-of-merit[1] $ZT = S^2\sigma T/\kappa$, where S, σ, and κ are the Seebeck coefficient, electrical, and thermal conductivity, respectively, at temperature T. In standard configurations, σ and the electronic contribution to κ are both proportional to the carrier concentration of the involved materials. Thus just altering the charge carriers' concentration will not trivially enhance *ZT*. Maximizing the efficiency (*ZT*) of a TE material involves a compromise between all of the involved properties in *ZT*.[1] *ZT* values higher than 1 are desirable for practical applications.[1] To-date, such values have been primarily observed in classic TE alloys (e.g., PbTe,[2] GeTe,[3–5] and BiTe[6]).

The penalty often comes with the use of rare, expensive, and in many cases toxic elements with the aid of synthetic nanostructuring methods, providing effective phonon scattering centers for reduction of κ without adversely affecting the other involved electronic properties.[7]

On the other hand, standard semiconducting materials being employed by the semiconductors industry, such as *p*- or *n*-type doped silicon, have much inferior TE properties in their bulk form. Although silicon is considered as the most abundant and widely used semiconductor with a large industrial infrastructure for low-cost and high-yield processing, bulk Si exhibits a high κ ($\sim$150 W m^{-1} K^{-1} at room temperature), giving $ZT\sim0.01$ at 300 K.[8,9] Nevertheless, some silicon device geometries may overcome this limitation by decoupling the σ, S, and κ correlation. Recent studies report on a significant improvement of the silicon TE qualities by using a nanowire (NW) technology. This approach uses the relatively low thermal conductivity of nanowires which is combined with their high electrical conductivity.[8]

The objective of this study is to examine the feasibility of generating a TE component that is based on bulk silicon technology and yet retaining the superior TE properties of a nanowire (NW) geometry, namely, a bulk silicon component that introduces "quasi-nanowire" (QNW) TE behavior. To demonstrate this phenomenon, a vertical power MOSFET has been selected. This vertical device enabled the generation of controllable temperature gradients at the top and back

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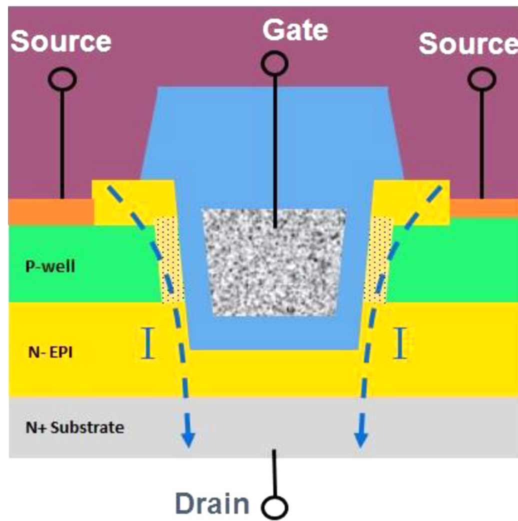

FIG. 1. Schematic cross section of a power n-type MOSFET (not to scale). A typical transistor array is comprised of several thousand cells like this one. N+ source (upper layer), N+ substrate and N-epi (epitaxial) layers are n-type, phosphorous doped silicon layers. P-well is a p-type, boron doped silicon layer. The gate is made of polysilicon. The p-well depth (actual channel length) is 1 μm. The gate to gate single cell pitch is $\sim$2 μm the epi and substrate depth thickness is $\sim$135 μm. The blue layer surrounding the gate conductance (gray) is an insulation oxide layer.

surfaces of the silicon crystal, where the TE properties of the conductance channel are examined in order to validate or disprove a TE-QNW behavior.

By applying gate-to-source voltage above, but in the near vicinity of the transistor threshold voltage, a very narrow conduction channel is created (QNW). This results in higher ZT values when compared with the properties of bulk silicon. A vertical MOS transistor design has been selected for this research (shown schematically in Fig. 1).

When positive gate voltage (V_{GS}) is applied, over the known threshold voltage, V_t, of the transistor, an n-type channel is created (electrons are attracted towards the gate terminal because of the electrical field that is created by the gate voltage). The n-type channel is now "opened." At this point, by supplying a negative voltage gradient (V_{DS}) between the "source" terminal and the N+ substrate ("drain" terminal), the electron current will flow from the "source" to the "drain" terminals. In our work, the channel current is induced not electrically, but by applying a temperature gradient (ΔT) between these terminals. The current flows only while the transistor channel is open (the gate voltage applied is higher than the threshold voltage, V_t).

The induced current is generated because of the Seebeck effect in the transistor channel and the bulk N−/N+ structure. Outside of the n-type channel that was opened because of the "gate" voltage applied, the Seebeck effect could not be observed, because the heated electrons and holes face a potential barrier with a semiconductor of opposite doping type (or in other words, there is no closed circuit that can generate current).

There are few reported studies related to the Seebeck effect in MOS transistors,[10–12] none of them, according to our knowledge, aiming to study the QNW channel properties. The goal of this work is to compensate for this gap, and investigate the feasibility of using silicon semiconductor devices fabricated in a standard microelectronic technology as a superior thermoelectric generator (TEG) by exploiting the QNW effect.

II. EXPERIMENTAL

A standard vertical power NMOS array (by International Rectifier-IRF 1104) was used (shown schematically in Fig. 1). No layout improvements were made in order to achieve the better thermoelectrical characteristics of a standard power transistor array device. The measurement setup scheme is shown in Fig. 2.

All of the measurements were performed in the laboratory under a fixed environmental temperature of 293.4 K. The measured array was placed on a chuck with a controllable temperature. The thermal contact resistance was minimized by using a special metal coating on the back side of the device and a thermal conductive paste. Seebeck effect in the metallization was negligible due to low Seebeck coefficient values in the metals (Al and Ag)[13] applied. The electrical connection to the device was done with microprobes. Two probes were connected to the top "gate" and "source" terminals. The bottom "drain" terminal was connected through the chuck of the probe station. The microprobes were connected through a low-leakage connection to an Agilent 4156B High Precision Semiconductor Tester. The chuck temperature was set using Temptronic temperature controller. The heat flux was applied to the upper surface using a heating blower. For obtaining a reversed thermal gradient (by heating the chuck), the top-side heat removal was done through convection by a cold dry nitrogen blower. The device bottom side temperature was controlled via the chuck temperature. The top temperature was measured using FLUKE TI110 thermal imager. Both temperatures were controlled with an accuracy of 0.1 K. Due to the fact that no real time temperature measurements inside the device were possible, the temperature gradient inside the device was simulated by a ComSol Multiphysics 4.4 thermal modelling. For this purpose, the following

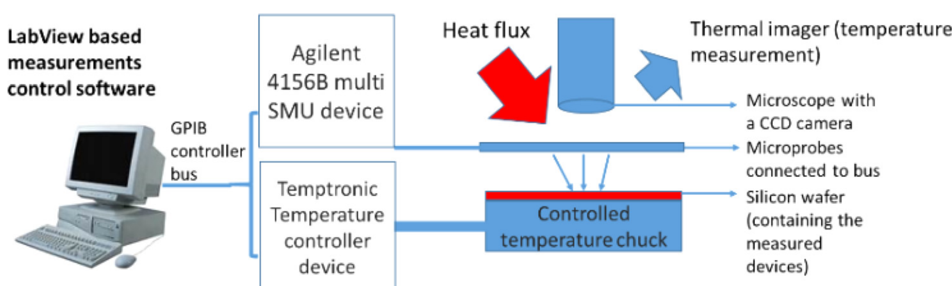

FIG. 2. Laboratory measurement setup scheme.

assumptions were used: (a) all the materials' thermal conductivity, κ, values were set as bulk standard values (including the thermal conductivity in the channel area—this assumption will be argued later); (b) a standard, "Heat Transfer in Solids" model, was used by setting the boundary temperatures as the experimentally applied temperatures. The modelling results showed that the actual drain to source thermal gradient (ΔT) was 95% of the externally applied temperature gradient and just 0.8% of the total gradient that fell on the channel area (our area of interest), indicating a nearly linear temperature gradient through the whole measured device. All of these results refer to the assumption that the thermal conductivity (κ) in the channel area is similar to the κ values of doped bulk silicon, 100 W m^{-1} K^{-1} (Ref. 9) (a very strict assumption that will be treated later). This result was used for *ZT* calculations of the channel layer.

The applied temperature gradients generated on the device was up to $\pm$40 K, the V_{GS} was set at 0–3.5 V, and for each V_{GS} and ΔT values, the stable channel current, I_{DS}, was measured.

III. RESULTS

The measured currents of the closed channel were in the order of nano-amperes, thus clearly indicating that no thermal current occurs while the channel is closed. The charge carriers face two P-N junctions in opposite directions, thus preventing the Seebeck current flow.

The I_{DS} as a function of V_{GS} for the investigated negative ΔT values are shown in Fig. 3. It can be seen that while applying a negative ΔT between the source and the drain, the thermal current is positive. It can be clearly seen that the transistor current is proportional to the absolute temperature gradient. The measured currents were in the order of several microamperes. While applying the opposite temperature gradients, the current direction was opposite to the measured in the previous case, thus showing once again that the current being measured is originated by the thermal gradient on the device. It can also be seen that the current exponentially increases with increasing the gate voltage. A higher gate voltage enhances the charge carrier concentration in the channel and thus contributing to the channel current (lower resistance). It can also be seen that the channel current increases only when the channel is open ($V_{GS} > 2.8$ V) which corresponds with V_t for this kind of transistor, that is over 2.7 V. At $V_{GS} = 3.5$ V the resulting current is up to 20 μA with a total absolute temperature gradient $\Delta T = 35$ K.

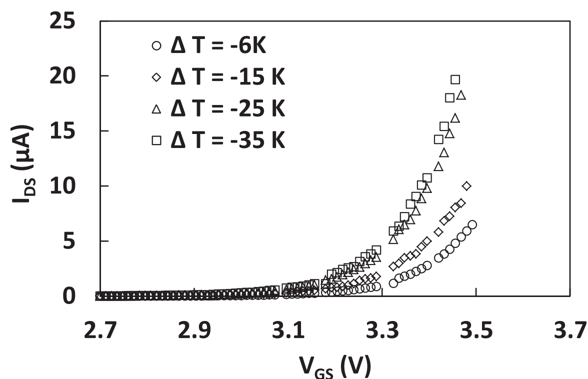

FIG. 3. Device channel current, as a function of gate voltage (near threshold voltage) for different ΔT values.

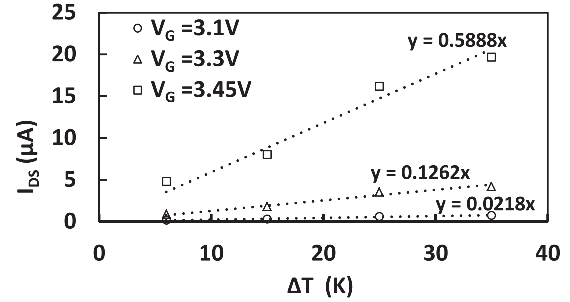

FIG. 4. Device channel current, as a function of ΔT at different gate voltages. The slope of each gate voltage plot is actually an effective Seebeck coefficient of the device for the specific gate voltage, divided by the total device resistance.

In Fig. 4, the channel current as a function of applied ΔT is plotted at different gate voltages. As shown by using the trend lines, in this temperature range, the device temperature gradient and the channel current are in linear proportion.

IV. DISCUSSION

In the investigated configuration, the transistor array is being operated in the linear (ohmic) mode, and hence, the induced channel and the resulted current can be presented according to the following standard transistor formula:[14]

$$I_{DS} = C \cdot [(V_{GS} - V_t) \cdot V_{DS} - V_{DS}{}^2/2], \tag{1}$$

C is a constant that is derived from the known device parameters, its value is calculated from the I_{DS} measurements, which for the current device, it is equal to $4.59 \times 10^{-4}\ \Omega^{-1}$ V^{-1}. In the current case, the applied V_{DS} should be substituted with the thermally induced drain to source Seebeck voltage, which can be farther separated into the bulk and the channel contributions

$$V_{DS} = S\Delta T = S_{ch}\,\Delta T_{ch} + S_{bulk}\,\Delta T_{bulk}, \tag{2}$$

with S, the effective Seebeck coefficient of the device and ΔT the total temperature gradient applied, S_{ch} and ΔT_{ch} are the Seebeck coefficient and temperature gradient of the channel, respectively, and S_{bulk} and ΔT_{bulk} are the Seebeck coefficient and temperature gradient of the bulk silicon, respectively. It can also be assumed that the thermal gradient behaves approximately linear, as a function of the layer length and thermal conductivity

$$\Delta T_{bulk} \approx \Delta T_{ch}\, L_{bulk}/L_{ch}\, \kappa_{ch}/\kappa_{bulk}, \tag{3}$$

with L_{bulk}/L_{ch}, the ratio between the bulk silicon thickness and the channel length, that in our case equals to 130, and $\kappa_{ch}/\kappa_{bulk}$ the ratio between the channel and the bulk thermal conductivities. This last approximation was approved by the COMSOL simulation, and it is valid only as long as κ_{ch} does not differ much from κ_{bulk} (i.e., at least at the same order of magnitude).

Since V_{DS} is much lower than the gate overvoltage, (V_{GS}-V_t), V_{DS}^2 in the current analysis may be neglected, and Eq. (1) can be rewritten as

$$I_{DS} = C\,(V_{GS} - V_t)\,(S_{ch}\,\Delta T_{ch} + 130\,S_{bulk}\,\Delta T_{ch}\,\kappa_{ch}/\kappa_{bulk}). \tag{4}$$

If there is no NW effect at the channel, $S_{bulk} = S_{ch}$ and $\kappa_{ch} = \kappa_{bulk}$, the transistor current is given by

$$I_{DS} = C\,(V_{GS} - V_t)\,(131\,S_{bulk}\,\Delta T_{ch}). \tag{5}$$

It should be noticed, as already mentioned, that in such a case, the actual effective temperature gradient on the channel is 0.8% of the total temperature gradient. Practically, most of the temperature drop is on the thick bulk layers (Fig. 1). For the simplicity of the calculation, the S_{bulk} value was taken as 0.355 mV/K which is an equivalent of the N+ and N− epi layers having Seebeck coefficients of 0.3 mV/K and 1.2 mV/K, respectively.[15] For $V_{GS} = 3.5$ V and $\Delta T = 35$ K, we would expect for $\Delta V = 35 \times 0.355 \approx 12.4$ mV, thus, the measured current should be ~4.5 μA, however, the actual current that was measured in this condition was much higher, up to 20 μA (see Fig. 3). One can argue that this difference, i.e., actual current that is more than 4 times higher than its calculated value, is a result of the temperature dependence of the transistor in its active region. In such a case, it should be expected that for a lower ΔT, where the transistor's average temperature is closer to room temperature, this effect will be vanished. However, repeating the above calculation for lower ΔTs resulted in even higher differences, reaching a factor of more than 8 for $\Delta T = 6$ K. Hence, the reason for this difference should be looked elsewhere. As can be seen from Eq. (4), since S_{bulk} and κ_{bulk} as well as the device geometry are all known, the only two parameters that can explain this deviation between the calculated and the measured current are higher S_{ch} and/or lower κ_{ch} (which corresponds to a higher ΔT_{ch}). It means that the channel area has a much higher Seebeck coefficient or much lower thermal conductivity than the bulk silicon, indicated here as a QNW behavior.

If this QNW behaviour only influences S_{ch} ($\kappa_{ch} \approx \kappa_{bulk}$) then Eq. (4) is still valid and S_{ch} can be estimated by equating the measured I_{DS} to the calculated one. Applying it, for the same experimental point as before ($V_{GS} = 3.5$ V, $\Delta T = 35$ K), results in a calculated S_{ch} value of ~150 mV/K which is more than two orders of magnitude higher than the Seebeck coefficient of bulk silicon with the same doping,[15] which is clearly not physical.

Hence, it should be assumed that this QNW behaviour influences also κ_{ch}. It was shown[16,17] that for nano scaled silicon structures, the κ value can even go down to 1 W/m^{-1} K^{-1}. Since in the investigated case study $\kappa_{ch} \neq \kappa_{bulk}$, Eqs. (3) and (4) are no longer valid and ΔT_{ch} and ΔT_{bulk} should be calculated using the COMSOL simulation. In this case, 25% (instead of previous 0.8%) of the total temperature gradient falls on the channel. Using these ΔT values and Eqs. (1) and (2) for equating the measured I_{DS} to the calculated, the obtained S_{ch} value is only ~3 times higher than that of the bulk silicon with a similar doping. The same values were reported in previous studies by different groups for nanoscaled thin silicon films with a high surface roughness,[15] which is similar to our case, since the channel width is only 5–8 nm,[18] thus the electrical current carriers move in a nanoscaled area that is close to the GOX (gate oxide) area boundaries.

Exploring the QNW behavior of the channel area, or in other words its deviation from a bulk-like behavior, upon varied V_{GS} voltages, indicates an interesting result, with a maximal deviation at $V_{GS} \approx 3.2$ V. This can be explained by the fact that at too low V_{GS} values, the channel's electrical conductivity, σ, is still too low to allow a high TE efficiency, or ZT (remembering that $ZT = S^2\sigma T/\kappa$), while at too high V_{GS} values, the channel width increases, gradually diminishing the QNW behaviour. Hence, as expected, there is an optimal value of V_{GS} for maximizing the TE efficiency. The calculated ZT value at this maximum efficiency point is ~0.04, which is ~4 times higher than that of the bulk silicon.

This demonstration of a QNW behavior enables to combine the high TE potential of NW silicon, which is still far from being a technologically ready device; with the well-established transistor technology; which is an important step for commercializing highly efficient silicon-based TE devices.

V. CONCLUSIONS

By applying a thermal (instead of the conventional electrical) gradient to a vertical NMOS transistor and applying a gate voltage above the threshold, much higher electrical currents were measured, with respect to the expected conventional bulk material values. This effect which is attributed to a QNW behavior of the transistor's channel, results in $ZT \sim 0.04$ (instead of $ZT \sim 0.01$ for bulk silicon) without any device improvements. The optimal TE performance was achieved for a gate voltage slightly above V_t (~3.2 V).

The results clearly indicate that using QNW-like structures, significantly higher TE conversion efficiencies compared to bulk silicon are expected which may be practically applied in standard microelectronic devices, for example, for power dissipation or energy harvesting.

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