Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

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***Abstract*—This paper introduces a new voltage regulator module (VRM) that merges a highly efficient switched-inductor converter as the main unit with a load-side switched-capacitor-based converter to assist during load transient events. The resulting hybrid-VRM exhibits improved dynamic performance for both loading and unloading transient events, while maintaining a compact design with reduced output capacitance and lower components stress. The hybrid controller that has been developed allows operation that is based on output voltage measurement alone, further reducing the circuit complexity. A power processing efficiency analysis that has been carried out shows efficiency improvement in favor of the hybrid-VRM when compared to time-optimal control under varying load conditions. The operation of the VRM is verified on a 20-W, 12V-to-1.5-V prototype with peak power conversion efficiency of 93%, demonstrating near-ideal transient recovery.**

***Index Terms*—Auxiliary circuit, digital control, improved transient-response, optimal control, switch-mode power supply, voltage regulation module.**

I. Introduction

In recent years, there has been a sharp rise in interest and demand for more compact, light, energy efficient, and economical voltage regulation solutions. In particular, tighter output voltage regulation, faster response times, and lower volume are of major concern in the design of present-day voltage regulator modules (VRMs). For processing power from fractions of a watt to several tens of watts with fast transient performance, multistage interleaved converters combined with analog controllers have been predominantly used [2]–[6]. There, fast response is usually achieved by designing a wide bandwidth control loop.

The advancement in hardware-efficient digital controllers [7]–[11] enabled the implementation of advanced nonlinear control methods that improve the dynamic performance and, as a consequence, drastically reduce the size of the output capacitor. Among them, time-optimal control (TOC) [12]–[17] and minimum-deviation [18] controllers have demonstrated transient response with virtually the smallest possible voltage deviation, restricted only by the inductor current slew-rate. In VRM applications, this limitation has a major effect on the output voltage deviation for the case of an unloading transient event, primarily due to the high input-to-output conversion ratio. Another weakness of the classical time-optimal approach is the relatively higher current stress, beyond the steady-state value, that is required to restore the lost charge of the output capacitor during the recovery time [19]. As a result, the overall power processing efficiency is impacted from consecutive transients, when compared to the steady state [20].

The state-of-the-art solutions that exceed the performance of the TOC method propose several circuit extensions to the original buck converter [21]. To deliver the current to the load with higher slew-rate, modifications that apply higher voltage on the inductor during load transients [22], [23] or to reduce the actual inductance of the main inductor [24], [25] have been proposed. Other extensions present an addition of a fast auxiliary converter in parallel to the main converter with smaller inductance [26]–[29], with a resonant circuit [30], with switching resistors [31]–[33], or with active region current injection circuit [34]–[37]. However, this comes at the cost of an increased input filter since the load transient is reflected to the input, and the switches of the auxiliary stage must be rated to the higher voltage of the system. This is partly resolved by compensating only for half of the current mismatch, which does not increase transient time [38]. Regulation of such auxiliary circuits requires additional sensors, which increases the realization, control, and system complexity.

Recent studies have reported improved loading and unloading transient performance, obtained using an auxiliary converter connected to the output side [39], [40]. An independent energy bank is used, eliminating the impact on the input and employs switches with lower voltage ratings, further reducing the power loss and size of the system. Although these solutions require additional sensors to regulate the auxiliary circuit's operation and are limited by switching frequency to mid-range output voltages, they provide a new concept to improve the performance of VRMs and therefore adopted in this study.

A recently developed resonant switch-capacitor-based gyrator converter (GRSCC) presented in [41] demonstrated an ultra-compact voltage regulator solution which obtains ideal transient response [42]. However, a modest efficiency (around 85%) at steady state is achieved due to high rms currents. Nonetheless, its main advantage is that no magnetic element is required, allowing on-chip integration.

Manuscript received December 3, 2015; revised March 20, 2016; accepted April 27, 2016. Date of publication May 6, 2016; date of current version December 9, 2016. This is an extended version of a paper presented at the *Applied Power Electronics Conference and Expo.*, 2015, Mar. 15–19, at Charlotte, NC, USA [1].

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Digital Object Identifier 10.1109/TPEL.2016.2564698

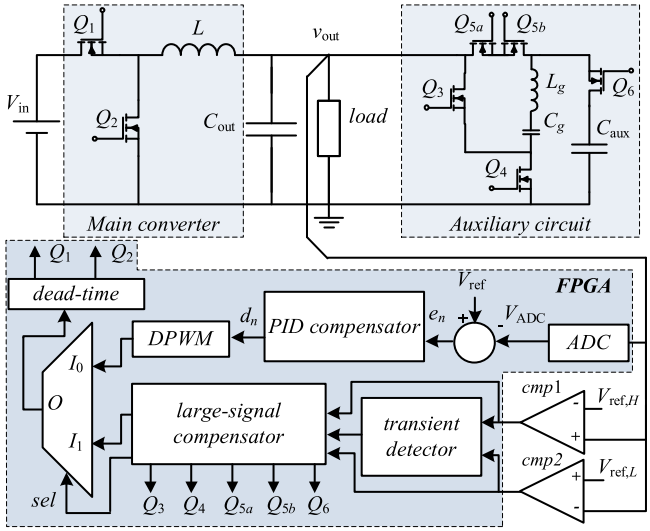

Fig. 1. Hybrid-VRM with the load-side GRSCC auxiliary circuit. The area within the bottom box is implemented within an FPGA.

The objective of this study is to introduce a new compact VRM solution that *merges a buck converter with a resonant switched-capacitor auxiliary circuit that is connected at the load side*, as detailed in Fig. 1. By incorporating a new control concept, the auxiliary circuit effectively mimics increased capacitance during loading and unloading transient events, reducing the burden on both the input and output filters, and reduces the current stress. In addition, the hybrid-VRM presented in this study *requires indication from the output voltage alone and implemented using a simple state-machine-based controller*, making this solution simple and cost-effective.

This paper is organized as follows. Section II describes the effect of different auxiliary current profiles on the transient-recovery performance and Section III discusses the improvement in power-processing efficiency. The implementation of the GRSCC as an auxiliary circuit is delineated in Section IV. Next, the details of the control scheme for the hybrid-VRM are detailed in Section V. Experimental results and conclusions are then provided in Sections VI and VII, respectively.

II. Transient Recovery by a Load-Side Auxiliary Circuit

A key factor for assisting the recovery of the main converter from a load transient is the capability of the auxiliary circuit to rapidly sink or source the current mismatch between the new load state and the main inductor current. To analyze the required behavior and control mechanism of the auxiliary unit, an idealized bidirectional current source that is connected to the output terminals of the voltage regulator can be assumed as depicted in Fig. 2.

The analysis is aided by Fig. 3 which shows average waveforms for different sinking patterns of the current source to a current unloading step of $\Delta I_{\rm out}$. It is further assumed that a time-optimal-like control is implemented for the main converter to maximally expedite the recovery phase.

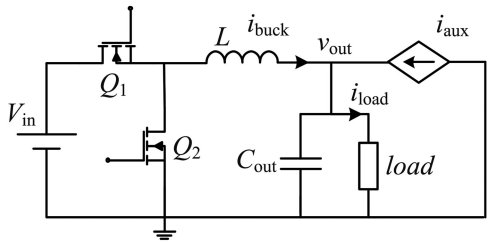

Fig. 2. Simplified circuit with the auxiliary circuit modeled as a controlled current source, demonstrating the current relationships toward the load.

To eliminate any deviations of $v_{\rm out}$ from the steady-state value $V_{\rm out}$, the auxiliary circuit is to mimic infinite capacitance, i.e., mirror the mismatch between $i_{\rm buck}$ and $i_{\rm load}$. As shown in Fig. 3(a), the auxiliary current $i_{\rm aux}$ is triangular, ramping down from $\Delta I_{\rm out}$ and reaching zero, when $i_{\rm buck}$ equals $i_{\rm load}$. In this case, the total transient time $T_{\rm tr}$ is governed by the main inductor current slew-rate and current mismatch, and can be expressed as

$$T_{\rm tr,loading} = \frac{L}{V_{\rm in} - V_{\rm out}} \Delta I_{\rm out} \quad , \quad T_{\rm tr,unloading} = \frac{L}{V_{\rm out}} \Delta I_{\rm out} \tag{1}$$

where L is the main inductor value and $V_{\rm in}$ is the input voltage. This case produces a significantly shorter transient time than obtained using classical TOC approach since no additional discharging is required to drain excess charge from $C_{\rm out}$.

Realization of an auxiliary unit as described by Fig. 3(a), rated for the peak load current is, to some extent, over designed. It requires higher stress-rating components to accommodate for stress that exists for slight fractions of the transient time. Furthermore, an ideal response with zero-voltage deviation is not an objective of a VRM. Even in tight VRM applications, some amount of voltage deviation is still tolerable by standard [43], and therefore more conservative approach can be taken. As shown in Fig. 3(b), improved unloading transient recovery, provided some allowed deviation margins, can be achieved by a constant current sinking profile of $I_{\rm aux} = \Delta I_{\rm out}/2$. It can be seen that although $v_{\rm out}$ initially deviates from $V_{\rm out}$, it is fully restored at $T_{\rm tr}$. In the aforementioned cases, the current source sinks an identical charge within $T_{\rm tr}$, meaning that the initial undercurrent is ultimately balanced by the overcurrent at the second half of the transient. Considering a maximum allowed overshoot of $\Delta V_{\rm out}$ and the greatest possible load change $\Delta I_{\rm max}, C_{\rm out}$ is sized as follows:

$$C_{\rm out} = \frac{\Delta I_{\rm max}^2 L}{8 \Delta V_{\rm out} V_{\rm out}}. \tag{2}$$

When compared to TOC, the shorter transient times and the smaller initial current mismatch are in favor of a hybrid-VRM, resulting in $C_{\rm out}$ which is four times smaller.

The method shown in Fig. 3(b) reduces the complexity of the auxiliary circuit compared to the method in Fig. 3(a), however, it requires a fairly accurate estimation of the load current. To overcome this obstacle, a recovery pattern as shown in Fig. 3(c) is suggested. In this method, the auxiliary current is set to $I_{\rm aux} = \Delta I_{\rm max}/2$ (by design), while the instantaneous $\Delta I_{\rm out}$

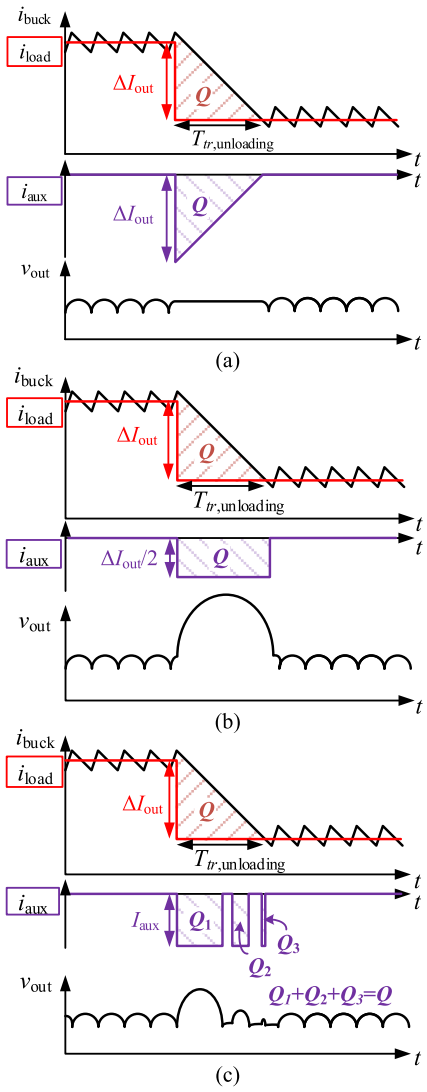

Fig. 3. Schematic response waveforms of the hybrid-VRM to an unloading step of $\Delta I_{\rm out}$ for different auxiliary behavior. (a) $i_{\rm aux} \approx i_{\rm load} - -i_{\rm buck}$, (b) $I_{\rm aux} = \Delta I_{\rm out}/2$, and (c) $I_{\rm aux} > \Delta I_{\rm out}/2$, segmented to match the overall charge Q.

is unknown. As long as $I_{\rm aux} \geq \Delta I_{\rm out}/2$, the resultant total transient time remains $T_{\rm tr}$, governed by the main inductor current slew-rate.

The design of an auxiliary source that compensates for $\Delta I_{\rm max}/2$ provides two main advantages: 1) the transient controller can be realized based purely on sensing the output voltage and without additional current sensing and 2) the conditions for the end-of-transient are within the main inductor current slew-rate for any given transient, without the need for extra time to reestablish the steady-state voltage.

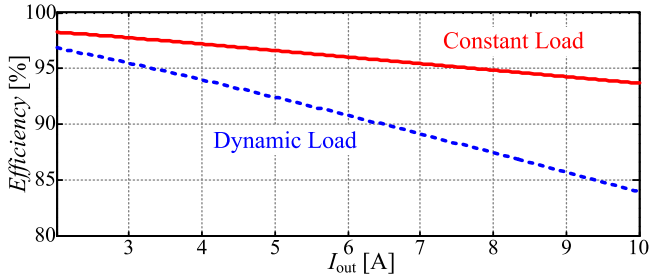

Fig. 4. Power processing efficiency of a buck converter connected to a constant load, versus a 50-kHz dynamic load with the same average current, 50% load duty-ratio (see Fig. 5).

III. Power Processing Efficiency

Present-day efficiency estimations for dc–dc converters are performed with general assumption of the steady-state operation as the dominant working condition, defined here as static conversion efficiency. Neglecting switching losses and assuming steady-state operation, the main contributor for the conduction losses is the average inductor current since the rms current of the ripple component is negligibly small [44].

These estimations for the efficiency are relatively accurate for most applications in which the load is static or mostly static. However, for modern applications with continuously varying loading conditions, the static conversion efficiency estimation might fail to predict the actual losses and as a consequence the required thermal design of the system. Fig. 4 shows comparison of a typical static efficiency curve compared with a dynamic loading one for a similar average output power. As can be observed, the deviation of the static efficiency estimation from actual one significantly increases with the load repetition rate. It should also be noted that the situation worsen for applications with relatively high conversion ratios, such as the VRM case.

To analyze the converter efficiency under varying load conditions, three cases are compared as shown Fig. 5: an ideal inductor current behavior, TOC [13], and beyond time-optimal one [31] which is adopted in this study. To focus on the difference between the controllers types, it is assumed that all methods are governed by an identical steady-state control law.

Without loss of generality, the analysis to obtain the rms value of the inductor current for all cases is carried out under the assumption of a repetitive load transient with magnitude of $\Delta I_{\rm out}$ and repetition rate of $f_{\rm tr}$ and duty ratio of 50%. For the TOC case, the rms value of the inductor current can be expressed

$$I_{L,\mathrm{RMS-TOC}} = \sqrt{\left(I_{\min}+\frac{\Delta I_{\rm out}}{2}\right)^2+\left(\frac{\Delta I_{\rm out}}{2}\right)^2+\frac{\Delta I_{\rm ripple}^2}{12}-\frac{\Delta I_{\rm ripple}^2\,\Delta I_{\rm out}\,L\left(1+\sqrt{D}+\sqrt{1-D}\right)}{12D\left(V_{\rm in}-V_{\rm out}\right)}f_{\rm tr}+\frac{\Delta I_{\rm out}^3 L}{12}\left(\frac{\left(1+\sqrt{D}\right)^3+\sqrt{1-D}^3}{V_{\rm in}-V_{\rm out}}+\frac{\sqrt{D}^3+\left(1+\sqrt{1-D}\right)^3}{V_{\rm out}}\right)f_{\rm tr}}. \quad (3)$$

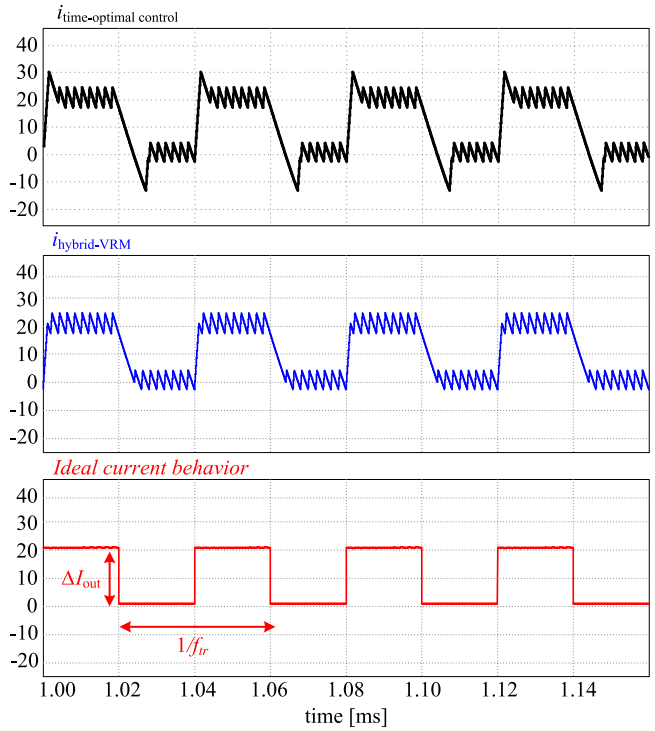

Fig. 5. Inductor current waveforms for TOC (top), hybrid-VRM (middle), and ideal inductor behavior (bottom).

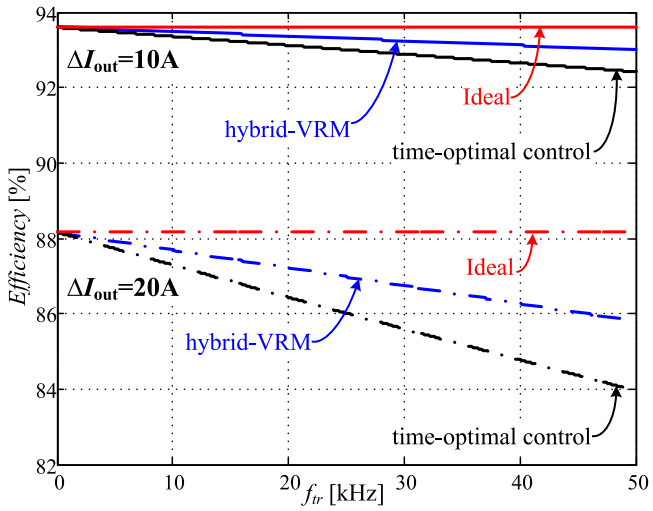

Fig. 6. VRM efficiency as a function of the load transient rate for two load-step magnitudes. $R_{\text{buck}} = 10\ \text{m}\Omega$, $R_n = 2$, switching losses are not considered.

as (3), shown at the bottom of the previous page, where $I_{\min}$ is the load current at light load, $I_{\min} + \Delta I_{\text{out}}$ is the load current at heavy load, ΔI_{ripple} is the inductor's steady-state current ripple, and D is the steady-state duty-ratio, i.e., $D = V_{\text{out}}/V_{\text{in}}$.

Applying the hybrid-VRM control, the inductor current peaks, over and under the steady-state value, are eliminated, and the transient time is reduced, resulting in the rms current (4), shown at the bottom of the page, whereas the auxiliary circuit rms current value is given by

$$I_{\text{RMS,aux}} = \sqrt{\frac{\Delta I_{\text{out}}^3 L}{3D\left(V_{\text{in}} - V_{\text{out}}\right)} f_{\text{tr}}}. \tag{5}$$

Since the hybrid-VRM consists of two current paths with different resistances, i.e., one through the buck converter and the other through the auxiliary circuit, the rms current value of the hybrid-VRM that should be used to calculate the conduction losses and efficiency is given by

$$I_{\text{RMS,hybrid-VRM}} = \sqrt{I_{L,\text{RMS,hybrid-VRM}}^2 + I_{\text{RMS,aux}}^2 R_{\text{n}}} \tag{6}$$

where R_{n} is the ratio between the current path resistance in the auxiliary circuit and the buck converter, i.e., $R_{\text{n}} = R_{\text{aux}}/R_{\text{buck}}$.

The comparison of the resultant efficiency curves of (3), (6), and the ideal current waveform as a function of the load transients rate is shown in Fig. 6. As can be observed, the elimination of the additional restoration current, i.e., peaks, reduces the overall rms current that in turn increases the power processing efficiency. In addition, another design concern is the inductor sizing. As derived in [19], TOC results in current overshoot of $\Delta I_{\text{out}}\sqrt{D}$ and undershoot of $\Delta I_{\text{out}}\sqrt{1-D}$ during loading and unloading transients of ΔI_{out}, respectively. Since these are eliminated by the hybrid-VRM approach, the sizing of the main inductor reduces as well.

IV. Gyrator Resonant-Switched-Capacitor Converter Auxiliary Circuit

The GRSCC topology has been recently presented in [41], based on the concept of a resonant switched-capacitor converter, but with the capability to maintain high efficiency over a wide and continuous step-up/down conversion ratio. Thanks to its soft-switching resonant nature it is applicable at high frequencies, and as a consequence, does not require a magnetic element. Furthermore, it has a bidirectional current sourcing behavior and is able to react *immediately* to create current step response with bandwidth of up to half its maximal switching frequency [42].

A voltage doubling variation of the GRSCC has been implemented in this study and is shown as the auxiliary circuit of Fig. 1. It is structured relying on a voltage multiplying resonant-switched capacitor converter topology, shifting the GRSCC's optimal efficiency point from V_{out} to $V_{\text{aux}} = 2V_{\text{out}}$. The main reason for the selection of this topology is to increase the power

$$I_{L,\text{RMS,hybrid-VRM}} = \sqrt{\left(I_{\min} + \frac{\Delta I_{\text{out}}}{2}\right)^2 + \left(\frac{\Delta I_{\text{out}}}{2}\right)^2 + \frac{\Delta I_{\text{ripple}}^2}{12} + \frac{\Delta I_{\text{out}} L\left(\Delta I_{\text{out}}^2 - \Delta I_{\text{ripple}}^2\right)}{12D\left(V_{\text{in}} - V_{\text{out}}\right)} f_{\text{tr}}} \tag{4}$$

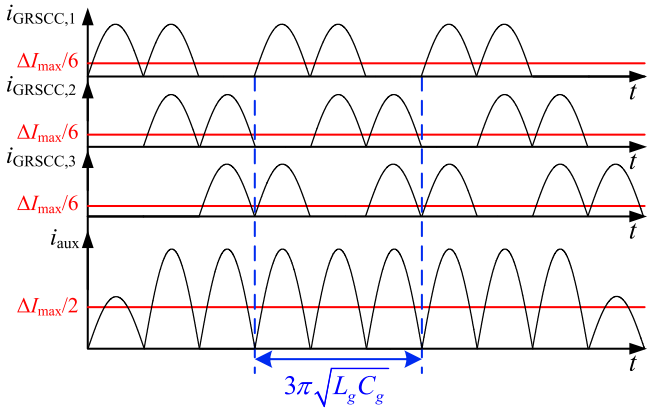

Fig. 7. Distribution of the auxiliary current between three interleaved GRSCCs operating at maximum frequency with half-resonance phase delay.

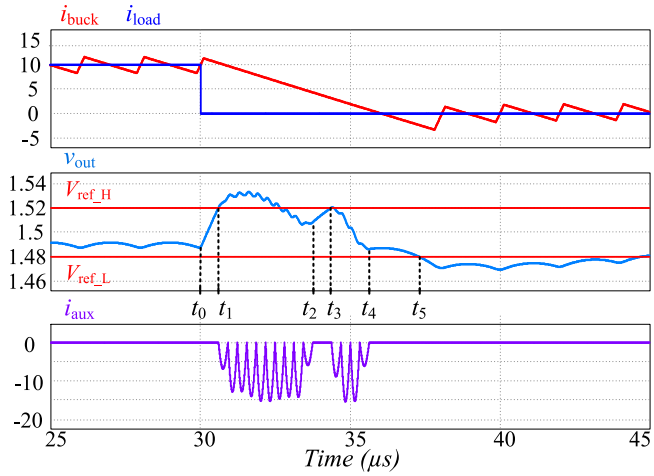

Fig. 8. Simulation results for the response of the hybrid-VRM to an unloading event.

density of the auxiliary storage capacitor $C_{\rm aux}$ by increasing its rated voltage, but without adding voltage stress to the transistors. Another advantage of the doubling realization is that the desired load-side current, i.e., $\Delta I_{\rm max}/2$, can be obtained by a higher characteristic impedance of the resonant network. This implies that higher target efficiency of the GRSCC can be obtained for a given loop resistance.

The GRSCC is resonant in nature and can be completely halted at the zero current after each cycle. As a result, the nominal current can be resumed within one cycle. In the context of this study, this zero-order step capability enables the GRSCC to be used as the auxiliary current source unit. Moreover, there is no limitation to scalability, the resonant tank values can be determined for any desired $V_{\rm out}$ and operating frequency with further option of interleaved operation. The bridge configuration also guarantees that the maximum stress on any given switch will be around $V_{\rm out}$, which translates into small area requirements of the power switches.

To further reduce the overall volume of system and enhance the auxiliary circuit's efficiency, it is realized in this study using three small interleaved GRSCC modules, each designed to output $\Delta I_{\rm max}/6$, operating with phase delay of a half-resonance period, as demonstrated in Fig. 7. By doing so, the auxiliary circuit rms current is reduced by a factor of $(2/3)^{0.5}$, when compared to a single-converter equivalent since there are more smaller pulses that are evenly distributed over the transient phase, for the same average current. This configuration also increases the accuracy and resolution as a current source. Furthermore, lower current is required per module, allowing higher impedance of the resonant network.

The magnitude of the auxiliary current $I_{\rm aux}$ when using three GRSCC units for both loading and unloading transients follows the gyrator relationship with the auxiliary capacitor voltage $V_{\rm aux}$, is given by

$$I_{\rm aux} = 6\, V_{\rm aux} f_g C_g \tag{7}$$

where f_g is the desired switching frequency of the GRSCCs and C_g is the capacitance of the GRSCCs' resonant tank. The accuracy and resolution of the current source depend on f_g, and therefore, it should be designed to be higher than the main converter's switching frequency f_s. For a selection of f_g, by setting $V_{\rm aux} = 2V_{\rm out}$ to obtain the optimal GRSCC efficiency and by using (7), the value of C_g can be extracted

$$C_g = \frac{I_{aux}}{12 V_{\rm out} f_g} \tag{8}$$

and the resonant characteristics of the GRSCCs yield the inductance L_g to operate at the desired frequency

$$L_g = [(3\pi f_g)^2 C_g]^{-1}. \tag{9}$$

V. Hybrid-VRM Controller

The configuration of the hybrid-VRM controller is divided into two main units as shown in Fig. 1: a steady-state voltage-mode controller that is entirely implemented on field-programmable gate array (FPGA) [45] and a transient-mode controller.

The possible solutions to achieve high-performance transient response are to measure the output capacitor's di/dt value [34] or dv/dt value [8], [38]. However, these solutions usually require prior information or estimation on the converter's components and high-bandwidth accurate sensors, which further increase the implementation complexity and cost of the system. In this study, in order to maintain the hardware requirements at minimum, the transient-mode controller is assisted by two auxiliary comparators with two thresholds, well below the maximum allowed voltage deviation, to facilitate fast transient detection and end-of-transient phase, as delineated in this section.

A. Principle of Operation

The description of the hybrid-VRM controller operation is assisted by Fig. 8 which provides in-detail the response for an unloading transient event.

At $t < t_0$, the controller operates the buck converter with a voltage-mode steady-state compensator whereas the GRSCCs are idle. A load step at t_0 creates current mismatch between

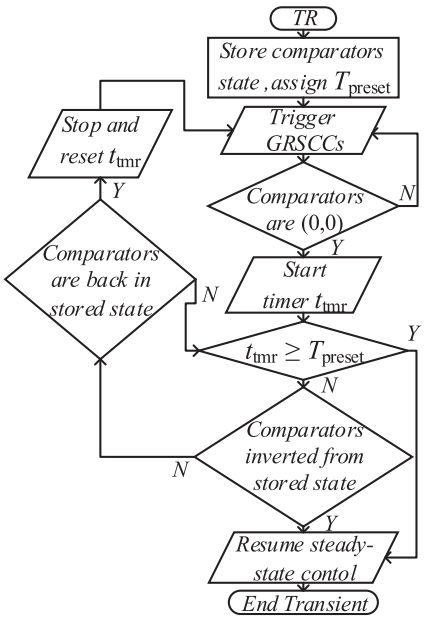

Fig. 9. Flowchart of the end-of-transient algorithm.

$i_{\rm buck}$ and $i_{\rm load}$ resulting in a rise of $v_{\rm out}$. At t_1, when $v_{\rm out}$ crosses $V_{\rm ref,H}$, an unloading event is detected by *cmp*1 (see Fig. 1) and a transient mode is initiated: Q_2 is turned ON to ramp $i_{\rm buck}$ down with the highest slew-rate available. Simultaneously, the GRSCCs are activated to sink excess current and are set to $I_{\rm aux} = \Delta I_{\rm max}/2$. Since $\Delta I_{\rm out} < \Delta I_{\rm max}$, at instance t_2, $v_{\rm out}$ returns within the steady-state range below $V_{\rm ref,H}$, the GRSCCs' operation is halted while Q_2 remains ON, however, $i_{\rm buck}$ is still larger than $i_{\rm load}$. This results in the output voltage rising over $V_{\rm ref,H}$ at t_3 which re-triggers the GRSCCs. When $v_{\rm out}$ is within the steady-state range at t_4, $i_{\rm buck}$ approximately equals to $i_{\rm load}$. The end of the transient phase (t_5), in this case, is due to $v_{\rm out}$ crossing $V_{\rm ref,L}$, detected by *cmp*2.

The information on the end-of-transient is derived, in this study, from the output voltage measurement by observing the comparator states. However, the information that is obtained from the output voltage indicates on the current charge state of the output capacitor and not directly on the current mismatch between $i_{\rm buck}$ and $i_{\rm load}$. Given the example of Fig. 8 (t_2), it can be observed that the output voltage is momentarily restored to the steady-state value without reaching the point that $i_{\rm buck}$ equals $i_{\rm load}$. The reason for this is that the charge balance has been achieved by the aid of the auxiliary circuit.

To overcome the problem of premature indication on the end-of-transient, without additional current sensors, a state-machine algorithm described by the flowchart of Fig. 9 has been developed. The controller monitors the output voltage by observing the comparator states. When $v_{\rm out}$ returns within the steady-state thresholds, the GRSCCs are immediately halted whereas the buck converter remains is the transient mode. In case that a current mismatch still exists, the output voltage is shifted back beyond the boundaries, and the auxiliary circuit is retriggered.

An end-of-transient indication (i.e., $i_{\rm buck}$ is in the vicinity of $i_{\rm load}$) happens when the comparators state has been inverted from the original transient-mode trigger. In the majority of cases, due to the use of $v_{\rm out}$ as a single indicator for the comparators, a small current mismatch may exist, as can be observed at t_5 in Fig. 8. To provide an additional layer of protection and minimize any current mismatch, without additional current sensors, a time limit has been added starting when $v_{\rm out}$ has returned within the comparators thresholds without change in the comparators states (detailed in Section V-C). In case the preset time has elapsed, an end-of-transient is detected and the steady-state voltage mode control is resumed.

B. Comparators Thresholds Settings

A finite voltage difference between the comparators thresholds is required to prevent the controller from falsely entering or exiting the transient mode. To prevent false entry, it is sufficient to satisfy that the voltage difference between the thresholds is well above the steady-state voltage ripple and accounting for additional noise errors (e.g., ESR, switching noise, and other measurement errors). However, to prevent a false indication of the comparators state and an early return to the steady-state mode, the difference between thresholds should be set such that the largest voltage deviation generated from a single discharge cycle of the auxiliary circuit is kept within the threshold boundaries. The largest value for this deviation occurs when current mismatch is small ($i_{\rm buck} \approx i_{\rm load}$), that is,

$$V_{\rm ref,H} - V_{\rm ref,L} \geq Q_g / C_{\rm out} + |\varepsilon_n| = 4V_{\rm out}C_g / C_{\rm out} + |\varepsilon_n| \tag{10}$$

where Q_g is the charge delivered from the auxiliary circuit during a single discharge cycle, C_g is the GRSCC resonant tank capacitor, and ε_n are additional measurement errors. The selection of the voltage detection window, i.e., the difference between the comparator's thresholds, according to (10) assures that the voltage drop due to a single GRSCC pulse is contained within thresholds. The voltage detection window should be kept as small as possible to prevent delayed transient detection which results in longer transient time and larger output voltage deviation as analyzed in [33].

C. Auxiliary Circuit Halt Time—$T_{\rm preset}$

As described earlier, steady-state operation may be resumed by either inversion of the comparators state or after specific time has elapsed since the auxiliary circuit was halted ($T_{\rm preset}$ in Fig. 9). Given the controller sequence when the steady state is resumed, and estimation on the range of error for the buck inductor current at that instance, the preset time can be set to assure that the steady-state operation is restarted without creating additional oscillations. In this study, it is defined that the first switching action of the steady-state controller is the opposite of the one obtained in the nonlinear mode, i.e., resuming from an unloading event starts with an on state, whereas an on state during a loading event is followed by an off state. This implies that the preferred instance to switch back to the steady state is when the inductor current has passed the target load current

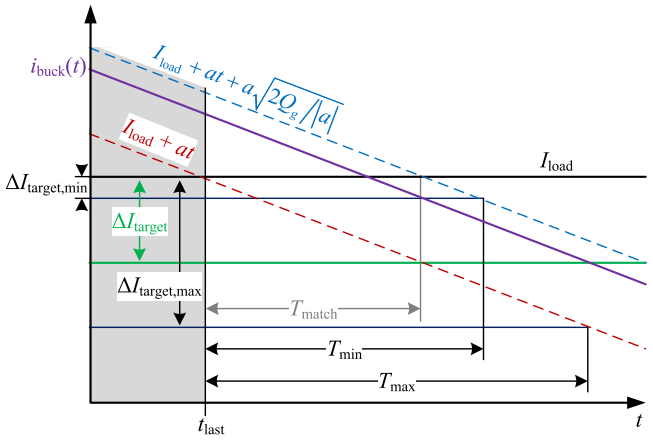

Fig. 10. Possible range of the buck inductor current around the T_{preset} instance.

value since less error in the inductor current is accumulated by the following switching action. The ideal case would be at the point that the inductor current is beyond the load value by $\Delta I_{\text{ripple}}/2$, then, the steady-state current is already within the target margins within the first switching action. Since this case cannot be guaranteed by voltage sensing alone, it is essential to map the range of the possible error in the current with respect to the preset halt time.

Fig. 10 shows a zoomed-in view to the preset instance, describing i_{buck} within two worst-case scenarios. The time index t_{last} indicates the instance of the last trigger event of the auxiliary circuit. The lower boundary of the inductor current is characterized as the condition when the inductor current reached the load current at t_{last}, given by

$$i_{\text{buck,min}}\left(t_{\text{last}}+t\right) = I_{\text{load}} + at \tag{11}$$

where a is the slope of the buck inductor current during the transient, given by

$$\begin{aligned} a &= -V_{\text{out}}/L, && \text{unloading} \\ a &= (V_{\text{in}} - V_{\text{out}})/L, && \text{loading.} \end{aligned} \tag{12}$$

The upper boundary of the inductor current is due to an additional charge injection by the auxiliary circuit Q_g at the instance of t_{last}, given by

$$i_{\text{buck,max}}\left(t_{\text{last}}+t\right) = I_{\text{load}} - a\sqrt{\frac{2Q_g}{|a|}} + at. \tag{13}$$

Equating (13) to I_{load} and solving for t yields the necessary condition to assure that the worst-case inductor current has reached the load current, that is,

$$T_{\text{match}} = \sqrt{2Q_g/|a|} \tag{14}$$

namely, the auxiliary circuit has completed its operation for the particular transient mode.

To further reduce the error of the inductor current to the allowed range of $\{\Delta I_{\text{target,max}}, \Delta I_{\text{target,min}}\}$, a target time range for return to the steady state is specified, as shown in Fig. 10. Equating (11) to the lower current boundary and (13) to the upper one yields the margin criterion, T_{min} and T_{max}, for T_{preset} as

$$\begin{aligned} T_{\text{min}} &= \Delta I_{\text{target,min}}/|a| + \sqrt{2Q_g/|a|} \\ T_{\text{max}} &= \Delta I_{\text{target,max}}/|a|. \end{aligned} \tag{15}$$

It should be noted that it is required to assure that the defined T_{preset} satisfies the conditions in (15) and the minimum time condition in (14), that is,

$$\max\left(T_{\text{min}}, T_{\text{match}}\right) \le T_{\text{preset}} \le T_{\text{max}}. \tag{16}$$

Furthermore, to avoid dependence of T_{preset} on the converter parameters and present dependence on the design considerations alone, (14) and (15) can be reorganized as:

$$\begin{aligned} T_{\text{min}} &= \frac{\Delta I_{\text{target,min}}\,(1-D)}{K I_{\text{nom}} f_s} + \sqrt{\frac{\Delta I_{\text{max}}}{K I_{\text{nom}} f_s f_g}} \\ T_{\text{max}} &= \Delta I_{\text{target,max}}\,(1-D)/K I_{\text{nom}} f_s \\ T_{\text{match}} &= \sqrt{\Delta I_{\text{max}}/K I_{\text{nom}} f_s f_g} \end{aligned} \tag{17}$$

where f_s is main converter switching frequency and f_g is the GRSCC maximal frequency, I_{nom} is the nominal load current at steady state, and $K = \Delta I_{\text{ripple}}/I_{\text{nom}}$ is the proportionality factor between the ripple and nominal currents. The criterion for a loading event can be extracted in a similar manner.

D. Auxiliary Capacitor Voltage Reset

The amount of energy that is processed by the auxiliary circuit during a transient event depends on the conversion ratio of the buck converter. In this study of a 12- to 1.5-V converter, during an unloading transient more charge is processed by the auxiliary circuit than during a loading transient of a similar magnitude. To maintain the ability to sink or source sufficient current from the output capacitor, prevent C_{aux} from overcharging and restore excess energy; a reset procedure for the independent auxiliary capacitor is essential.

A key consideration in the design of the reset procedure is to avoid interference with the desired steady-state operation of the main converter, i.e., the reset procedure will not cause a significant change of the output voltage. This implies that the auxiliary circuit reset current has to sink or source sufficiently small amount of charge per pulse and to be distributed over a longer period of time compared to the total load transient time. To this end, in this study, one of the three GRSCC modules is further employed during the steady-state phase to balance the auxiliary charge and reset the capacitor voltage back to its target value. Since the output voltage is well-regulated by the steady-state controller, the module is allowed to operate as a classical open-loop resonant-switched-capacitor converter, forcing the auxiliary capacitor to converge to $2V_{\text{out}}$, without any additional sensors. To limit the average current injected by the module during the reset phase, the effective operating frequency can be reduced by additional time delay between RSCC cycles [46].

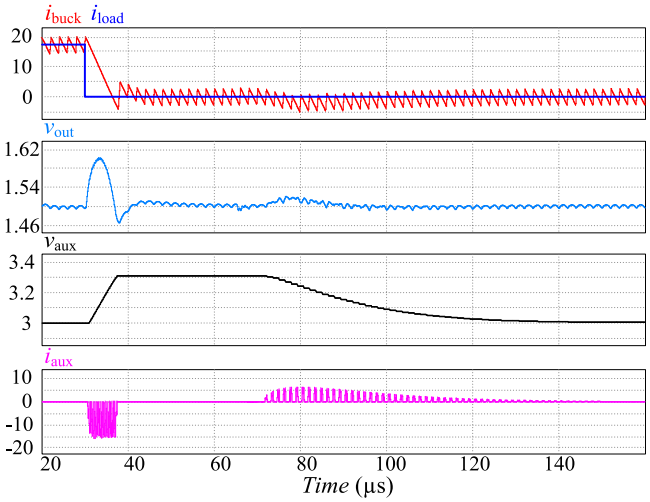

Fig. 11. Simulated unloading transient followed by a reset of $v_{\rm aux}$ back to $2V_{\rm out}$.

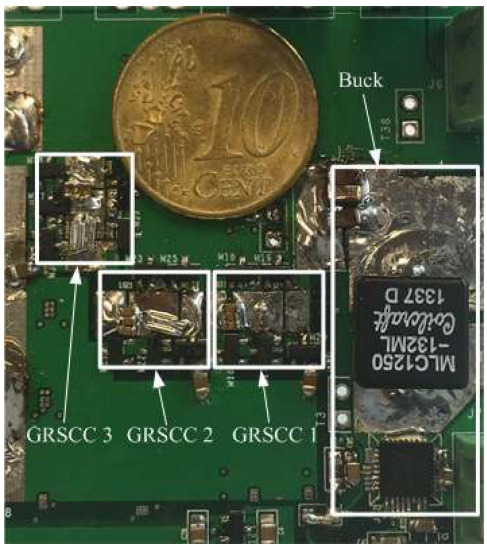

Fig. 12. Photograph of the hybrid-VRM power stage, including the buck converter and three interleaved GRSCCs.

Fig. 11 can be used to demonstrate the reset procedure. It shows an unloading transient that causes $v_{\rm aux}$ to rise due to the current sinking operation. It is then followed by a reset performed using one GRSCC module operating as a RSCC at lower effective frequency which restores $v_{\rm aux}$ back to the target value of $2V_{\rm out}$. It can also be observed that the voltage-mode control law maintains $v_{\rm out}$ within its steady-state margins.

VI. Experimental Verification

In order to validate the operation of the hybrid-VRM, a 20-W 12- to 1.5-V prototype was built and tested, with a measured peak efficiency of 93%. The auxiliary circuit was realized by three interleaved GRSCCs, sharing the same input, output, and control, as described in Section IV. A photograph of the experimental prototype is shown in Fig. 12. Table I lists the component values and parameters of the experimental prototype. A standalone efficiency measurement of the GRSCCs, i.e., without the main converter active, for various Vaux values is given in Fig. 13. The digital controller comprises steady-state voltage-mode control and transient-mode control, realized on an Altera Cyclone IV FPGA [47]. The steady-state control is assisted by high-performance integrated analog-to-digital converter (ADC) and digital pulse width modulation (DPWM) on-FPGA realizations as described in [45]. The load transient signals were generated by an external signal generator, independently, without synchronization to the controller.

TABLE I
Experimental Prototype Values

Component	Value
Input voltage $V_{\rm in}$	12 V
Output voltage $V_{\rm out}$	1.5 V
Main inductor L	1.3 μH
Output capacitor $C_{\rm out}$	150 μF
Buck converter switching freq. f_s	500 kHz
GRSCC maximal switching freq. f_g	∼1.7 MHz
Auxiliary capacitor $C_{\rm aux}$	20 μF
GRSCCs resonant tank capacitor C_g	0.3 μF
GRSCCs resonant tank inductor L_g	∼10 nH (stray inductance)
Number of GRSCC stages	3

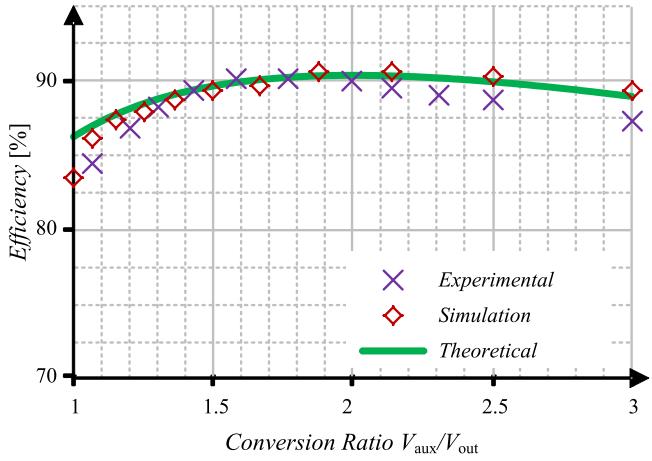

Fig. 13. Efficiency measurement of the GRSCCs.

Fig. 14 presents the hybrid-VRM response to loading and unloading transient events of 10 A in comparison to the buck converter operating under TOC, using the same transient detection circuit. Fig. 14(a) and (b) shows the response to a loading transient event of 10 A (1.5 to 11.5 A) for the hybrid-VRM and for TOC, respectively. The measured output voltage undershoot and total transient time for the hybrid-VRM are 60 mV and 3 μs and for the TOC case they are 120 mV and 9 μs, respectively. An unloading transient of 10 A (11.5 to 1.5 A) is depicted in Fig. 14(c) and (d). For this case, the hybrid-VRM's response results in output voltage overshoot of 100 mV with settling time of 12 μs, and using TOC, the voltage overshoot sums to be 390 mV with 21 μs settling time.

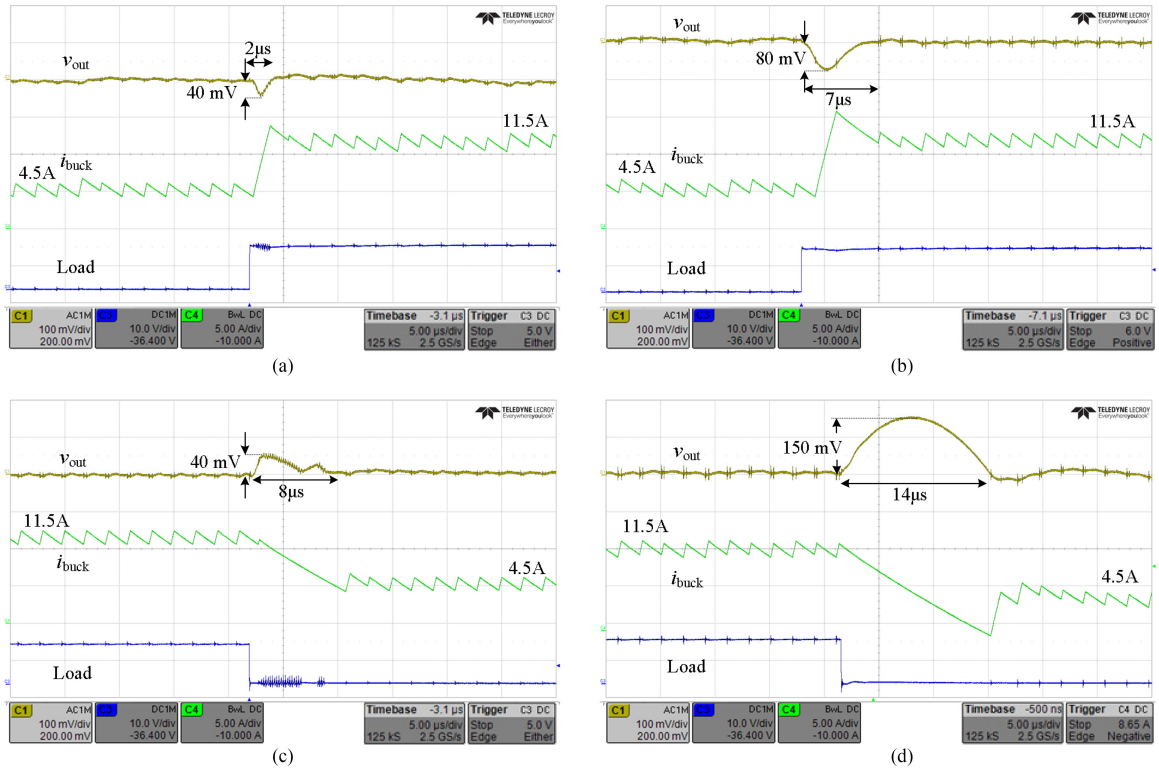

Fig. 14. Experimental results showing a 10-A load transient response of the [(a), (c)] hybrid-VRM versus [(b),(d)] TOC. Signals from top to bottom: $V_{\rm out}$[(a), (b): 100 mV/div.; (c), (d): 200 mV/div, ac coupled], $i_{\rm buck}$ ibuck (5A/div), and load-step signal. Time scale is $5\mu{\rm s/div}$. (a), (b) 1.5–11.5-A loading event. (c), (d) 11.5–1.5-A unloading event.

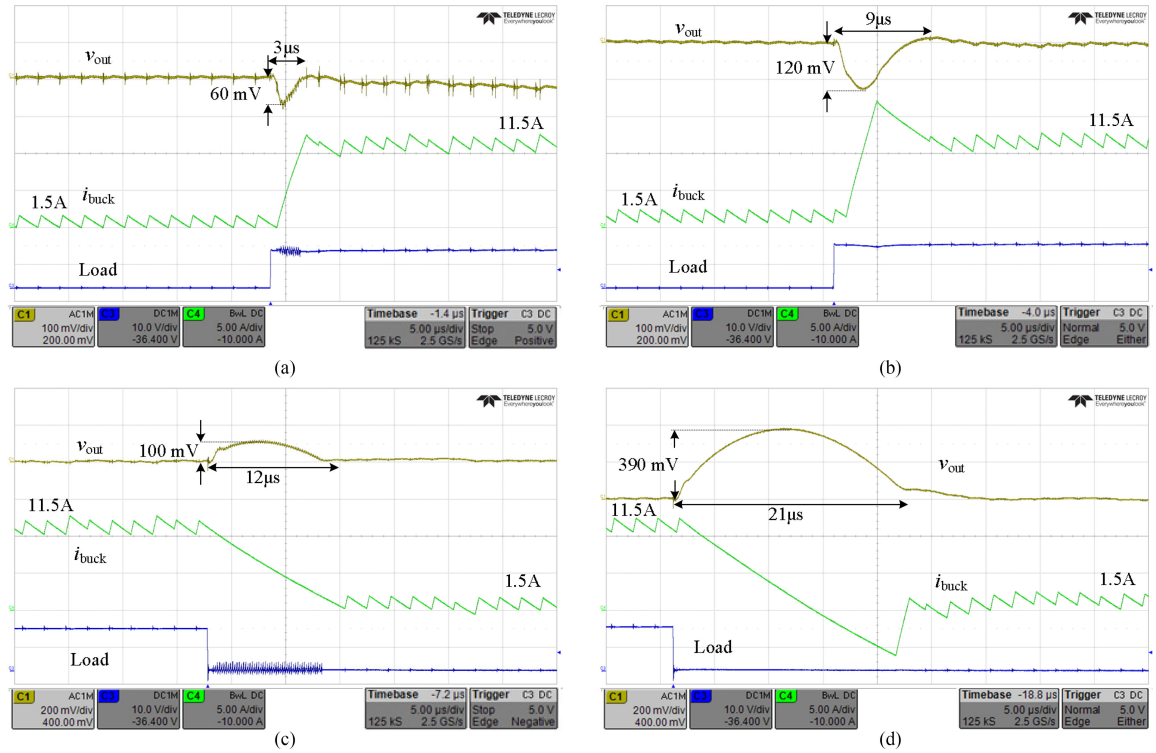

Fig. 15. Experimental results showing a 7-A load transient response of the [(a), (c)] hybrid-VRM versus [(b), (d)] TOC. Signals from top to bottom: $V_{\rm out}$ (100 mV/div, ac coupled), $i_{\rm buck}$ (5A/div), and load-step signal. Time scale is 5µs/div. (a), (b) 4.5–11.5-A loading event. (c), (d) 11.5–4.5-A unloading event.

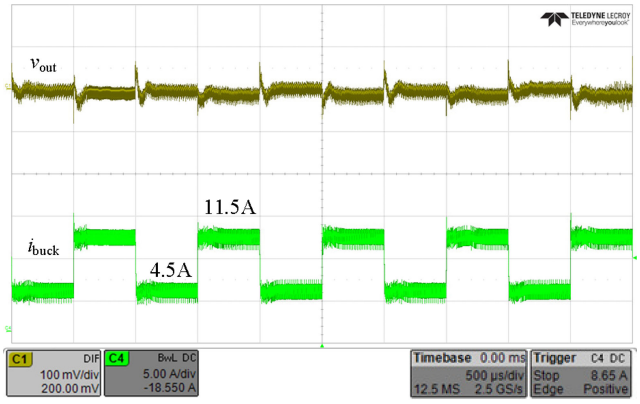

Fig. 16. Screenshot demonstrating the hybrid-VRM's response to a repetitive 1-KHz loading–unloading transients from 4.5 to 11.5 A. Output capacitor voltage 100 mV/div, inductor current 5 A/div, and time scale 500µs/div.

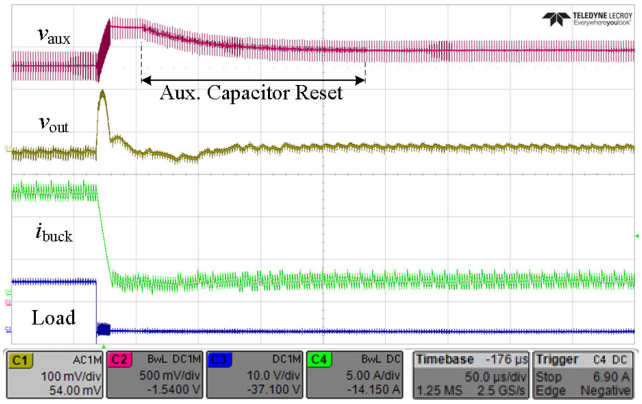

Fig. 17. Experimental results showing the auxiliary capacitor voltage reset procedure that follows an unloading transient. Signals from top to bottom: $v_{\rm aux}$ (500 mv/div), $v_{\rm out}$ (100 mV/div, ac coupled) $i_{\rm buck}$ (5 A/div), and load-step signal. Time scale is 50 µs/div.

Fig. 15 presents the comparison between the hybrid-VRM and TOC for loading and unloading transients, smaller than the rated $\Delta I_{\rm max}$(4.5 to 11.5 A). In the hybrid-VRM case of an unloading transient response [see Fig. 15(c)], the GRSCCs are halted and then retriggered in a similar manner to the analysis and simulation (see Fig. 8). This occurs as the GRSCCs are set to sink current of more than half the load-step magnitude.

Fig. 16 shows the hybrid-VRM's response to a repetitive load transients of 7 A (4.5 to 11.5 A) at a frequency of 1 KHz with 50% load duty ratio. As can be observed, the output voltage overshoots and undershoots remain the same as in Fig. 14, validating the capability of the system to handle consecutive transients.

Fig. 17 shows the auxiliary capacitor voltage reset procedure, confirming its capability to balance the charge of the auxiliary capacitor without affecting the steady-state operation. It should be noted and can be seen that the charge-balance current is significantly lower than the magnitude of $i_{\rm aux}$ during the load transient. This ensures stable steady-state operation without false-triggering of additional load-transients.

A transient efficiency and power loss measurements for the hybrid-VRM and for the system with TOC have been conducted

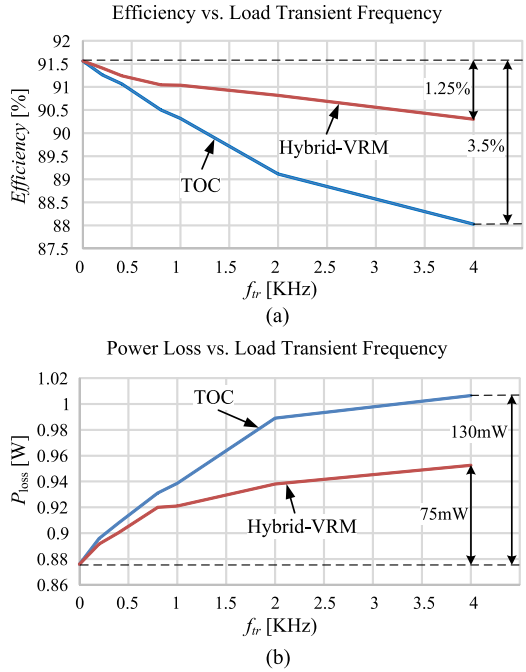

Fig. 18. Load transient efficiency and power loss measurements for TOC and the hybrid-VRM. (a) Efficiency measurement. (b) Power loss measurement. Load duty ratio is 50%.

and are presented in Fig. 18, with load duty ratio of 50%. As can be observed, due to the load transients the efficiency of the system decreases with the rise of the load transient rate, as analyzed in Section III. The efficiency of the system under TOC drops by up to 3.5% and the added power loss is up to 130 mW. With the hybrid-VRM, the efficiency drop is up to 1.25% and the added power loss is up to 75 mW. The transient efficiency and power loss results are in correlation to the results of [20], [26], and [33]. However, it should be noted that in this study, the power processing efficiency has improved compared to the TOC performance.

VII. Conclusion

A VRM with improved loading and unloading transient response has been presented. The improvement has been achieved by the addition of a load-side auxiliary circuit that comprises three interleaved converters, implemented using a recently presented GRSCC topology. This VRM has the potential to be space conserving and cost-effective when implemented into an IC design. The output capacitance is significantly reduced at the cost of small additional semiconductors and few capacitors, and does not require ferromagnetic elements.

The experimental results exemplify the performance of the design for both loading and unloading events, reducing output overshoots by up to 390% and transient time by up to 175% compared to TOC, without affecting the input side. In particular for the relatively high conversion ratio case, significant improvement has been demonstrated in the response to an unloading event, compensating for the moderate current slew-rate of the buck inductor.

The hybrid-VRM operates autonomously with reduced circuit complexity, i.e., no additional current-sense circuitry or pretransient information is required. In addition, since no complex mathematical estimations are needed, the complete FPGA implementation for the control (including the ADC and DPWM peripherals) sums less than 8000 logic elements, providing a cost-effective and simple controller solution.

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