Low-Frequency DC-Link Ripple Elimination in Power Converters With Reduced Capacitance by Multiresonant Direct Voltage Regulation

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***Abstract*—In this paper, a method for suppressing the low-frequency portion of dc-link ripple inevitably present in power conversion systems with reduced capacitance is proposed. The discussed active capacitance reduction circuitry (consisting of a feedback-controlled shunt-connected bidirectional buck-boost converter, terminated by a small auxiliary capacitance) directly regulates the dc-link voltage, utilizing a dual-loop control structure with parallel-connected multiresonant-bank-enhanced voltage loop stabilizing controller to achieve nearly constant, low-frequency-ripple-free steady-state dc-link voltage. Consequently, the proposed active capacitance reduction system may be perceived as a virtual infinite capacitor from the dc link point of view. The suggested circuitry is successfully applied to a single-phase commercial power factor correction front end in a nearly plug-and-play fashion. The control algorithm effectiveness is fully supported by simulations and experimental results.**

***Index Terms*—Bulk capacitance, dc-link ripple, grid-interfacing converters, resonant control.**

I. Introduction

POWER factor requirements of modern grid codes force the grid-connected converters to carefully shape the mains-side current [1], [2]. As a result, the instantaneous grid power typically contains pulsating, zero-average part in addition to dc component. Moreover, the system loads may draw instantaneous power with similar decomposition. The average power balance of the system is typically assured by driving the sum of the dc components to zero. On the other hand, pulsating components are typically different and uncontrolled. Consequently, a power-matching element (usually realized by a bulk dc-link capacitor) is required in order to preserve the instantaneous power balance [3] by driving the sum of pulsating components to zero. Unfortunately, the process of absorbing the sum of pulsating power by the bulk capacitance component creates the dc-link voltage ripple. The ripple, which is directly proportional to the conversion system rating and inversely proportional to the dc-link capacitance value, must retain within strictly predetermined limits in order to avoid violating both power converters' functionality and dc-link capacitor voltage rating. Subsequently, in applications rated higher than several tens of watts electrolytic capacitors are typically required. Consequently, the well-known reliability and physical size issues related to electrolytic capacitors [4]–[9] are directly transferred to the application.

In order to improve the both mentioned drawbacks, active solutions to capacitance reduction by dc-link ripple suppression were proposed in the literature as follows.

It was demonstrated in [10]–[14] that it is possible to achieve some reduction of the dc-link capacitance value by distorting the input current of the grid-connected converter without employing additional circuit components. As a result, the power factor is sacrificed, decreasing from unity to the minimal permitted limit. However, even though the approach does not require additional hardware, it is computational intensive. Moreover, injecting some amount of harmonic current into the grid may be unacceptable is some cases; thus, the approach cannot be considered universal.

The second group of active capacitance reduction methods utilizes the auxiliary power electronics-based circuits, allowing to maintain the dc-link voltage ripple within predetermined limits while reducing the capacitance utilized. The three subgroups may be identified as follows. In the first [15], [16], the dc-link capacitance is split into two small capacitors, connected via a bidirectional buck-boost converter, similarly to active equalization principle [17]. However, instead of equalizing the instantaneous capacitor voltages, only their dc values are kept equal while corresponding low-frequency ripples are forced to possess opposite polarities. As a result, no ripple appears across the dc link. In the second subgroup [18]–[24], a shunt-connected bidirectional power converter, terminated by a reduced-value auxiliary

Manuscript received May 26, 2016; revised July 21, 2016 and August 20, 2016; accepted September 1, 2016. Date of publication November 8, 2016; date of current version February 9, 2017.

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Digital Object Identifier 10.1109/TIE.2016.2626241

capacitance, replaces the bulk dc-link capacitance. The system operates as an active power filter, drawing the ripple portion of the dc-link current. The last subgroup of active solutions [25], [26] suggests utilizing circuitry similar to that of the second subgroup yet connected to the dc link in series. Consequently, it operates as a series voltage compensator, recompensing the ripple portion of the dc-link voltage. The idea behind the two last approaches is based on the fact that the amount of utilized bulk capacitance energy comprises only small fraction of the stored energy in dc-link capacitor. Consequently, significantly lower capacitance is sufficient to absorb the pulsating power component once its terminal voltage is released from the dc-link ripple constraints. The latter is accomplished by decoupling the power matching capacitor from the dc link by a bidirectional power converter. The shunt-connected ripple eliminator is believed to be the most general solution since it can be simply plugged into the dc bus to reduce voltage ripple and improve power quality [27].

Since shunt-connected solutions operate similarly to active power filters, they naturally resemble current sinks (from the dc link point of view). Therefore, the majority of related control algorithms operate as follows. Pulsating component is extracted from the measured dc-link current and utilized as current reference for the ripple eliminator. This may require measurements of several currents (equal to the amount of conversion stages, connected to the dc link) as well as physical access to measurement points. Recently, an alternative approach to controlling shunt-connected dc-link ripple eliminators was proposed [28]–[31]. Instead of focusing on the dc-link current, these methods perform direct dc-link voltage regulation. Thus, the ripple eliminator indirectly absorbs the pulsating current component without measuring the dc-link currents, i.e., dc-link voltage sensing is only required. Nevertheless, such a control scheme is nontrivial and challenging since the ripple eliminator may be perceived as an output-voltage regulated wide-input-range boost converter feeding a bidirectional power load as shown in [30]. There, a cascaded dual-loop control structure was shown to be able to stabilize the system while achieving the same peak-to-peak dc-link ripple as the original system utilizing the bulk dc-link capacitance. In [31], the control structure was further improved by adding the feed-forward (FF) and gain-scheduling (GS) actions obtained by partial feedback linearization, achieving 42% reduction of the dc-link ripple magnitude. This paper reveals that even though the main goal of the control system is regulating the dc link to a constant value, the disturbances (i.e., input voltage and output current) of the ripple eliminator are periodic rather than dc signals. This is why PID controllers utilized in [30] and [31] as loop compensators were unable to completely eliminate the dc-link ripple. Following internal model principle [32], in order to eliminate the steady-state error, the controller must possess infinite gain at frequencies, characterizing both reference and disturbance signals. As a solution, we propose enhancing the PID-type voltage controller by parallel-connected multiresonant bank, tuned to the major multiples of disturbance signal frequency (PID controller is still required to cope with the constant reference signal). Multiresonant controllers are usually utilized for tracking/disturbance rejection of periodic nonsinusoidal signals and has been successfully applied among

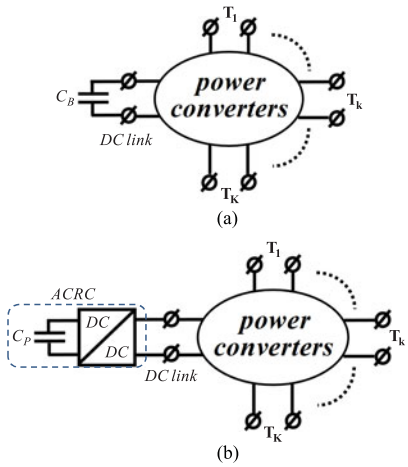

Fig. 1. Generalized power conversion system. (a) With bulk dc-link capacitor C_B. (b) With active capacitance reduction circuit (ACRC), $C_P << C_B$.

others to motor drives [33], dc–dc converters [34], uninterruptible power supplies [35], and distributed power generation systems [36]. The paper reveals that when resonant bank is utilized in the voltage controller only, further enhancements are unnecessary since they do not add noticeable performance improvement. Since the proposed solution is capable of eliminating the low-frequency portion of the dc-link ripple (obviously, switching frequency component would still be present), the proposed ripple eliminator may be perceived as an infinite virtual capacitor, connected to the dc link. In [28], the theoretical realization of a virtual infinite capacitor was proposed by means of sliding mode controller with switching frequency of 2 MHz and no experimental results were provided. Here, experimental circuitry utilizing 50 KHz switching frequency successfully validates the proposed method.

The rest of the paper is organized as follows. The generalized grid-connected power conversion system is analyzed in Section II to obtain a general expression for pulsating power element. The proposed method of dc-link capacitance reduction and ripple elimination is revealed in Section III. A case study of applying the proposed solution to a dc power supply with power factor correction (PFC) front end is demonstrated in Section IV, followed by the experimental validation shown in Section V. The paper is concluded in Section VI.

II. Generalized Power Conversion System With DC Link

Consider a generalized *K*-terminal power conversion system with dc link, as shown in Fig. 1(a) (one or more terminals may be directly connected to the dc link). Moreover, assume that each terminal T_k, $k = 1, \ldots, K$ is characterized by periodic yet nonsinusoidal behavior, given by

$$v_k(t) = V_{k0} + \sum_{n=1}^{\infty} V_{kn} \sin(n\omega_k t + \theta_{kn})$$
$$i_k(t) = I_{k0} + \sum_{n=1}^{\infty} I_{kn} \sin(n\omega_k t + \varphi_{kn}). \quad (1)$$

Thus, instantaneous power at each terminal is obtained as

$$p_k(t) = v_k(t)i_k(t) = P_k + \Delta p_k(t) \tag{2}$$

with P_k and Δp_k denoting average (dc) and pulsating (zero average) power components. In steady state, system power balance must sustain, i.e.,

$$\sum_{k=1}^{K} P_k = 0, \quad \sum_{k=1}^{K} \Delta p_k(t) + p_C(t) = 0 \tag{3}$$

must hold with $p_C(t)$ denoting the instantaneous power of the dc-link capacitor. The former condition is assured by a dedicated controller, regulating the average value of the dc-link voltage to a constant reference $V_{\rm dc}^*$, whereas the latter demonstrates the necessity of a power matching element (typically realized by a capacitor) since, in general,

$$\sum_{k=1}^{K} \Delta p_k(t) \neq 0. \tag{4}$$

Consequently, the steady-state dc-link voltage is given by

$$v_{\rm dc}^{ss}(t) \approx V_{\rm dc}^* + \frac{1}{C_B V_{\rm dc}^*} f_P(t) = V_{\rm dc}^* + \Delta v_{\rm dc}(t) \tag{5}$$

with

$$f_P(t) = \int_0^t \sum_{k=1}^{K} \Delta p_k(\tau) d\tau \tag{6}$$

and $\Delta v_{\rm dc}(t)$ denoting the instantaneous dc-link ripple. Since $f_P(t)$ depends on power system sources/loads and cannot be altered from the dc-link side, the value of dc-link capacitance is the only tunable parameter, influencing dc-link ripple magnitude. The latter is typically bounded by the system power converters' operational constraints as well as by the dc-link capacitor rated voltage value, implying utilizing electrolytic capacitors in systems rated above several tens of watts. Assuming dc-link ripple magnitude restrictions given by

$$v_{\rm dc}^{\rm MIN} < v_{\rm dc}^{\rm ss}(t) < v_{\rm dc}^{\rm MAX} \tag{7}$$

the required bulk dc-link capacitance value may be determined from

$$C_B = \frac{1}{V_{\rm dc}^*} \max\left(\frac{\max\limits_t f_P(t)}{\left(v_{\rm dc}^{\rm MAX} - V_{\rm dc}^*\right)}, \frac{\min\limits_t f_P(t)}{\left(v_{\rm dc}^{\rm MIN} - V_{\rm dc}^*\right)} \right). \tag{8}$$

III. Virtual Infinite Capacitance

It is interesting to note that letting

$$C_B \to \infty \tag{9}$$

in (5) yields

$$\Delta v_{\rm dc}(t) \to 0,\ v_{\rm dc}^{\rm ss}(t) \equiv V_{\rm dc}^* \tag{10}$$

which is obviously nonfeasible when utilizing a passive power matching element. ACRCs [Fig. 1(b)] allow physical decoupling of the power matching capacitor from the dc link, releasing its voltage from ripple constraints given by (7). This leads to significant reduction of the power matching capacitance, i.e., $C_P << C_B$ in Fig. 1(b). It is further shown that (10) may be achieved employing an ACRC by emulating infinite capacitance while utilizing a finite-value matching capacitor C_P, as shown in Fig. 2(a) (C_R is a small ceramic capacitor always present at dc-link side terminals of the ACRC to absorb switching ripple). Note that even though capacitor C_P operates as power matching element, its voltage ripple restrictions are much more relaxed than (7).

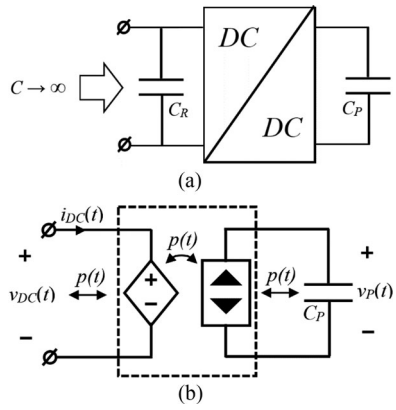

Fig. 2. Active realization of virtual infinite capacitance (C_R and C_P are finite). (a) Generalized topology. (b) Equivalent functionality.

In case $v_{\rm dc}$ is well regulated to $V_{\rm dc}^*$ by the ACRC, C_P absorbs the pulsating power component, as shown in Fig. 2(b), i.e., its steady-state voltage would be given by

$$v_P^{\rm ss}(t) \approx V_P^* + \frac{1}{C_P \left(V_P^*\right)^2} f_P(t) = V_P^* + \Delta v_P(t) \tag{11}$$

with V_P^* and $\Delta v_P(t)$ denoting constant reference value and instantaneous ripple of $v_P(t)$, respectively. It should be emphasized that magnitude constraints of $\Delta v_P(t)$ are related to the ACRC operational requirements as well as the rated voltage value of C_P while being independent on the rest of the system power converters' operational restrictions. Assuming

$$v_P^{\rm MIN} < v_P^{\rm ss}(t) < v_P^{\rm MAX} \tag{12}$$

the value of the auxiliary power matching capacitance is determined from

$$C_P = \frac{1}{V_P^*} \max\left(\frac{\max\limits_t f_P(t)}{v_P^{MAX} - V_P^*}, \frac{\min\limits_t f_P(t)}{v_P^{MIN} - V_P^*} \right) \tag{13}$$

and minimized by setting

$$V_P^* = \sqrt{\frac{1}{2}\left(\left(v_P^{MAX}\right)^2 + \left(v_P^{MIN}\right)^2\right)}. \tag{14}$$

It is interesting to note that the dc-link ripple is independent on the value of C_P and is governed by the regulation abilities of ACRC converter only. Hence, in case dc-link voltage controller is capable of satisfying (10), infinite capacitance is emulated by the system (from the dc link point of view) while actually utilizing the total capacitance of $C_R + C_P$.

The overall closed-loop control system is shown in Fig. 3, comprising reference input $V_{\rm dc}^*$ and disturbance inputs v_P and $i_{\rm dc}$ (the proposed controller is based on direct regulation method of the dc-link voltage; yet it may be easily modified to be utilized

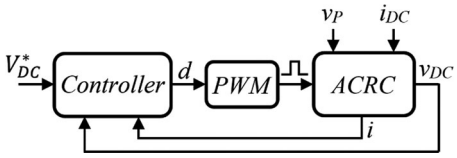

Fig. 3. Closed-loop system structure of an infinite virtual capacitor.

in classical active-power-filter-like ripple mitigation structures as well). As depicted, the controller might also utilize information regarding ACRC inductor or switch current i to generate the duty cycle input d to the pulse width modulation modulator. Once dc-link voltage is tightly regulated, the ACRC converter input voltage and output current are given in steady state by

$$v_P(t) = V_P^* \sqrt{1 + \frac{2}{C_P (V_P^*)^2} \int_0^t \sum_{k=1}^{K} \Delta p_k(\tau) d\tau} \tag{15}$$

and

$$i_{\rm dc}(t) = \frac{1}{V_{\rm dc}^*} \sum_{k=1}^{K} \Delta p_k(t) \tag{16}$$

respectively. While the reference is constant, disturbances are periodic yet nonsinusoidal, containing (in general) dc and frequency components at integer multiples of ω_k, $k = 1, \ldots, K$. According to internal model principle, in order to achieve the zero steady-state error, the loop gain magnitude must possess infinite gain at all the mentioned frequencies. Nevertheless, in reality only dc as well as several multiples of each base frequency are significant and should be treated. Consequently, the resulting loop gain must contain an integrator to cope with dc signals and several finite resonant banks (or repetitive controllers) to eliminate the dominant multiples of each ω_k. Then, near-zero steady-state error would be expected, i.e., dc-link voltage should be ripple free.

IV. Example

As an example, consider (for brevity and clarity) a unity-power-factor operating single-phase rectifier, driving a dc load. Hence

$$p_C(t) = P_L cos2\omega_1 t \tag{17}$$

with P_L and ω_1 symbolizing the load power and grid frequency, respectively [24]. In case bidirectional buck-boost ACRC converter ($v_P < v_{\rm dc}$) is utilized, power matching capacitance may ideally be reduced to

$$C_P = \frac{P_L}{\left(\sqrt{2}-1\right)\omega_1 (V_{\rm dc}^*)^2} \tag{18}$$

for $V_P^{\rm MIN} = 0, v_P^{\rm MAX} = V_{\rm dc}^*$. In reality, somewhat higher matching capacitance should be selected to allow safety margins and improve robustness against abrupt load changes [31]. Steady-state input voltage and output current of the ACRC are

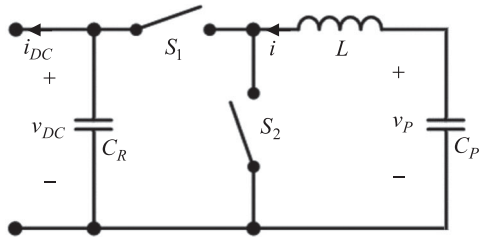

Fig. 4. Bidirectional buck-boost ACRC.

TABLE I
System Parameter Values

Parameter	Value	Units
Switching frequency, T_s^{-2}	50	kHz
ACRC inductance, L	320	μH
ACRC capacitance, C_P	22	μF
Total dc-link capacitance, C_R	9.4	μF
Grid frequency, ω_1	100π	rad/s
Reference voltage, T_P^*	271	V
Reference voltage, $V_{\rm dc}^*$	400	V
Rated load power, $P_{2,\rm MAX}$	360	W

then obtained as

$$v_P(t) = V_P^* \sqrt{1 + \frac{P_L}{C_P \omega_1 (V_P^*)^2} \sin 2\omega_1 t} \tag{19}$$

and

$$i_{\rm dc}(t) = \frac{P_L}{V_{\rm dc}^*} cos2\omega_1 t \tag{20}$$

respectively. Apparently, while ACRC output current is sinusoidal at double-grid frequency, its input voltage is periodic yet nonsinusoidal as expected. Consequently, in order to reject both disturbances, multiresonant (or repetitive) structure is required in dc-link voltage loop, tuned to multiples of $2\omega_1$.

Consider a buck-boost ACRC shown in Fig. 4 with related numerical data summarized in Table I. According to (18), C_P may be reduced down to 17 μF by setting $V_P^* = 400/\sqrt{2}V$. Nevertheless, 22 μF is utilized due to the reasons stated above and hence slightly lower V_P^* is selected.

ACRC large-signal dynamics (switching cycle averaged) is governed by

$$\begin{aligned} C_P \frac{dv_P}{dt} &= -i \\ L\frac{di}{dt} &= v_P - (1-d)\, v_{\rm dc} \\ C_R \frac{dv_{\rm dc}}{dt} &\approx \frac{v_P}{v_{\rm dc}} i - i_{\rm dc} \end{aligned} \tag{21}$$

with d denoting the duty cycle of the switch S_2 and complementary duty cycle of the switch S_1. In [30], dual-loop control structure shown in Fig. 5(a) was proposed to implement the direct dc-link voltage regulation as follows. The small-signal

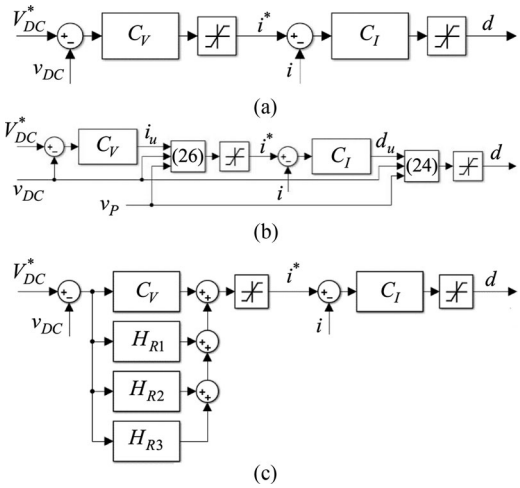

Fig. 5. ARCR control structures. (a) Basic dual loop. (b) Dual loop with partial feedback linearization. (c) Multiresonant.

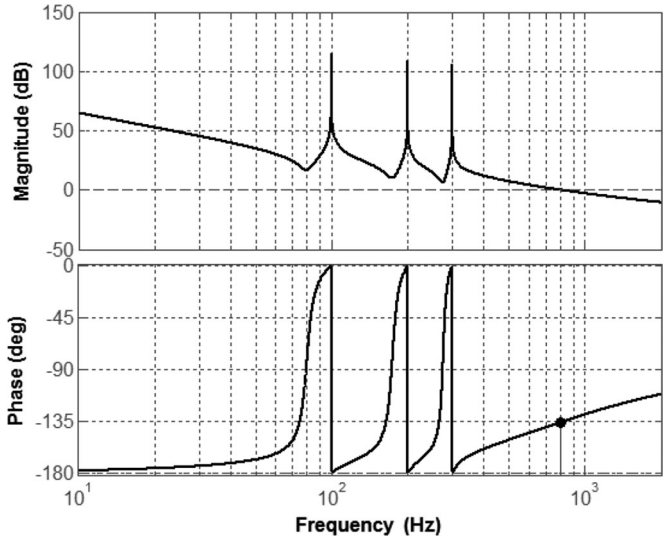

Fig. 6. Bode diagram of voltage loop gain. Crossover frequency and phase margin are ∼800 Hz and 45°, respectively.

inductor current may be obtained from (21) as

$$\tilde{i}(s) = \frac{C_P V_{\rm dc} s}{LC_P s^2 + 1}\left(\tilde{d}(s) - \frac{1-D}{V_{\rm dc}}\tilde{v}_{\rm dc}(s)\right) \tag{22}$$

with $V_{\rm dc}$ and D denoting dc operating point values of $v_{\rm dc}$ and d, respectively. In order to damp the resonance and reject the disturbance term of (22), PI controller $C_I = K_{\rm PI} + K_{\rm II}/s$ was utilized as the inner loop compensator. The controller was designed following [37], achieving ∼4-kHz bandwidth with 45° phase margin. Unfortunately, utilizing a PI controller as current loop compensator yields nonunity closed-loop gain, leading to steady-state current tracking error $e_i(t) = i^*(t) - i(t)$. It should be emphasized that since C_I is linear time invariant, i^*, I, and e_i possess similar frequency-domain distributions, i.e., e_i is periodic as well. Once the inner loop is closed around ACRC inductor current i, the small-signal dc-link voltage is given by

$$\tilde{v}_{\rm dc}(s) \approx \frac{C_P V_P s - I}{V_{\rm dc} C_P C_R s^2}\left(\tilde{i}^*(s) - \tilde{e}_i(s)\right) - \frac{1}{C_R s}\tilde{i}_{\rm dc}(s) \tag{23}$$

with V_P and I denoting the dc operating point values of v_P and i, respectively. Once $e_i(t)$ is nonzero, it appears as an additional disturbance in (23). Note that I is positive when the ACRC is discharging and negative when charging. Therefore, (23) possesses negative gain with unstable zero when $I > 0$ and positive gain with stable zero when $I < 0$. An outer loop stabilizing controller $C_V = K_{\rm PV} + K_{\rm IV}/s$ was designed, utilizing one-fifth of the current loop bandwidth (refer to [30] and [31] for further voltage controller design details). However, time-varying behavior of v_P, i, and e_i cannot be fully contradicted by a linear time-invariant voltage controller. Eventually, the proposed system was capable of achieving dc-link ripple of 12 Vpp when operating under rated load. In order to enhance the performance, partial feedback linearization via GS and FF actions was applied to the basic dual-loop control structure in [31] [cf., Fig. 5(b)] as follows. In the current loop, the duty cycle was formed by

$$d = \frac{1}{v_{\rm dc}}\left(d_u - v_P + v_{\rm dc}\right) \tag{24}$$

where d_u denotes the output of C_I. This gives

$$i(s) = \frac{1}{Ls} d_u(s) \tag{25}$$

and hence utilizing C_I above as current loop compensator results in unity dc gain of the closed loop, significantly reducing the steady-state current tracking error e_i. In the voltage loop, the reference current was constructed as

$$i^* = \frac{v_{\rm dc}}{v_P} i_u^* \tag{26}$$

where i_u^* denotes the output of C_V. This gives

$$\tilde{v}_{\rm dc}(s) \approx \frac{1}{C_R s}\left(\tilde{i}^* - \tilde{e}_i - \tilde{i}_{\rm dc}\right) \tag{27}$$

and hence utilizing C_V above as voltage loop compensator results in unity dc gain of the closed loop as well. Consequently, the dc-link ripple was reduced to 7 Vpp (∼42% improvement) under rated load operation. Obviously, dc ripple could not be completely eliminated due to finite loop gain at disturbance frequencies (multiples of $2\omega_1$). Here, we utilize the same basic dual-loop structure with C_V and C_I as in [35] without partial feedback linearization. Instead, the voltage controller C_V is coupled with parallel triple-resonant bank given by

$$H_{Rk}(s) = \frac{\alpha s}{s^2 + \beta s + (2k\omega_1)^2},\ k = 1 \ldots 3 \tag{28}$$

as shown in Fig. 5(c), without modifying the rest of the control structure, thus forcing the loop gain to possess very high gain at first three multiples of $2\omega_1$ in addition to dc. As mentioned above, this allows both nearly perfect tracking and disturbance rejection at mentioned frequencies according to internal model principle. Nominal voltage loop gain is shown in Fig. 6 (respective controller parameters are summarized in Table II). As predicted, the loop gain possesses infinite gain at dc and the first three multiples of 100 Hz.

TABLE II
CONTROLLER PARAMETER VALUES

Parameter	Value
K_{PI}	0.047
K_{II}	701
K_{PV}	0.03
K_{IV}	105
α	50
β	0.1

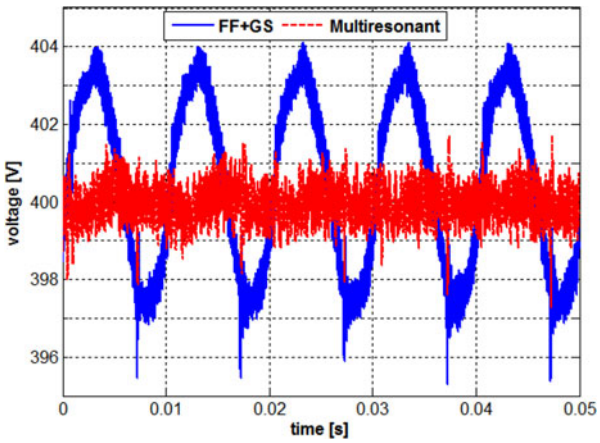

Fig. 7. Simulation results. Steady-state dc-link voltage behavior utilizing dual-loop control structures with partial feedback linearization (FF + GS) and multiresonant structures under rated load.

It should be noted that once tightly regulated, the dc-link voltage does not reflect the system power balance anymore. Hence, $v_P(t)$ must be fed back to the voltage controller of the unity-power-factor operating single-phase rectifier in order to maintain the correct operation of the latter (refer to [30] and [31] for more details).

Simulated steady-state dc-link voltage behaviors of the two nonbasic dual-loop control structures are compared in Fig. 7 for the system operating under rated load. Apparently, dual-loop PI controller-based structure with partial feedback linearization is incapable of eliminating the steady-state error at nonzero frequencies, whereas dual-loop PI controller-based structure with resonant-bank-enhanced voltage controller successfully copes with the task as expected, even though its current loop possesses steady-state error, as shown in Fig. 8. This is due to the infinite loop gain at dc and multiples of double-base frequency (cf., Fig. 6), where the disturbances (including steady-state current error) possess the majority of energy content.

It is interesting to note that three enhanced control arrangements were further examined as follows. In the first scheme, the FF term (24) was added to the current loop of the dual-loop PI controller-based structure with resonant-bank-enhanced voltage controller. In the second, the current controller C_I was coupled with a parallel triple-resonant bank similar to that of the voltage loop. In the third arrangement, the control structures of Fig. 5(b) and (c) were merged to include both partial feedback linearization and resonant banks in both current and

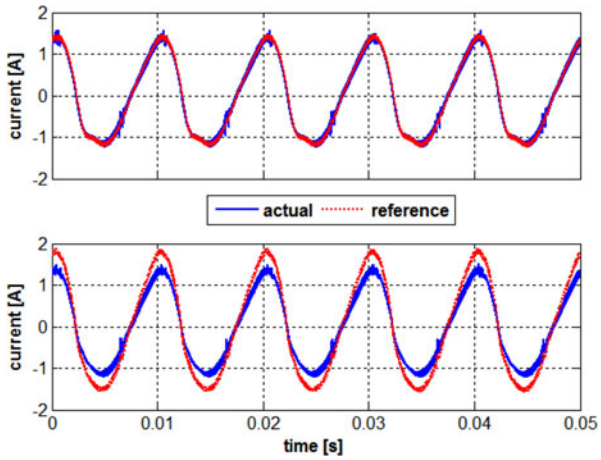

Fig. 8. Simulation results. Steady-state ACRC current tracking behavior: top—partial feedback linearization; bottom—multiresonant.

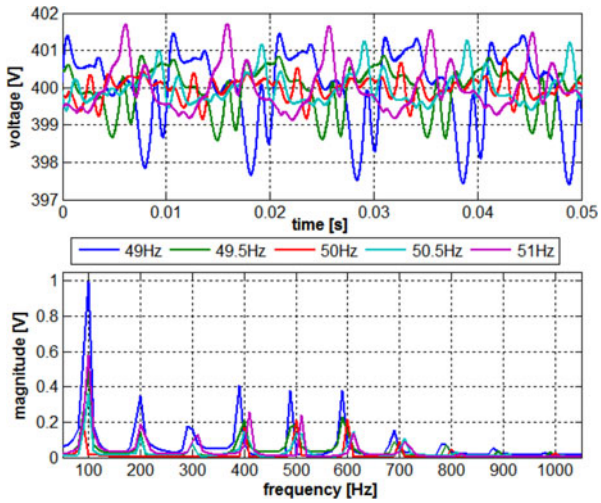

Fig. 9. Simulation results. Frequency deviation impact on dc-link ripple.

voltage loop. Nevertheless, even though current tracking error was driven to zero in all enhanced arrangements, noticeable improvement of the dc-link voltage behavior was hardly evident. Consequently, including the proposed resonant structure in the voltage loop only is sufficient and no further enhancement is required to eliminate the low-frequency dc-link ripple.

Additional important point is that while resonant bank is tuned to multiples of 100 Hz, grid frequency seldom remains constant. Fig. 9 presents time and frequency-domain dc-link ripple behavior (without switching component for facilitation) upon grid frequency residing within 50 ± 1 Hz range. Apparently, frequency deviation has insignificant impact on the performance due to the relatively high gain around the resonant frequencies (cf., Fig. 6).

V. EXPERIMENTAL VERIFICATION

In order to validate the proposed control system, Texas Instruments UCC28180EVM-573 360[W] power factor correction front-end evaluation board, as shown in Fig. 10 [38], was utilized

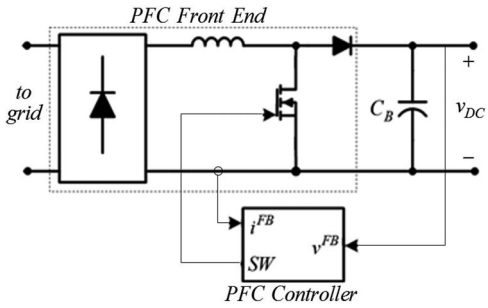

Fig. 10. Texas Instruments UCC28180EVM-573 structure.

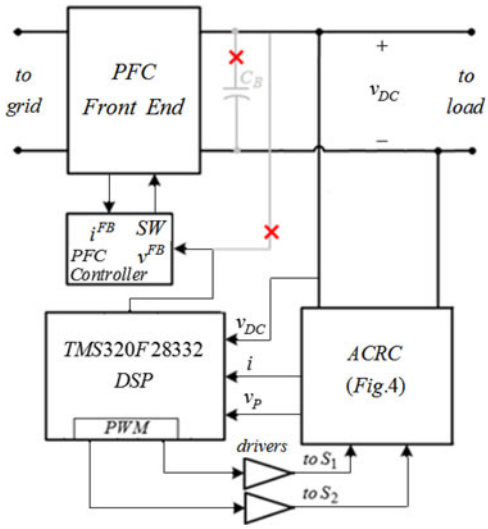

Fig. 11. Combined PFC + ACRC system interconnections.

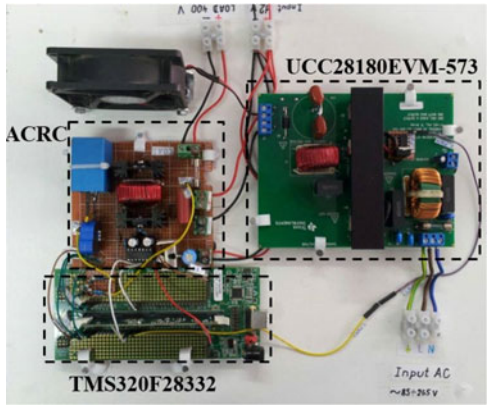

Fig. 12. Experimental setup.

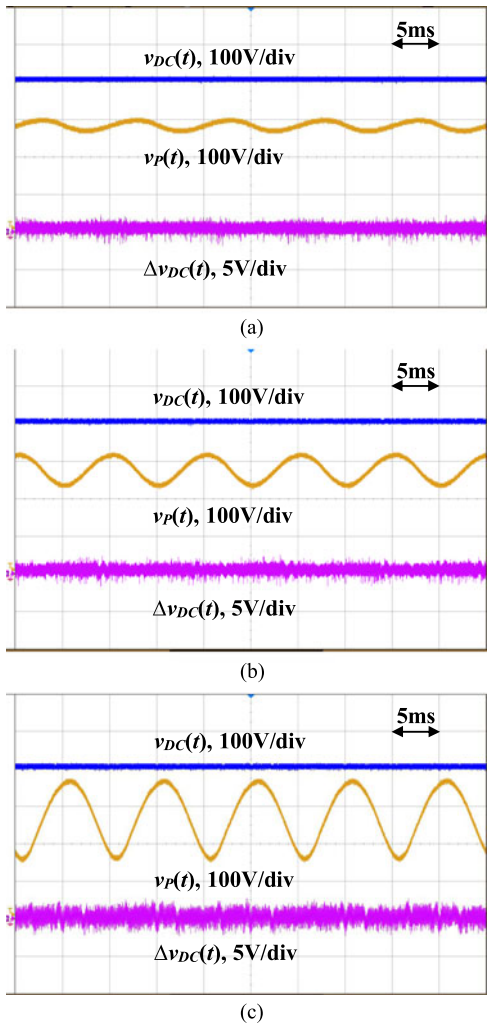

Fig. 13. Experimental results. Steady-state performance of the proposed system for the following load levels. (a) 50 W. (b) 150 W. (c) 350 W.

as a unity-power-factor operating single-phase rectifier, terminated by a bulk dc-link electrolytic capacitor $C_B = 270\ [\mu F]$. The ACRC converter (cf., Fig. 4) was built according to the parameters in Table I, with switches S_1 and S_2 realized by Infineon 20N60C3 MOSFETs. During experiments, the voltage feedback path to the PFC controller and the electrolytic capacitor C_B was disconnected. TMS320F28332 digital signal processor was utilized to both control the ACRC and manipulate the voltage feedback to the power factor correction front end, as shown in Fig. 11. An interested reader is referred to [30] for further details on the experimental setup (cf., Fig. 12) and [31] for details on PFC controller feedback voltage manipulation.

Experimental results of the proposed multiresonant controller-based system steady-state operation are shown in Fig. 13 for different load levels. Apparently, the dc-link voltage $v_{\rm dc}(t)$ remains tightly regulated, while the ripple $\Delta v_{\rm dc}(t)$ is dominated by switching ripple component at all time. The voltage $v_P(t)$ across the power matching capacitor C_P reflects the absorbed pulsating power component according to (19).

Fig. 14 compares the dc-link time and frequency-domain voltage behaviors of the partial feedback linearizing controller proposed in [31] and of the multiresonant one suggested here. As shown by the magnitudes of dc-link voltage ripple Fourier transforms $\mathrm{FFT}(\Delta v_{\rm dc})$, while the ripple harmonic content of the former method is dominated by the first three double-grid-frequency harmonics, multiresonant bank flattens the frequency response peaks, as expected.

It is known that one of the main drawbacks of active ripple eliminators with reduced capacitance is the reduced hold-up

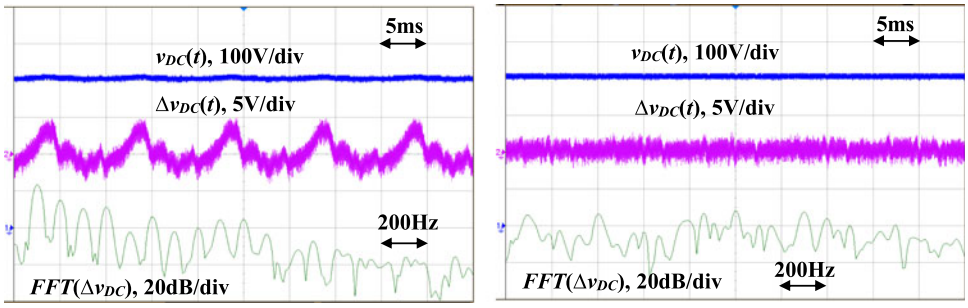

Fig. 14. Experimental results. Steady performance time and frequency-domain behavior comparison of dual-loop control structures with partial feedback linearization (left) and multiresonant-bank-enhanced voltage controller (right) for rated load operation.

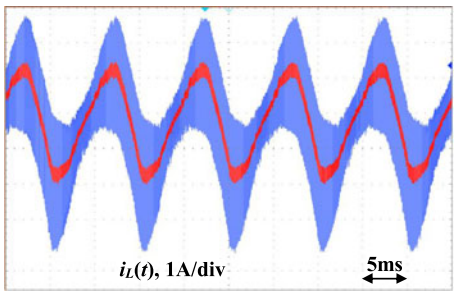

Fig. 15. Experimental results. ACRC inductor current for rated load operation.

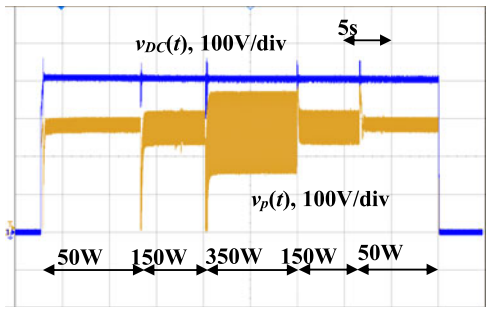

Fig. 16. Experimental results. Transient performance of the proposed system under load power variations.

ability, converted into poor transients handling. Moreover, since auxiliary capacitance voltage pulsates between the two distant extremes, in case the load increases when $v_P(t)$ is close to zero, dc-link voltage may collapse. The value of the auxiliary capacitance is hence selected higher than that dictated by (18) to keep $v_P(t)$ well above zero at all time. The ACRC inductor current for rated load operation is shown in Fig. 15 (switching-ripple-free waveform is also shown), matching well the simulated waveform of Fig. 8.

Dynamic response of dc link and auxiliary capacitance voltages to load steps is shown in Fig. 16. As expected, upon sudden load increase, the energy stored in the auxiliary capacitance is insufficient to compensate the load and hence its voltage drops toward zero. At the same time, dc-link voltage reduces too since the small dc-link capacitor supplies part of the load energy. Once the PFC voltage loop responds, both dc link and auxiliary capacitance voltages are restored back to their corresponding steady-state values. On the other hand, upon sudden load decrease, auxiliary capacitance absorbs the excessive energy supplied by the PFC and its voltage rises. Once the overvoltage protection embedded into the PFC is tripped, its output is forced to reduce and the system returns to the normal operation. Apparently, transient handling is somewhat problematic and will be investigated for possible solutions in future works.

VI. Conclusion

In this paper, a control algorithm allowing to achieve complete elimination of the low-frequency dc-link ripple in power electronics based energy conversion systems was proposed. Ripple suppression was accomplished by diverting the corresponding spectrum of the pulsating power component, usually causing the mentioned ripple, to a small auxiliary capacitor via shunt-connected bidirectional dc–dc converter. The proposed algorithm was based on a dual-loop control structure, in which the voltage loop stabilizing compensator was combined with a parallel-connected bank of resonant controllers, tuned to major multiples of pulsating power component base frequencies. Complete elimination of the dc-link ripple was shown to be equivalent to connecting an infinite bulk capacitor across the dc-link terminals. Simulations and experimental results of applying the proposed method to an off-the-shelf PFC front end validated well the findings presented in this paper.

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