High-Efficiency Nonisolated Converter With Very High Step-Down Conversion Ratio

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***Abstract*—This paper introduces a new nonisolated converter topology with very high step-down conversion ratio and high efficiency for high current low voltage point-of-load voltage regulator modules. Compared to a conventional two-phase buck converter, the new converter triples the effective duty-ratio and lowers the voltage stress of the transistors, significantly reducing the overall volume of the converter while maintaining high efficiency. The new converter is capable of delivering high current to the output by two interleaved phases and further features an inherent current sharing to balance the load between the phases. The use of lower voltage stress transistors allows operation at high switching frequencies that translates into fast dynamic response to load perturbations. The operation of the topology is verified on a 30 W, 48 V-to-1 V prototype, demonstrating peak efficiency of 91.5% and above 88% for most of the load range.**

***Index Terms*—High conversion ratio, point-of-load converter, voltage regulator module.**

I. Introduction

In the recent years, with the proliferation of cloud computing, power consumption of datacenters has grown significantly [1]. Datacenters typically use a large number of CPUs, each requires a well-regulated dc voltage that is provided by a voltage regulator module (VRM) as the back-end converter. This is done to satisfy the power quality for the load and in particular to assure a tightly regulated supply under rapid and consecutive load transients. In the majority of applications, since the power source is an unregulated 48 V dc, the power processing chain in datacenters is constructed as a two-stage converter architecture. The first stage is a 48 V-to-12 V converter to provide the 12 V bus and the second is a 12 V-to-1.x V point-of-load (PoL) converter. The two-stage architecture has been widely used in the last 20 years, and due to the massive increase in power consumption of datacenters, improving the efficiency of the power delivery architectures has been assigned as a primary objective [2]–[4].

One of the popular solutions for a two-stage conversion from 48 V-to-1.x V is by cascading two converters [5]. Since each of the stages has different objectives, they are designed accordingly. To achieve fast dynamic response required by the CPU and to shrink to components size, the 12 V-to-1.x V PoL buck converter operates at relatively high switching frequency, whereas the objective of the 48 V-to-12 V converter is mainly to maintain high efficiency. Typically, the 12 V-to-1.x V converter comprises multiphase interleaved buck converters, to be able to deliver the high current (few tens of amps) to the CPU and to reduce the output filter volume while maintaining good efficiency over wide load range [6], [7]. However, although each of the two-stages is over 90% efficient, the overall 48 V-to-1.x V conversion efficiency is less than 85% [5], [8]. Aside of the power losses in each of the converters, one of the contributors that lowers the efficiency is the 12 V power delivery bus that produces high conduction losses [8].

For some time now, due to both conservative reasons and implementation issues, a single-stage PoL solutions that apply direct 48 V-to-1.x V conversion have been avoided. However, with the advancement in semiconductor power devices and control algorithms, some solutions have the potential of being more efficient overall when compared to the two-stage architecture. The main reason for this is the conduction losses on the 48 V power bus are significantly lower (for the same power level), up to 16 times, than on a 12 V one. As a result, the direct 48 V-to-1.x V conversion has another advantage of further reducing the volume of the overall system by trimming down the conductors of the 12 V bus.

Very high conversion ratio converters have been investigated in previous years [9]–[30], where in most solutions transformers are used to handle the high voltage conversion ratio. To accommodate the size and cost, these solutions are typically rated for higher power and designed to supply few processors cores. In addition, they typically lack the ability of producing the fast dynamic response to load changes, making them less attractive for VRM applications as a single-stage. The nonisolated high conversion ratio solutions that have been reported in recent years can be divided into two groups. The first group is of enhanced performance buck converter that has been enabled by the advancement of semiconductor technology and the introduction of Gallium Nitride (GaN) power devices [31]. Therefore, the narrow on time that is required (1/48 T_s, neglecting losses) is achieved by fast switching transistors. However, the efficiency of the converter does not pass the mid-80%. Another problem is that an extremely high resolution duty-ratio generator is required to facilitate accurate regulation. The second group of the direct conversion solutions is topology extension of combined-merged converters that employ flying capacitors to lower the effective conversion ratio, enabling multilevel multiphase capabilities to the converter which translates to lower stresses, higher efficiency, and wider dynamic range. Among these topologies

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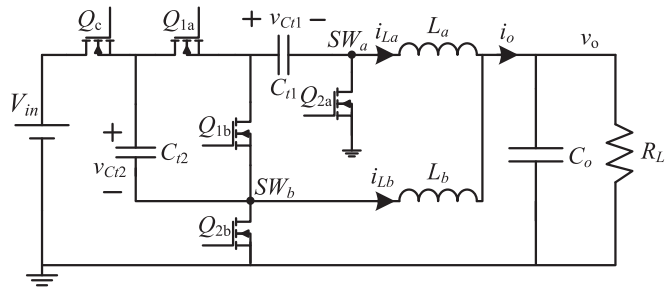


Fig. 1. Double series-capacitor buck converter (DSCBC) topology.

are the multiphase buck converters with extended duty cycle and their derivations [13]–[23], which one of the derivations is also known as the series-capacitor buck converter [22], multilevel buck converters [24]–[28], 7-switch flying capacitor multilevel buck converter [29], and variations of the Ćuk converter [30]. These converters perform better than a buck converter in terms of efficiency since their effective duty ratio is extended and the transistors voltage stress is reduced [22]. Naturally, any of the variation can be further enhanced with GaN power devices. It should be noted that, to the authors' knowledge, thus far, none of the extended duty-ratio converters has been detailed for a 48 V-to-1.x V applications.

Within the wide variety of the nonisolated solutions, the series-capacitor buck converter stands out as an attractive solution due to various features. From the load side, it operates similarly to a two-phase interleaved buck converter that can produces extremely fast dynamic response to load changes [32], [33] and also has the same component count except for one capacitor, yet has half of the voltage stress on three out of the four transistors. It operates at a doubled duty ratio compared to a buck converter and the series capacitor, along with the symmetrical operation, provides natural current sharing between the phases [34]. On the other hand, at high conversion ratios the low-side transistors still need to handle both high rms current and the voltage stress that is not negligible. In addition, the doubling feature of the duty ratio may still be tight for regulation in very high conversion ratio applications.

The objective of this study is to introduce a new nonisolated topology for very high conversion ratio applications with high efficiency. The new topology, depicted in Fig. 1, *effectively triples the duty ratio, lowers and better distributes the transistors' voltage stress, and features natural current sharing between the phases*. The new double series-capacitor buck converter (DSCBC) adds one series capacitor and one transistor to the component count of a series-capacitor buck converter. It is especially beneficial in terms of volume, cost, and efficiency for VRM applications and as a 48 V-to-1.x V single-stage converter solution.

The rest of the paper is organized as follows. Section II presents the DSCBC principle of operation and provides typical key waveforms of the new converter. In Section III, a full steady-state analysis of the DSCBC is delineated and simulation results are presented. Experimental results and efficiency measurements are provided in Section IV, and Section V concludes the paper.

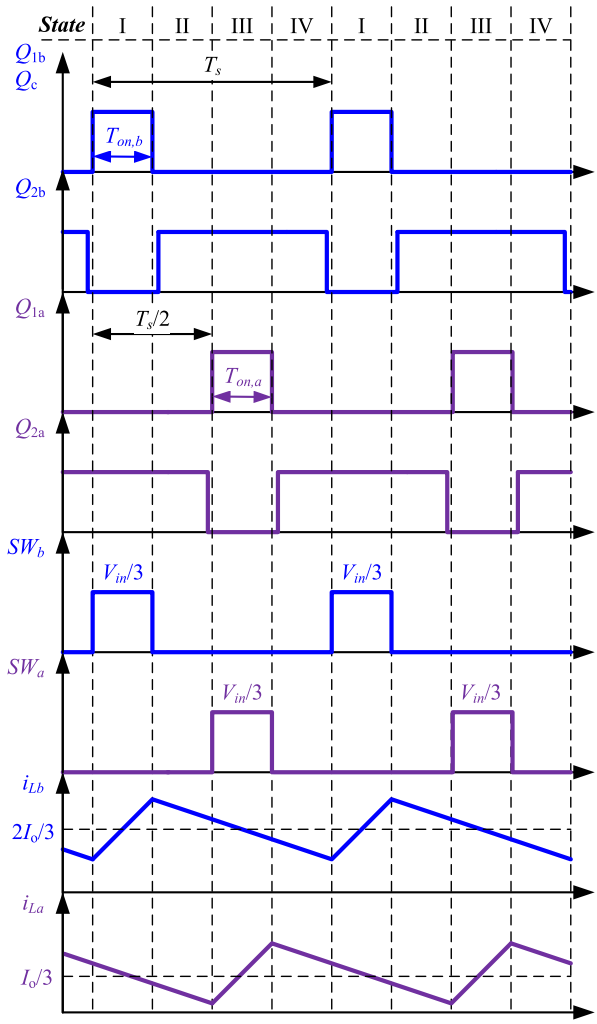


Fig. 2. Idealized waveforms of the DSCBC topology.

II. Double Series-Capacitor Buck Converter

The DSCBC topology, shown in Fig. 1, combines the benefits of a switched-capacitor circuit and a series-capacitor buck converter. This topology adds two series capacitors (C_{t1} and C_{t2}) and one transistor (Q_c) to the component count of a standard two-phase buck converter and has a total of five transistors, two power delivery capacitors, and two inductors. The converter's configuration and waveforms resemble the ones of the series-capacitor buck converter and the two-phase interleaved buck converter, with the benefits of tripled duty ratio, lower voltage stress transistors, and inherent current balancing, making the topology an ideal candidate for high output current high conversion ratio applications.

The description of the DSCBC operation is aided by the idealized timing diagram in Fig. 2 and the subcircuits with their currents paths highlighted in Fig. 3. The switching period is divided into four time intervals with four states (I–IV), where states II and IV are, in fact, identical. During state I [phase B is ON and phase A is OFF, see Fig. 3(a)] the transistors Q_{1b}, Q_{2a}, and Q_c are ON. The input voltage connects to L_b through the capacitor C_{t2} which reduces the applied voltage on the inductor, and the inductor current i_{Lb} is ramped up while

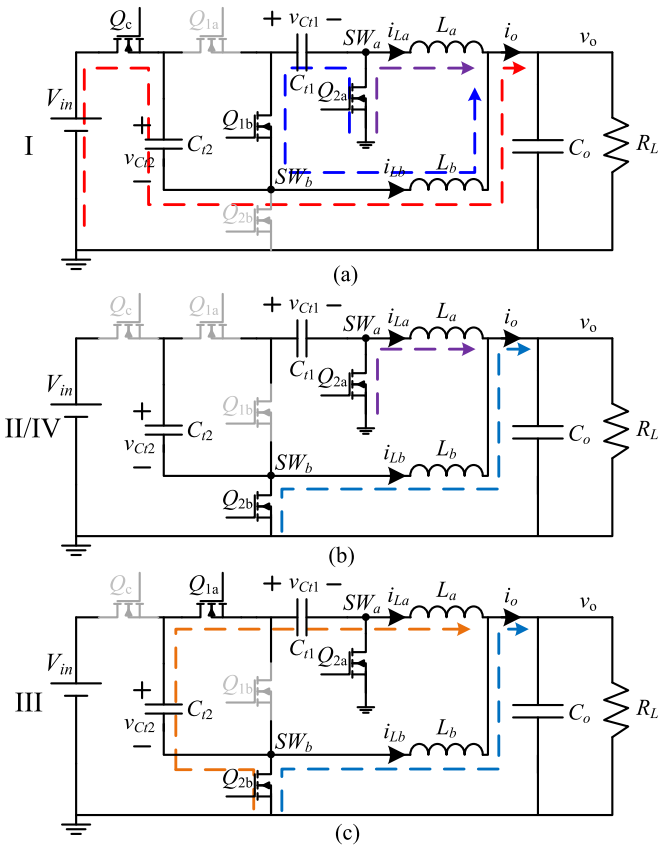


Fig. 3. Currents paths in the DSCBC topology. (a) State I: phase B is ON and phase A is OFF. (b) States II and IV: both phases A and B are OFF. (c) State III: phase B is OFF and phase A is ON.

charging C_{t2}. In parallel, the capacitor C_{t1} also connects to L_b and discharges. Since in this phase SW_a is at GND, the inductor L_a is connected between GND and the output capacitor C_o and delivers its stored energy to the output. In state II [see Fig. 3(b)], the transistors Q_{2a} and Q_{2b} are ON, resulting in both nodes SW_a and SW_b to connect with GND, and both phases A and B are OFF. Both inductors are connected between GND and C_o and the inductors currents ramp down. State III [phase A is ON and phase B is OFF, see Fig. 3(c)] start at half the switching period at $T_s/2$ and the transistors Q_{1a} and Q_{2b} are ON. L_a is sourced by a series connection of C_{t2} and C_{t1}, where C_{t2} is discharges while C_{t1} is charged by i_{La}. Since SW_b is at GND, the stored energy in the inductor L_b is delivered to the output. By connecting the two capacitors in series with opposite polarities the applied voltage on L_a during this state is lowered, resulting in a lower current ripple that, in turn allows the extension of the duty ratio. State IV is identical to state II, transistors Q_{2a} and Q_{2b} are ON and the two phases are OFF.

As can be observed in Fig. 2, by setting a symmetrical duty-ratio command on both phases, the operation of the DSCBC is similar to a two-phase interleaved buck converter with an input voltage one-third V_{in} for each phase which translates to extended duty-ratio operation with respect to the input voltage. In addition, the average current is distributed $I_o/3$ and $2I_o/3$ ratio which also implies on the power that is processed by each phase. As will be analyzed and further detailed in the next section, while the basic features (extended duty ratio, lower voltage stress, and current balancing) are maintained, the duty-ratio settings of each phase translates into power processed by it, a feature that adds another degree of freedom in optimizing the design of the converter.

III. Steady-State Analysis

The steady-state analysis of the DSCBC topology presented in this section is assisted by a steady-state simulation of a 30 W 48 V-to-1 V converter, operating at 500 KHz switching frequency per-phase, and is depicted in Fig. 4. The simulation shows the key waveforms of the new topology: inductors currents, output voltage, switching nodes voltages, series capacitors voltages and currents, and voltage stress of all the transistors.

A. Average Analysis and Voltage Gain

A key factor in the operation of the DSCBC is the capacitors voltages, which lower the transistors voltage stress and enable the operation with larger on-time of the transistors compared to both a buck converter and a series-capacitor buck converter. Since the average voltage applied on the inductors is zero, the average voltages at the switching nodes SW_b and SW_a equal V_o, the average output voltage can be expressed as

$$\begin{aligned}(V_{\mathrm{in}} - V_{\mathrm{Ct2}})\, D_b &= V_o \\ (V_{\mathrm{Ct2}} - V_{\mathrm{Ct1}})\, D_a &= V_o,\end{aligned} \tag{1}$$

where $D_a = T_{\mathrm{on},a}/T_s$ and $D_b = T_{\mathrm{on},b}/T_s$ are the duty ratios for phases A and B, respectively. During state I, the sum of the capacitors' voltages equals the input voltage, i.e.,

$$V_{\mathrm{Ct1}} + V_{\mathrm{Ct2}} = V_{\mathrm{in}}. \tag{2}$$

Using (1) and (2), and after some manipulations, yields the average capacitors voltages

$$\begin{aligned}V_{\mathrm{Ct2}} &= \frac{D_a + D_b}{2D_a + D_b} V_{\mathrm{in}} \\ V_{\mathrm{Ct1}} &= \frac{D_a}{2D_a + D_b} V_{\mathrm{in}}.\end{aligned} \tag{3}$$

The voltage conversion ratio can be derived from (1) and (3), and can be expressed as

$$M = \frac{V_o}{V_{\mathrm{in}}} = \frac{D_a D_b}{2D_a + D_b}. \tag{4}$$

Therefore, (3) and (4) imply that setting equal duty ratios, i.e. $D_a = D_b = D$, for the two phases, results in average capacitors voltages of $V_{\mathrm{Ct2}} = 2V_{\mathrm{in}}/3$ and $V_{\mathrm{Ct1}} = V_{\mathrm{in}}/3$, where the expression for voltage conversion ratio is reduced to

$$M = \frac{V_o}{V_{\mathrm{in}}} = \frac{D}{3} \tag{5}$$

which is three times higher compared to the duty ratio of a buck converter.

B. Steady-State Inductors Currents and Output Voltage Ripple

As mentioned in Section II, the operation of the DSCBC is similar to a two-phase interleaved buck converter, but with different input voltage for each phase. The input voltage for

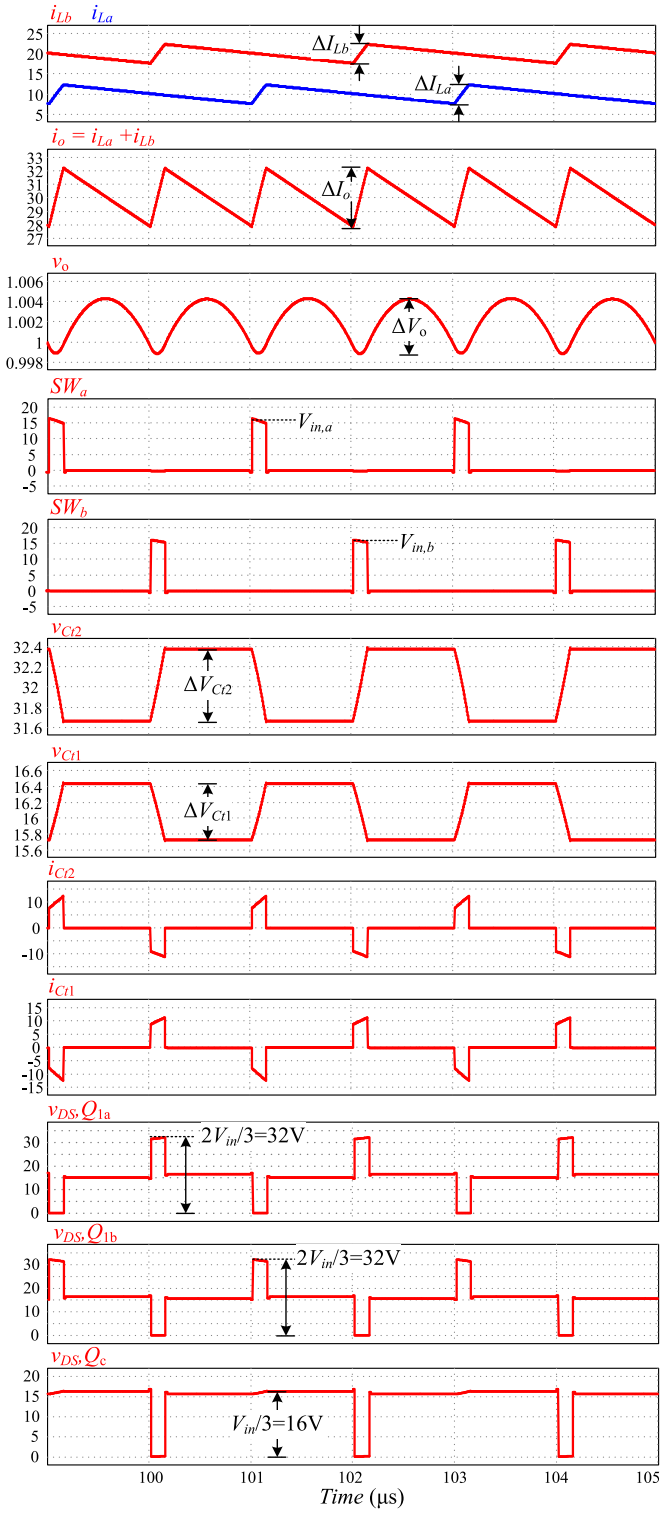


Fig. 4. Simulation waveforms of the DSCBC topology for equal duty ratios.

each of the phases is calculated by the voltage during the on-time of each phase at the nodes SW_a and SW_b for phases A and B, respectively. Using (3), the input voltage of phase A can be expressed as

$$V_{\mathrm{in},a} = V_{\mathrm{Ct2}} - V_{\mathrm{Ct1}} = \frac{D_b}{2D_a + D_b} V_{\mathrm{in}} \tag{6}$$

and in a similar manner, the input voltage of phase B is

$$V_{\mathrm{in},b} = V_{\mathrm{in}} - V_{\mathrm{Ct2}} = \frac{D_a}{2D_a + D_b} V_{\mathrm{in}}. \tag{7}$$

As a result, two effective voltage conversion ratios for each of the phases are considered, $V_o/V_{\mathrm{in},a}$ for phase A and $V_o/V_{\mathrm{in},b}$ for phase B.

The slew rates of the inductors currents $\mathrm{i_{La}}$ and $\mathrm{i_{Lb}}$ during the on-time of each of the phase are

$$\left.\frac{di_{\mathrm{La}}}{dt}\right|_{\mathrm{on},a} = \frac{V_{\mathrm{Ct2}} - V_{\mathrm{Ct1}} - V_o}{L_a}, \quad \left.\frac{di_{\mathrm{Lb}}}{dt}\right|_{\mathrm{on},b} = \frac{V_{\mathrm{in}} - V_{\mathrm{Ct2}} - V_o}{L_b} \tag{8}$$

where for the rest of the period the slew rates are

$$\left.\frac{di_{\mathrm{La}}}{dt}\right|_{\mathrm{off},a} = -\frac{V_o}{L_a} \quad \left.\frac{di_{\mathrm{Lb}}}{dt}\right|_{\mathrm{off},b} = -\frac{V_o}{L_b}. \tag{9}$$

The inductors currents' ripples ΔI_{La} and ΔI_{Lb} can be calculated using (8) and are given by

$$\Delta I_{\mathrm{La}} = \frac{V_{\mathrm{Ct2}} - V_{\mathrm{Ct1}} - V_o}{L_a f_s} D_a, \quad \Delta I_{\mathrm{Lb}} = \frac{V_{\mathrm{in}} - V_{\mathrm{Ct2}} - V_o}{L_b f_s} D_b \tag{10}$$

where f_s is the switching frequency. For the private case of equal duty ratios $D_a = D_b = D$, the inductors currents ripples can be expressed as

$$\Delta I_{\mathrm{La}} = \frac{V_{\mathrm{in}}/3 - V_o}{L_a f_s} D, \qquad \Delta I_{\mathrm{Lb}} = \frac{V_{\mathrm{in}}/3 - V_o}{L_b f_s} D. \tag{11}$$

Assuming equal duty ratios, the output voltage ripple can be calculated using the charge delivered and consumed from the output capacitor during a switching period and can be expressed as

$$\Delta V_o = \frac{\Delta I_o}{8 C_o f_s} \tag{12}$$

where ΔI_o is the total current ripple at the output, obtained by summing the inductors currents, i.e., the ac component magnitude of $i_{\mathrm{La}}(t) + i_{\mathrm{Lb}}(t)$. Using (8), (9), and after some manipulation ΔI_o is given by

$$\Delta I_o = \frac{(V_{\mathrm{in}}/3 - V_o)\, L_b - V_o L_a}{L_a L_b f_s} D \tag{13}$$

and assuming $L_a \approx L_b \approx L$ the output voltage ripple is calculated by substitution of (12) into (13)

$$\Delta V_o = \frac{V_{\mathrm{in}} - 6V_o}{24 L C_o f_s^2} D. \tag{14}$$

C. Current Balancing and Power Distribution

The load current I_o is delivered from both phases A and B and equals to the sum of the average inductors currents

$$I_o = I_{\mathrm{La}} + I_{\mathrm{Lb}}. \tag{15}$$

The average value of each of the inductors currents can be calculated using the fact that charge balance is achieved for each of the capacitors C_{t1} and C_{t2}. For example, the charge delivered to C_{t2} during state I must equal the charge consumed

from C_{t2} during state III. This yield

$$\text{State I}: \quad Q_{\text{Ct2}} = \frac{1}{2} I_{\text{Lb}} \frac{D_b}{f_s} \tag{16}$$

$$\text{State III}: \quad Q_{\text{Ct2}} = I_{\text{La}} \frac{D_a}{f_s}. \tag{17}$$

Substituting (15) into (16) and equating it to (17), yields the average inductors currents that are given by

$$I_{\text{La}} = \frac{D_b}{2D_a + D_b} I_o \tag{18}$$

and

$$I_{\text{Lb}} = \frac{2D_a}{2D_a + D_b} I_o. \tag{19}$$

As can be seen in (18) and (19), the average inductors currents depend on the duty-ratio settings. This provides an additional degree of freedom to distribute the load current between the phases by changing the ratio between D_a and D_b. For example, by setting the duty ratios to be equal, the average inductors currents are

$$I_{\text{La}} = \frac{1}{3} I_o$$

$$I_{\text{Lb}} = \frac{2}{3} I_o \tag{20}$$

and by setting $D_b = 2D_a$ the average inductors currents will be equal, i.e.,

$$I_{\text{La}} = I_{\text{Lb}} = \frac{I_o}{2}. \tag{21}$$

D. Series Capacitors Voltage Ripple

The simplified analysis of the converter's behavior in a steady-state operation, and in particular for the average behavior the capacitors voltages V_{Ct1} and V_{Ct2} can be considered constant. However, in practice their voltage ripple, caused by charging and discharging them each switching cycle, can play a crucial role in the final design and size of the converter. It is therefore essential to quantify the voltage ripple for each of the series capacitors.

During the charging and discharging states, the capacitors' currents are determined by the inductor current that is connected to them during the on-time, i.e., by I_{Lb} during state I and by I_{La} during state III. The voltage ripple of the capacitors can be easily calculated during state III, when phase A is ON and both the capacitors are connected in series with L_a

$$\Delta V_{\text{Ct1}} = \frac{I_{\text{La}} D_a}{C_{t1} f_s}, \quad \Delta V_{\text{Ct2}} = \frac{I_{\text{La}} D_a}{C_{t2} f_s} \tag{22}$$

and for equal duty ratios the capacitors voltage ripple can be calculated using (5) and (20), which yields

$$\Delta V_{\text{Ct1}} = \frac{I_o V_o}{C_{t1} V_{\text{in}} f_s}, \quad \Delta V_{\text{Ct2}} = \frac{I_o V_o}{C_{t2} V_{\text{in}} f_s}. \tag{23}$$

It should be noted that the charging and discharging actions of the capacitors are so-called soft-charged [35], i.e., connected through an inductance that dictates the charging or discharging current and as a result does not involve emulated resistance losses [36], [37] that are a function of the switching frequency.

E. Summary of the Topology Highlights

The DSCBC topology features natural current sharing between phases A and B, as can be seen from expressions (18) and (19). The current sharing attribute is the result of the charge balance on the capacitors C_{t1} and C_{t2}, and it is independent on their capacitance values. The feature of duty-ratios-dependent current sharing allows to control the power distribution per phase and enables the proper design of each of the phases. For example, if equal currents between the two phases is desired, setting $D_a = 2D_b$ satisfies the requirement, but comes at the cost of different effective voltage conversion ratios of each of the phases. In this case, phase B voltage conversion ratio will be $V_{\text{in}}/4V_o$ whereas phase A voltage conversion ratio will be $V_{\text{in}}/2V_o$. By setting $D_a = D_b$, phase B current will be twice higher than the current in phase A, according to (20). However, since the current sharing is an inherent feature and it is parameter-independent, the two phases can be designed according to the load (average current) that is being processed by each phase, i.e., with different transistors and inductors for each phase, to optimize the converter's operation, efficiency, and power density.

In addition to the above characteristics of the DSCBC, the topology also lowers the voltage stress of the transistors compared to a two-phase buck converter. As opposed to the voltage stress of the transistors in a buck converter, which is V_{in} for both of the transistors, the voltage stress of the transistors in the DSCBC is divided with an opposite ratio to the current handling per transistor, and fortunately, in favor of higher efficiency design. Here, the voltage stress of the transistors Q_c, Q_{2a}, and Q_{2b} equals V_{Ct1} and the stress of Q_{1a} and Q_{1b} equals V_{Ct2}; all are given in (3). This feature allows for a better and more compact design of the converter, especially in high voltage conversion ratio applications, since the transistors Q_{2a} and Q_{2b} that have much higher rms currents (since they conduct most of the switching cycle at high conversion ratios) also have significantly lower voltage stress which allows the use of transistors with lower $R_{\text{DS(on)}}$ per silicon area. Moreover, for these kind of applications with short on-time, the low rms current through the transistors Q_c, Q_{1a}, and Q_{1b} allows to consider transistors with higher $R_{\text{DS(on)}}$ but with much lower capacitances, which expedites the switching transitions and lowers both switching losses and the gate drivers requirements, especially in high input voltage applications.

IV. Experimental Results

To validate the operation of the DSCBC at high voltage conversion ratio, a 30 W 48 V-to-1 V prototype that operates at 500 KHz switching frequency per phase was built and tested. Table I lists the components values and parameters of the experimental prototype. The converter was digitally controlled using an Altera FPGA [38] using fully digital high-performance ADC and DPWM peripherals as detailed in [39].

Figs. 5–8 show the converter's waveforms for output current of 18 A with equal duty ratios. Fig. 5 shows the input voltage, the

TABLE I
EXPERIMENTAL PROTOTYPE VALUES

Component	*Value/Type*
Input voltage $V_{\rm in}$	48 V
Output voltage V_o	1 V
Switching frequency f_s	500 kHz per phase (1 MHz effective)
Output capacitor $C_{\rm out}$	100 μF
Inductors L_a and L_b	0.44 μH, 0.21 mΩ DCR
Capacitors C_{t1} and C_{t2}	3.3 μF, 100V, 3 mΩ ESR,1206 case
Q_c MOSFET	SiA466EDJ, 20 V, 9.5 mΩ
Q_{1a} and Q_{1b} MOSFETs	Si4288DY, 40 V, 20 mΩ, Dual
Q_{2a} MOSFET	SiRA12DP, 30 V, 4.3 mΩ
Q_{2b} MOSFET	SiRA04DP, 30 V, 2.2 mΩ

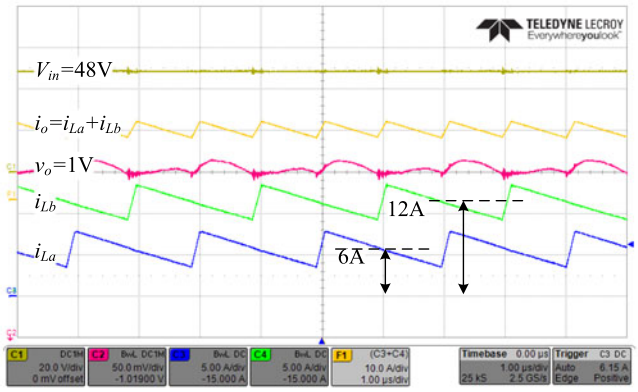


Fig. 5. Experimental results: C1—input voltage (20 V/div), C2—output voltage (50 mV/div), C3—phase A inductor current (5 A/div), C4—phase B inductor current (5 A/div), F1—output current (sum of the inductors currents, 5 A/div). Time scale is 1 μs/div.

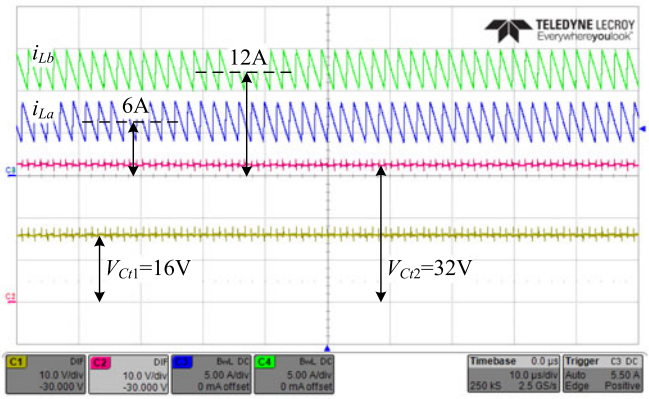


Fig. 6. Experimental results: C1 and C2—series capacitors voltages (10 V/div), C3 and C4—inductors currents (5 A/div). Time scale is 10 μs/div.

output voltage, and the sum of the inductor currents. Due to the two-phase interleaved operation of the converter, the effective switching frequency at the output of the converter doubles, from 500 KHz to 1 MHz. The inductors currents and series capacitors voltages are depicted in Fig. 6. As can be observed, natural current sharing between phases A and B is obtained and with a ratio of 2:1, and the capacitors voltage are $V_{\rm in}/3$ and $2V_{\rm in}/3$ for C_{t1} and C_{t2}, respectively. Fig. 7 shows the voltages at the switching nodes SW_a and SW_b. The duty ratio of the switching

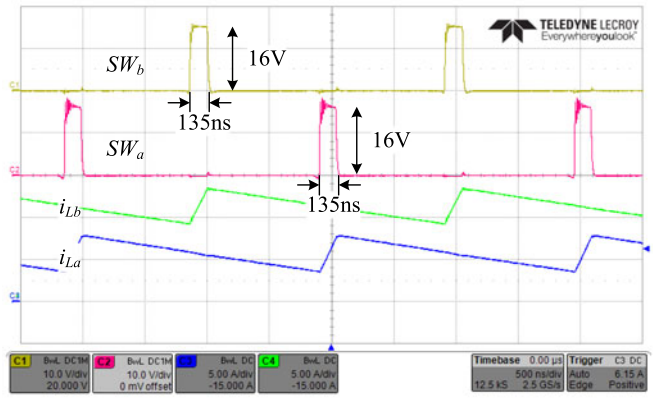
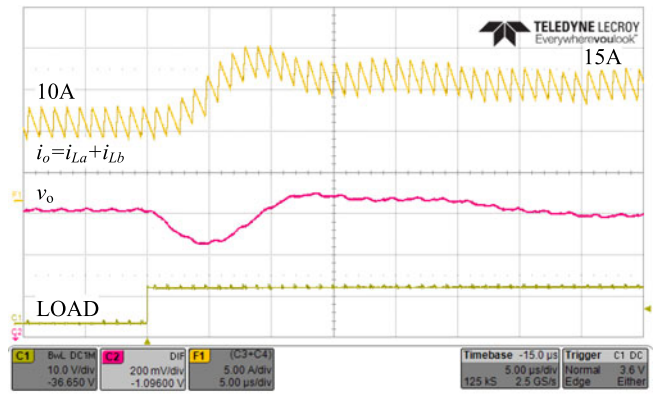
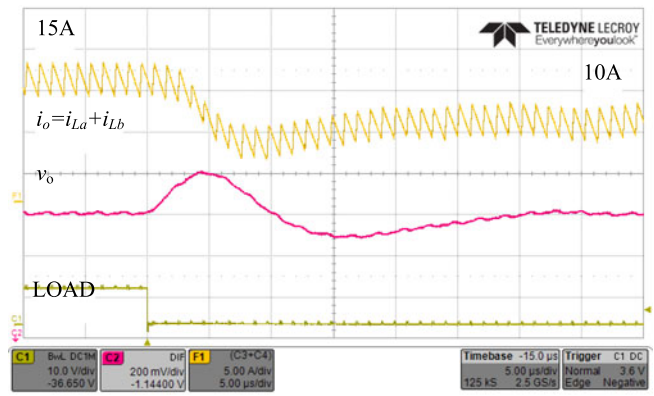


Fig. 7. Experimental results: C1—switching node SW_b (10 V/div), C2—switching node SW_a (10 V/div), C3 and C4—inductors currents (5 A/div). Time scale is 500 ns/div.



(a)



(b)

Fig. 8. Experimental results of 5 A load transients. (a) 10–15 A loading transient and (b) 15–10 A unloading transient. C1—load step signal, C2—output voltage (200 mV/div), F1—output current (sum of the inductors currents, 5 A/div). Time scale is 5 μs/div.

nodes is slightly higher than 1/16 (due to losses), validating the ability of the converter to effectively and practically triple the duty ratio compared to a buck converter. Loading and unloading transients of 5 A are depicted in Fig. 8, demonstrating the fast dynamic response of the converter to load change. Efficiency measurement of the converter with 48 V input and various output

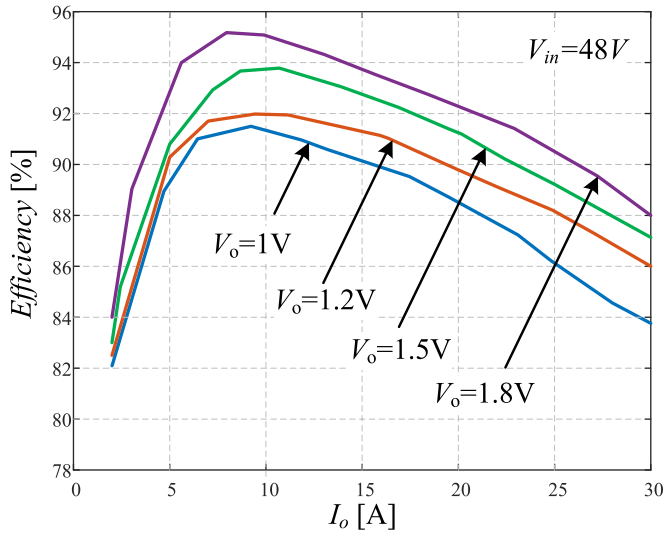


Fig. 9. Experimental efficiency measurements of the DSCBC for different output voltages.

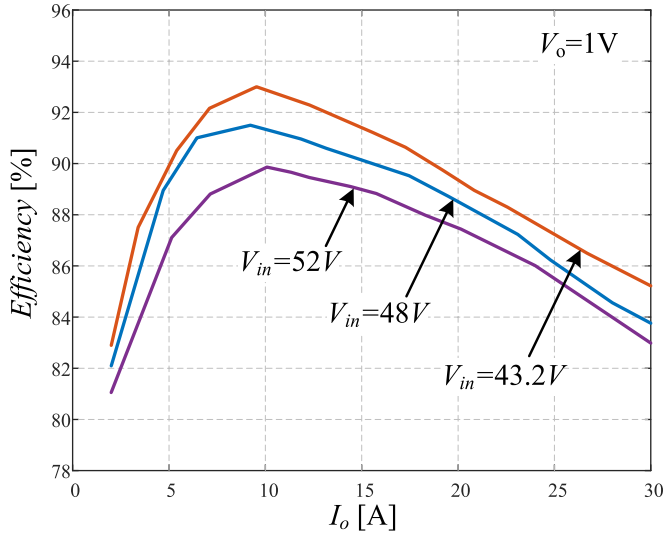


Fig. 10. Experimental efficiency measurements of the DSCBC for different input voltages.

voltages are provided in Fig. 9, demonstrating a peak efficiency of 91.5% and above 88% for most of the load range at 1 V output and even higher efficiency for higher output voltages. Fig. 10 shows the efficiency measurement for 1 V output and various input voltages to examine the DSCBC efficiency in case the input voltage is unregulated.

V. Conclusion

A new very high step-down conversion ratio with high efficiency and nonisolated converter topology has been presented. The topology comprises two-phases for high current delivery and uses two series capacitors, operating with soft-charging characteristic. The energy processing by the capacitors significantly lowers the voltage stress of the transistors, triples the duty ratio and provides an inherent current sharing feature between the two phases. These properties reduce the VRM's volume while increasing the efficiency in 48 V-to-1.x V conversion that is common and highly desired in datacenters and other cutting-edge applications.

The experimental results validated the theoretical analysis and demonstrated the superior performance of the topology for a 48 V-to-1 V operation, achieving 91.5% peak efficiency and above 88% for most of the load range. The high efficiency of the converter has been obtained while the solution has not compromised other important specifications such as fast dynamic response. These make the new converter topology a very attractive candidate for 48 V input, single-stage PoL converters for datacenters, and other VRM applications.

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