

Fast Response of Deviation-Constrained Hybrid Controllers for Indirect Energy Transfer Converters

Or Kirshenboim ¹, *Student Member, IEEE*, and Mor Mordechai Peretz ², *Member, IEEE*

Abstract—This paper introduces and surveys a new family of transient-oriented controllers for indirect energy transfer converters. The controllers incorporate a peak current programmed mode control for steady-state operation and a nonlinear, state-plane-based transient-mode control schemes for load transients. The new controllers facilitate extremely fast convergence from a loading transient to the new steady-state operating point while constraining the output voltage and inductor current deviations to a desired (minimal) value. As a result, the loading transient performance of indirect energy transfer converters can be significantly improved since two control objectives (convergence time and minimal components' stress) are simultaneously obtained. A detailed principle of operation of the controllers is provided and explained through a state-plane analysis. The operation of the controllers is experimentally verified on a 30 W 3.3 V-to-12 V boost converter, demonstrating a significantly lower output voltage deviation and lower peak inductor current when compared to time-optimal control, allowing for volume reduction of the converter.

Index Terms—Digital control, nonlinear control, state-space control, time-optimal control.

I. INTRODUCTION

Tighter output voltage regulation, faster response time to load changes, and lower volume are of major concern in the design of modern switch-mode power supplies. To obtain fast transient response, beyond the small-signal bandwidth, some transient-oriented controllers, among them time-optimal controllers have been introduced [1]–[9]. These controllers implement nonlinear, state-variable-based control laws, which allow convergence to large-signal perturbations that is only limited by the physical limitations of the reactive components, e.g., inductor current slew-rate. For system performance improvement and total volume reduction of the converter, in particular for boost-type converters, decreasing of the components' stress has been assigned as the primary performance goal [10]. This goal can be achieved by setting the control objective as an output voltage deviation minimization and peak inductor current reduction rather than the convergence time [11], [12]. Due to this trade-off, recent studies have introduced a benchmarking tool for evaluating the

response of converters when compared to the physical limit, i.e., compared to the minimum output voltage deviation and minimum response time [13].

Nonlinear, large-signal transient-oriented controllers can be generally divided into two types. The first type uses a single control law for the entire operation range of the converter, e.g., boundary controllers [14]–[31] with particular cases of hysteretic and sliding-mode controllers [32]–[35]. Boundary controllers are defined as a switching surface on the state space and for the case of indirect energy transfer converters can achieve low output voltage deviation [12] or time-optimal response for both start-up transients and load transients using the natural switching surface [17]–[20]. In the past, these controllers suffered from variable switching frequency, difficult implementation when designed as steady-state controllers and it was hard to guarantee the controller's stability. However, recent studies solved these issues by using boundary control law in pulse width modulation (PWM) switching mode [21], definition of the region-of-convergence to guarantee the large-signal stability [36], and efficient hardware implementation [12]. So far, boundary controllers mainly focused on a single control objective, either time-optimal response or minimum output voltage deviation, and controllers that combine these control objectives (within the physical limits of indirect energy transfer converters) have not been introduced. The second type of controllers merges control laws of different kinds (linear and nonlinear) and switch between them depending on the operating conditions. Within the context of power converters applications, a hybrid controller typically merges a steady-state linear controller (i.e., PI or PID) to achieve zero steady-state error by simple means [37] and allow constant operating frequency which simplifies the design of the power converter, and a transient-mode controller to enable the desired large-signal response.

Implications of the control method on the resultant response may vary from one converter configuration to another. For example, with direct energy transfer converters, e.g., buck or forward, the time-optimal control produces the fastest possible dynamic response to load transients with the minimum possible output voltage deviation. However, when applying time-optimal control on indirect energy transfer converters, e.g., boost or flyback, the fast dynamic response comes at the cost of higher output voltage deviation and peak inductor current, increasing the sizing requirements from both the output capacitor and the inductor. On the other hand, minimum output voltage deviation for boost-type converters results in prolong transient time, infinite in the ideal case [12].

The main goal of this paper is to introduce a new set of controllers for indirect energy transfer converters that, compared

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The authors are with the Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 8410501, Israel (e-mail: orkir@post.bgu.ac.il; morp@ee.bgu.ac.il).

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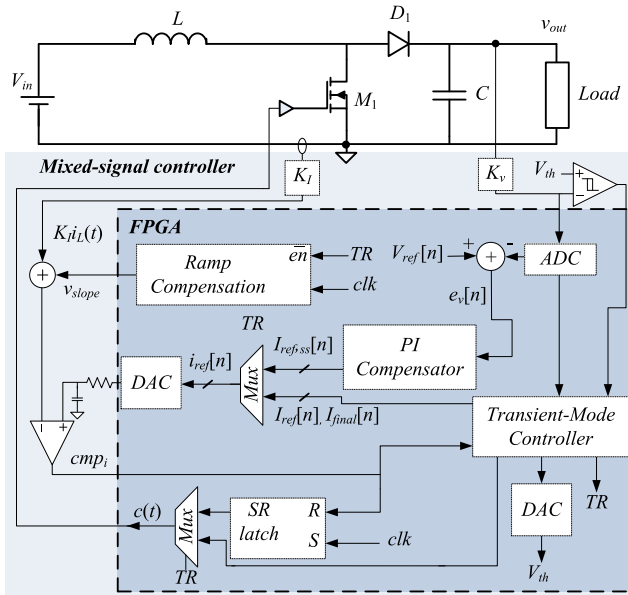


Fig. 1. Generalized FCDC hybrid controller regulating operation of a boost converter.

to the time-optimal solutions, constrain the output voltage deviation or peak inductor current (or both) while maintaining fast convergence in response to load transients. This translates to output capacitance reduction and smaller magnetic element for the inductor. A generalized realization for the fast convergence within a deviation-constrained (FCDC) hybrid controller is depicted in Fig. 1. It incorporates a steady-state peak current programmed mode (CPM) controller and a transient-mode controller. The transient-mode controller utilizes a new nonlinear, state-plane-based control and is designed to produce a load transient response that *constrains the output voltage and/or peak inductor current deviation to a desired value while maintaining very short transient time within these constraints*.

The rest of the paper is organized as follows: Section II delineates the state-plane and time representation. The FCDC controllers' design and control schemes are given in Section III, including detailed simulations. Section IV provides an analysis to determine the minimum expected voltage drop when using the FCDC controllers. Next, Section V provides expansion of the controllers for other topologies along with practical implementation details. Experimental results of the FCDC controllers and time-optimal controller are presented in Section VI. Section VII concludes the paper.

II. STATE-PLANE AND TIME REPRESENTATION

In state-plane representation, the time parameter is implicit, and as a result, evaluation of the convergence period from one operating conditions to another is not immediate. However, the rate of convergence of a switch-mode converter can be expressed by means of energy and power with respect to the state variables. This section aims to describe the relationship between the time of convergence and the movement of the state variables on the state plane by an example of a loading transient on a boost converter that is loaded by a resistive load (RL).

When the load changes, the controller of the converter is in charge of bringing the state variables from an initial steady-state

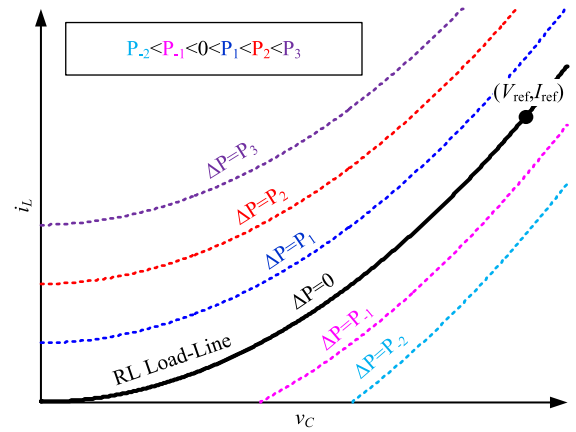


Fig. 2. Power representation on the state plane of a boost converter loaded by an RL.

operating point to a new one. Each steady-state point indicates an instantaneous energy stored in the reactive components of the converter, i.e., $e = Cv_C^2/2 + Li_L^2/2$. For a loading transient event, this stored energy of the previous steady-state point $E_{old} = CV_{ref}^2/2 + LI_{old}^2/2$ must rise up to a new, higher energy $E_{ref} = CV_{ref}^2/2 + LI_{ref}^2/2$. The rate of energy change in the converter can be obtained by taking the energy derivative with respect to time, as follows:

$$\frac{de}{dt} = Cv_C \frac{dv_C}{dt} + Li_L \frac{di_L}{dt} = V_{in}i_L - \frac{v_C^2}{R} = P_{in} - P_{out} = \Delta P. \quad (1)$$

This implies that the energy rises faster for higher difference between the input and output power. For a boost converter case, (1) is valid for both the ON and OFF state trajectories.

According to 0 and [32], the load line represents the states where $P_{in} = P_{out}$, i.e., $\Delta P = 0$. Accordingly, the points on the state plane where $i_L > v_C^2/RV_{in}$ represent points of $\Delta P > 0$. As demonstrated in Fig. 2, higher i_L results in higher ΔP ; above the load line (see Section IV), ΔP is greater than zero which expedites the convergence for a loading transient. Using this observation and taking into account the possible trajectories of the converter, an enhanced convergence time controller can be designed as detailed in the next section.

III. FAST CONVERGENCE WITHIN A DEVIATION-CONSTRAINED HYBRID CONTROLLER

The control objective of transient-oriented controllers ranges from minimum recovery time to minimum output voltage deviation in response to load transients and usually focus on one of them. As opposed to direct energy transfer converters, e.g., buck or forward, where minimum convergence time results in minimum output voltage deviation, a control objective of minimum output voltage drop for indirect energy transfer converters results in long transient time which is, in fact, infinite in the ideal case [12]. The reason for this behavior is that the first point in the region-of-convergence [36] is located on the load line, where $\Delta P = 0$, and therefore the rate of convergence is slow. Based on the energetic description of the previous section, FCDC controllers that combine a fast recovery time for an allowed voltage deviation constraint, current deviation constraint, and both voltage and current deviations constraints have been developed. The

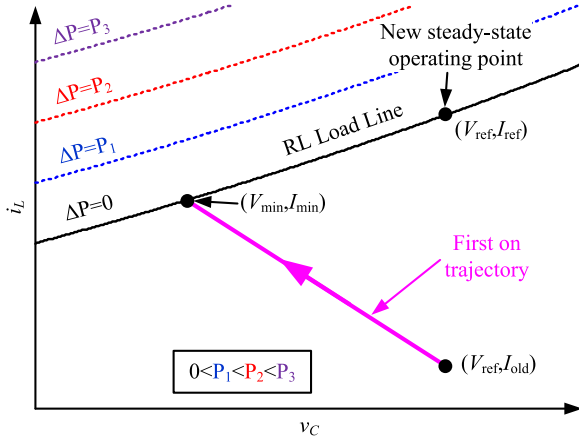


Fig. 3. Intersection of the first on trajectory with the load line.

controllers' operation is demonstrated on a boost converter, but due to the high resemblance of the state-plane and state trajectories of indirect energy transfer converters it can be used for other converters as well. Therefore, the FCDC controllers' operation can be easily modified to fit other indirect energy transfer converters, e.g., buck–boost, noninverting buck–boost (NIBB), and flyback, using transformation of the state equations as given in Section V.

The design approach of the FCDC controllers family is aided by the state-plane illustration shown in Fig. 3. At the detection of a loading transient, by turning the transistor ON, the ON trajectory brings the state variables to the (V_{\min}, I_{\min}) point (the intersection with the load line, see Section IV). Following the possible trajectories of a boost converter, convergence to the new steady-state operating point $(V_{\text{ref}}, I_{\text{ref}})$ is impossible without a further increment of the inductor current and as a result, increasing the voltage drop [12]. Theoretically, there is infinite number of possible movement patterns from (V_{\min}, I_{\min}) toward $(V_{\text{ref}}, I_{\text{ref}})$, but when taking into account constraints on the deviation of either the voltage or the current and based on the energetic description of the previous section, three movement patterns remain. The three types of possible FCDC controllers are

- 1) Voltage-deviation-constrained controller,
- 2) Current-deviation-constrained controller, and
- 3) Voltage- and current-deviation-constrained controller.

The new controllers provide extremely fast dynamic response for loading transients without adding components' stress due to higher voltage deviation or higher peak current, while satisfying the large-signal stability criteria for indirect energy transfer converters that are delineated in [36].

A. Voltage-Deviation-Constrained Hybrid Controller

Employing the observations of the previous section, the fastest way to increase the stored energy without increasing the voltage deviation is to ramp up the inductor current vertically, along V_{th} , as illustrated in Fig. 4. Since such trajectories do not exist, a simple hysteretic-type sliding-mode control along the boundary $v_C = V_{\text{th}}$ has been added, causing the state variables to move vertically by sequenced ON and OFF states

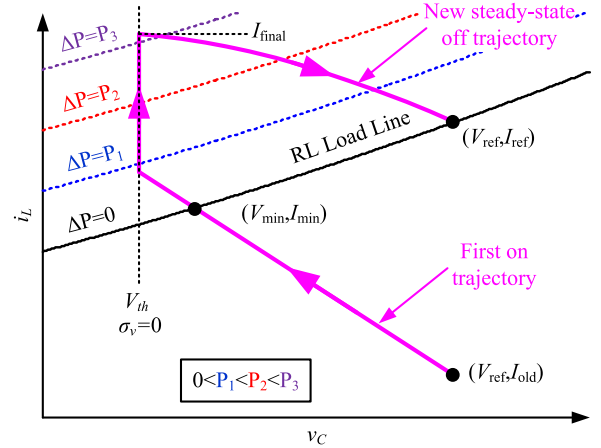


Fig. 4. Illustrative movement of the state variables on the state plane for the voltage-deviation-constrained controller handling a loading transient.

(chattering), similarly to bang–bang control along V_{th} . This can be realized by a simple comparator with hysteresis, and as a sliding-mode controller can be expressed as

$$\begin{aligned} \sigma_v(v_C, i_L) &= v_C - V_{\text{th}}, \quad \text{for } i_L < I_{\text{final}} \\ \text{on : } &\sigma_v > 0 \\ \text{off : } &\sigma_v < 0. \end{aligned} \quad (2)$$

During steady-state operation, the CPM controller is active. Upon detection of a loading transient, from I_{old} to I_{ref} , the transient controller recovers from a loading transient in a three-step process, as demonstrated by the simulation results in Fig. 5. First, the CPM controller is bypassed and the transistor of the boost is turned ON, while the new load state is estimated using the procedure described in Section V. During this time and based on the new load estimation, the controller sets two thresholds, one for the output voltage V_{th} and the other for the inductor current I_{final} . V_{th} is the output voltage-deviation constraint and must be lower than V_{\min} , and I_{final} is determined by the OFF state trajectory passing through the new steady-state operating point and by V_{th} , given by

$$\begin{aligned} I_{\text{final}} &= \frac{V_{\text{ref}}}{R} \\ &+ \sqrt{\frac{C}{L} \left((V_{\text{ref}} - V_{\text{in}})^2 - (V_{\text{th}} - V_{\text{in}})^2 \right) + \left(\frac{V_{\text{ref}}^2}{RV_{\text{in}}} - \frac{V_{\text{ref}}}{R} \right)^2}. \end{aligned} \quad (3)$$

Once the output voltage has dropped and reached V_{th} , during the second step, the controller operates as sliding-mode controller along the boundary (2), causing the inductor current to rise up without changing the voltage. The end of the second step is defined when the inductor current has reached I_{final} . Then, the controller enters the third and last step, turning the transistor OFF and ramping the inductor current down by charging the output capacitor back to the steady-state voltage V_{ref} . Once reaching V_{ref} , the transient recovery has completed and the steady-state CPM controller is resumed.

To avoid any windup issues during steady-state resume caused by the usage of different controllers, once the output voltage

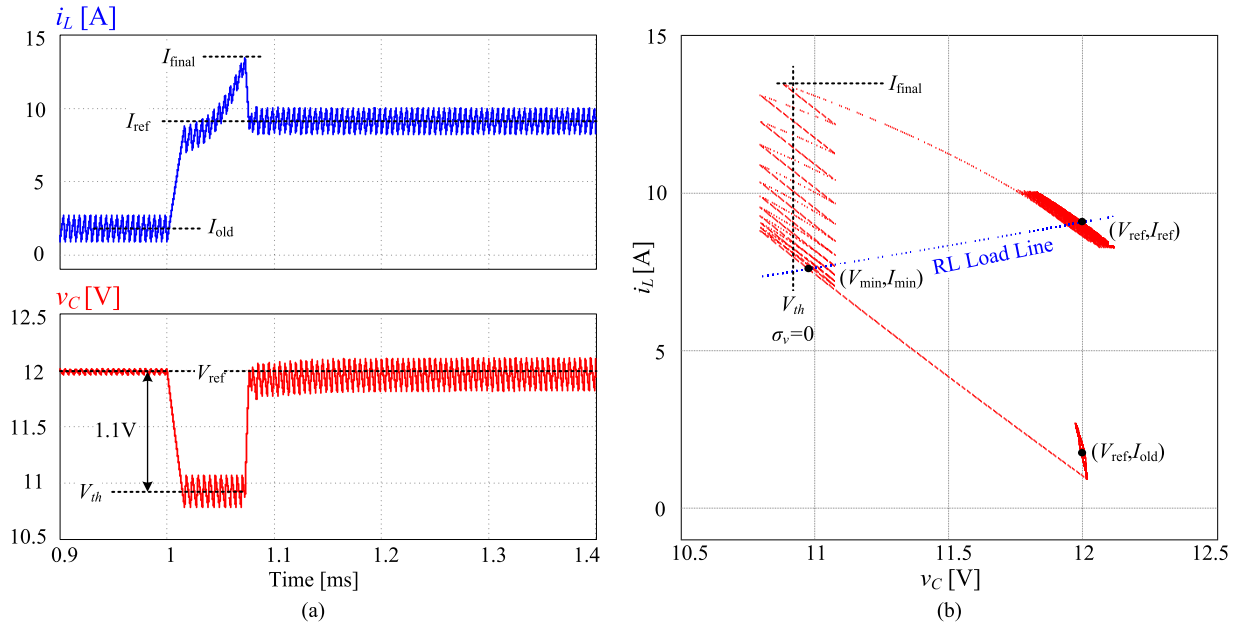


Fig. 5. Simulated response of the voltage-deviation-constrained hybrid controller to a 2.5 A loading transient of a boost converter loaded by an RL. (a) Inductor current (top—blue) and output voltage (bottom—red). (b) State-plane representation of the output voltage and inductor current.

reaches V_{ref} , the PI compensator's error register is set to zero to allow smooth controller transition, while its output $I_{ref,ss}$ (see 0) is set using the load current estimation. It should be noted that calculation of (3) requires information about the converter's parameters, which may lead to robustness issues. To overcome this obstacle, controllers that do not require the value of I_{final} and therefore do not require any information about the converter's parameters have been developed and are presented in the following sections.

B. Current-Deviation-Constrained Hybrid Controller

In a similar manner to the operation of the voltage-deviation-constrained controller, the current-deviation-constrained controller recovers from a loading transient in a two-step process. This controller limits the inductor current to be not higher than the new steady-state inductor current, eliminating any current overshoot. First, the transistor is turned ON to ramp up the inductor current, and the output voltage decreases, as illustrated in Fig. 6. During this time, the new load current is estimated, and by using the load current estimation the controller sets a current threshold I_{th} that equals the new steady-state inductor current I_{ref} , i.e., $I_{th} = I_{ref}$. In the second step, the controller is assisted by the current threshold to operate as a sliding-mode controller along it to create a pseudo-horizontal trajectory, defined by

$$\begin{aligned} \sigma_i(v_C, i_L) &= i_L - I_{th}, \quad \text{for } v_C < V_{ref} \\ \text{on : } \sigma_i &< 0 \\ \text{off : } \sigma_i &> 0. \end{aligned} \quad (4)$$

This sliding phase maintains the inductor current in the close neighborhood of I_{ref} , and since in this region $\Delta P > 0$, the output voltage must rise back up to V_{ref} . Once the output voltage has reached the value of V_{ref} it will not pass it, i.e., there will be no overshoot, as demonstrated by the simulation results in Fig. 7. Since at this point $\Delta P = 0$, no overshoot of the output voltage occurs, and therefore the output voltage remains V_{ref} and steady-

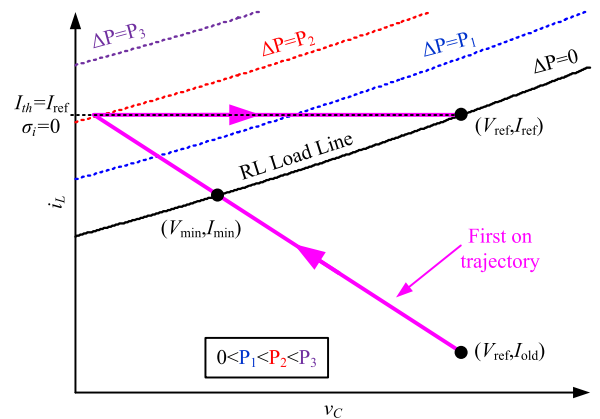


Fig. 6. Illustrative movement of the state variables on the state plane for the current-deviation-constrained controller handling a loading transient.

state CPM controller can be resumed. It should be noted that using this controller, the output voltage deviation is expected to be higher than the one achieved by the voltage-deviation-constrained controller for the same load step. This is since the intersection of the first on trajectory with the sliding boundary occurs at a lower voltage than V_{min} , whereas with the voltage-deviation-constrained controller this intersection can limit the voltage deviation to be as close as desired to V_{min} in order to minimize the output voltage deviation. In spite of the voltage deviation penalty, this controller does not require any additional hardware to the existing steady-state hardware, since only one comparator with hysteresis for the current is needed, which is already available with the steady-state CPM control. Another important advantage of this controller is that the value of I_{final} is not required which simplifies the controller and that the convergence of the output voltage is smooth and naturally stable [36], governed by the inductor current.

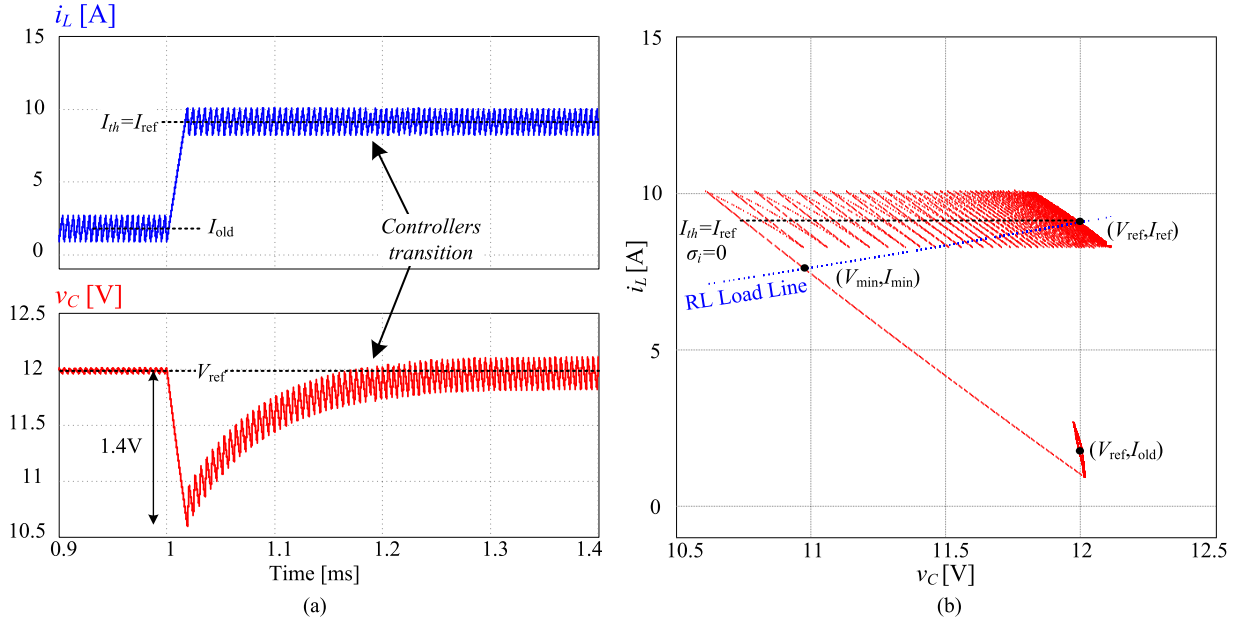


Fig. 7. Simulated response of the current-deviation-constrained hybrid controller to a 2.5 A loading transient of a boost converter loaded by an RL. (a) Inductor current (top—blue) and output voltage (bottom—red). (b) State-plane representation of the output voltage and inductor current.

At the end of transient, when the transition between the transient-mode and steady-state controller occurs and regardless of setting the PI compensator's error register to zero, a small mismatch between the instantaneous inductor current and the new steady-state inductor current may occur. This is due to two reasons:

- 1) The transient-mode controller and the steady-state controller are not synchronized, and therefore the start of the switching period occurs when the inductor current is within the current ripple value, but its instantaneous value is unknown; and
- 2) The ripple of the inductor current is not taken into account when designing the controllers, and it is assumed to be small.

These two reasons for the current mismatch can be translated into a limit on the current error at the end of transient i_{error} , given by

$$|i_{\text{error}}| = |I_{\text{ref}} - i_L| < \Delta I_{\text{ripple}} \quad (5)$$

where ΔI_{ripple} is the steady state's inductor current ripple. Since the maximum current error is limited by the current ripple magnitude and it is relatively small, the transition does not cause any significant problems such as cycling back and forth between the controllers. It should be noted that when neglecting the ripple effect, the transition between the controllers is smooth. The transition between controllers is presented in Fig. 7, showing the small current error at the transition instance and its minor effect on the output voltage.

C. Voltage- and Current-Deviation-Constrained Hybrid Controller

Using the results of the two controllers for voltage and current deviations constraints, a third controller that merges the two controllers has been developed. This controller constrains both

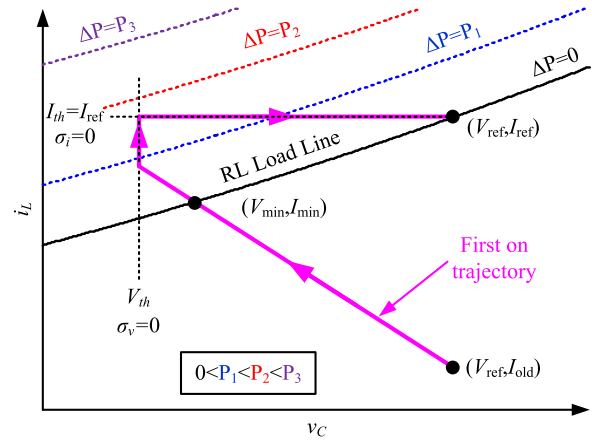


Fig. 8. Illustrative movement of the state variables on the state plane for the voltage- and current-deviation-constrained controller handling a loading transient.

the output voltage to a desired level and the inductor current to the new steady-state value and operates in a three-step process as well. First, similar to the other controllers, the transistor is turned ON to ramp up the inductor current, while the output voltage decreases and the new load state is estimated. During this step, the controller sets two thresholds, one for the output voltage V_{th} and the other for the inductor current I_{th} , based on the load estimation. The threshold V_{th} is set to be lower than V_{min} and the threshold I_{th} is set to be the new steady-state inductor current I_{ref} , as illustrated in Fig. 8. In the second step, the controller is assisted by the voltage threshold to operate as a sliding-mode controller that is defined by

$$\begin{aligned} \sigma_v(v_C, i_L) &= v_C - V_{\text{th}}, \quad \text{for } i_L < I_{\text{th}} \\ \text{on : } &\sigma_v > 0 \\ \text{off : } &\sigma_v < 0. \end{aligned} \quad (6)$$

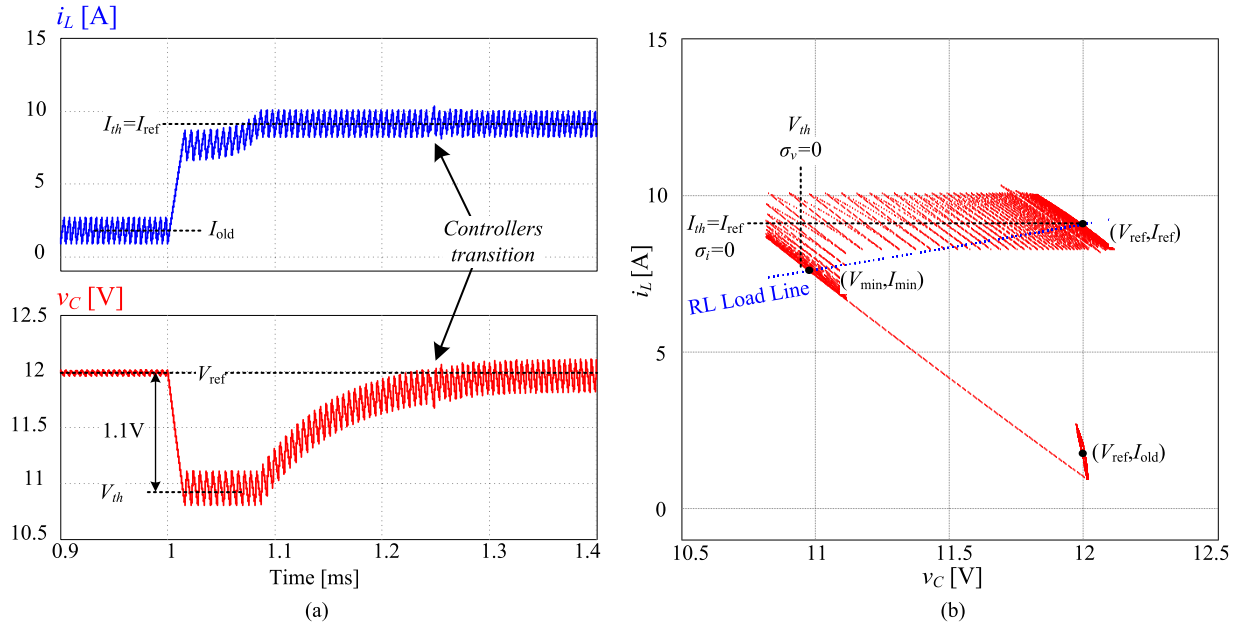


Fig. 9. Simulated response of the voltage- and current-deviation-constrained hybrid controller to a 2.5 A loading transient of a boost converter loaded by an RL. (a) Inductor current (top—blue) and output voltage (bottom—red). (b) State-plane representation of the output voltage and inductor current.

During this step, the inductor current rises without changing the output voltage, until it reaches the current threshold I_{th} and the controller moves on to the third step. During the third and final step, the controller operates similarly to the current-deviation-constrained controller. It moves along the boundary $i_L = I_{th}$ in a sliding-mode operation, with the same controller that is defined by (4). This controller enables the volume reduction of both output capacitance (due to lower output voltage deviation) and inductor (due to lower peak current), but comes at the cost of slightly longer transient time (although the increment is minor within these constraints) compared to the other controllers presented in this study. The advantage of this control scheme over the current-deviation-constrained controller is its ability to constrain the output voltage deviation to its minimal value during the load transients without any hardware penalty. As explained in the previous section, the transition between the steady-state and transient mode controllers may create a small current error, and also here the transition, marked in Fig. 9, has a minor effect on the output voltage. An evaluation of the maximum switching frequency during each of the sliding phases is detailed in Section V.

D. Comparison of the FCDC Controllers to CPM and Time-Optimal Controllers

To evaluate the operation of the presented FCDC controllers compared with other known controllers, additional simulations of CPM controller and time-optimal controller have been conducted for the same converter's parameters. The simulations exhibit the advantages of the FCDC controllers over existing controllers in terms of output voltage deviation, peak inductor current, and total transient time, all for the same converter settings.

TABLE I
COMPARISON OF CONTROLLERS' RESPONSE TO A 2.5 A LOADING TRANSIENT

	Voltage deviation	Peak current	Settling time
Voltage-deviation constrained controller	1.1V	13.4A	77 μ s
Current-deviation constrained controller	1.4V	10.1A	190 μ s
Voltage and current deviations constrained controller	1.1V	10.1A	240 μ s
Peak current programmed-mode (CPM) controller	2.2V	10.8A	900 μ s
Time-optimal controller	2.25V	16.1A	40 μ s

Simulation of a CPM controller with optimized compensation network (PI) response to a 2.5 A loading transient is depicted in Fig. 10. As can be observed, the output voltage undershoot is 2.2 V, compared with 1.4 or 1.1 V undershoot of the FCDC controllers (see Figs. 5, 7, and 9), and the transient time is at least four times longer. In addition, the peak inductor current is higher than the new steady-state inductor current, which is the peak inductor current for the current-deviation-constrained controllers.

A similar 2.5 A loading transient simulation of time-optimal controller is depicted in Fig. 11. In this case, the total transient time is significantly shorter. However, as mentioned throughout the paper, the shorter transient time comes at the cost of high voltage deviation of 2.25 V, similar to the CPM controller's case, and the peak inductor current is significantly higher.

Table I summarizes the differences of the FCDC, time-optimal control (TOC), and CPM controllers in response to an identical 2.5 A loading transient of the same converter. It can be observed that there are significant trade-offs between the objectives of voltage deviation, peak current, and settling time.

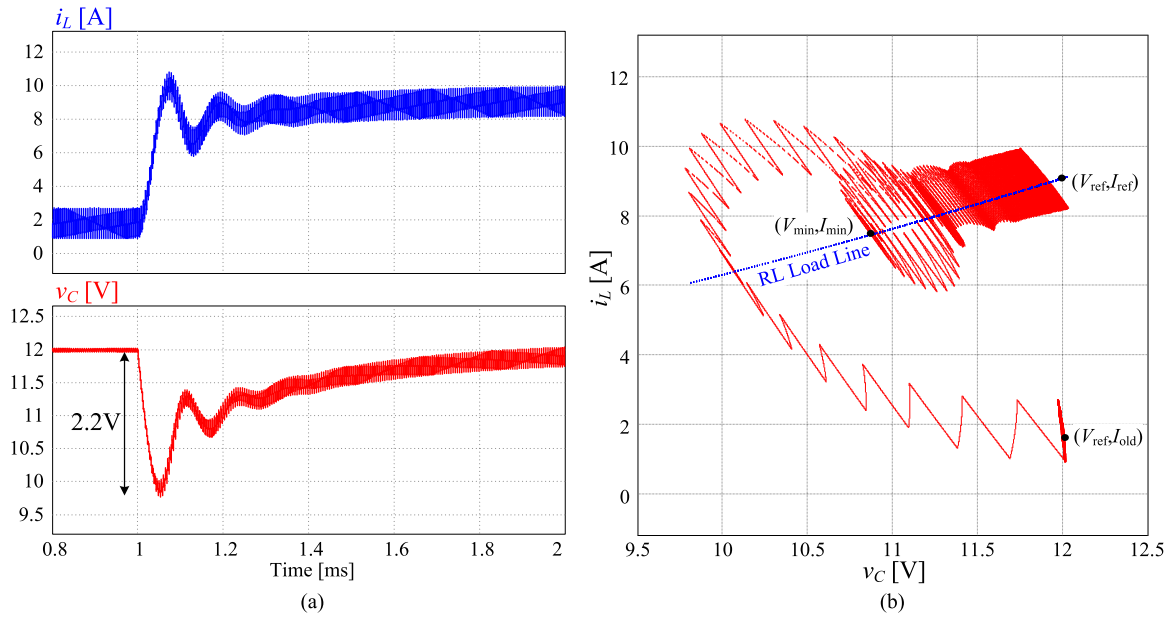


Fig. 10. Simulated response of CPM controller to a 2.5 A loading transient of a boost converter loaded by an RL. (a) Inductor current (top—blue) and output voltage (bottom—red). (b) State-plane representation of the output voltage and inductor current.

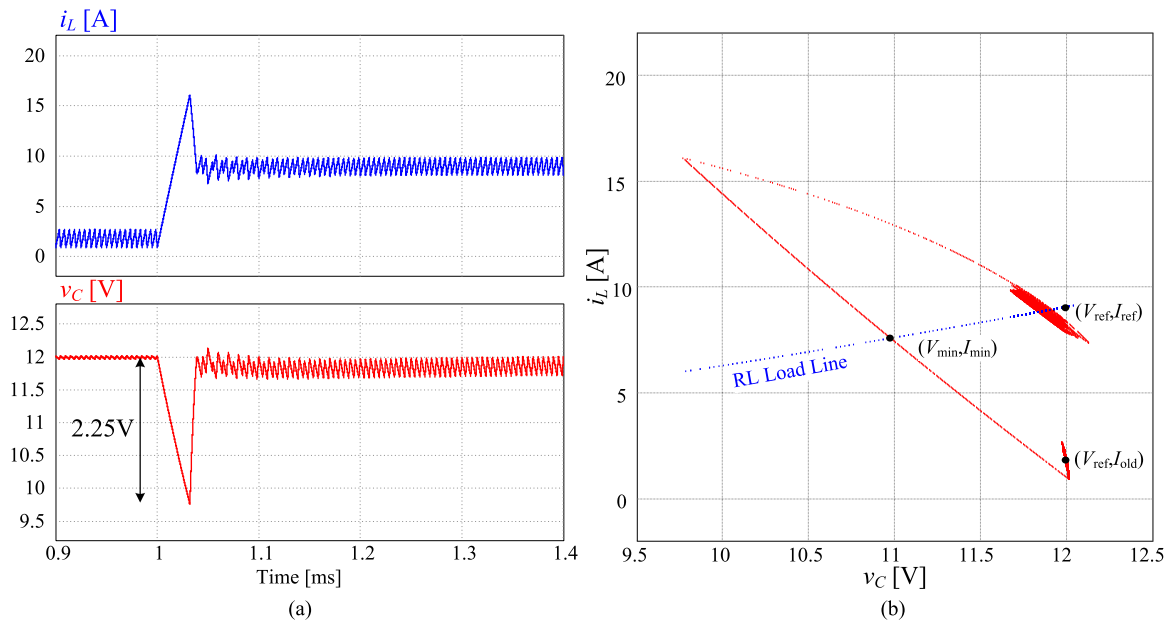


Fig. 11. Simulated response of time-optimal controller to a 2.5 A loading transient of a boost converter loaded by an RL. (a) Inductor current (top—blue) and output voltage (bottom—red). (b) State-plane representation of the output voltage and inductor current.

IV. MINIMUM EXPECTED VOLTAGE DROP

In the design of the FCDC controllers and the converter's components, information on the expected voltage drop is essential to determine feasibility of convergence [36]. In this section, the minimum possible output voltage deviation that enables the converter to converge toward the new steady-state operating point for the case of a loading transient of a boost converter is analyzed, along with the expected output voltage deviation for the current-deviation-constrained controller.

The definitions made for the analysis are as follows: the minimum output voltage deviation point V_{\min} is the upper limit for V_{th} , i.e., $V_{\text{th}} < V_{\min}$ must hold in order to converge toward the steady-state operating point [10]. The lower limit of V_{th} is $V_{\text{th,TOC}}$, where $V_{\text{th,TOC}}$ is the minimum output voltage that is obtained by a time-optimal controller. Setting V_{th} further lower than $V_{\text{th,TOC}}$ results in a voltage overshoot once the voltage has recovered due to overcharging of the inductor [7].

The extraction of V_{\min} is carried out by examination of the converter's state trajectories and the load line [15]. Exemplified

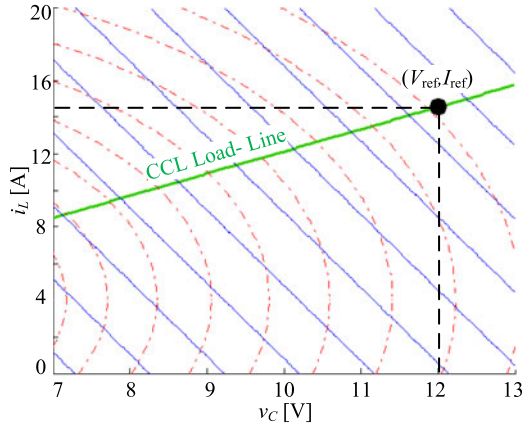


Fig. 12. ON and OFF states trajectories and the load line of a boost converter loaded by a CCL.

on a boost converter, the state-plane trajectories and the load line for the case when loaded by a constant current load (CCL) I_o can be extracted from the set of differential equations:

$$\begin{aligned} \text{on} &: \frac{dv_C}{dt} = -\frac{I_o}{C}, \quad \frac{di_L}{dt} = \frac{V_{in}}{L} \\ \text{off} &: \frac{dv_C}{dt} = \frac{i_L - I_o}{C}, \quad \frac{di_L}{dt} = \frac{V_{in} - v_C}{L} \end{aligned} \quad (7)$$

where C is the output capacitance, L is the inductor value, v_C is the output voltage, and i_L is the inductor current. Using any of the three methods presented in [15] to obtain the load line, it is given by

$$LL_{CCL}(v_C, i_L) = \left\{ v_C, i_L : i_L = \frac{I_o}{V_{in}} v_C \right\} \quad (8)$$

and its state plane is depicted in Fig. 12. For this type of load, the ON trajectories are straight lines and the OFF trajectories are ellipses.

In a similar manner for an RL case, the state-plane trajectories of a boost converter are derived from

$$\begin{aligned} \text{on} &: \frac{dv_C}{dt} = -\frac{v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{in}}{L} \\ \text{off} &: \frac{dv_C}{dt} = \frac{Ri_L - v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{in} - v_C}{L} \end{aligned} \quad (9)$$

where R is the load resistance, and the load line can be expressed as

$$LL_{RL}(v_C, i_L) = \left\{ v_C, i_L : i_L = \frac{v_C^2}{RV_{in}} \right\}. \quad (10)$$

For this case, the ON trajectories are exponential and the OFF trajectories are spirals instead of ellipses. However, within the region of interest for a boost converter where $v_C > V_{in}$ and $i_L > 0$, the OFF trajectories can be well-approximated to ellipses, under the assumption of small output voltage deviation [31], which coincide with the FCDC controllers' operation. As demonstrated in Fig. 13, for the same output power, the load line of the CCL case is higher in i_L than the load line of the RL case for $v_C < V_{ref}$, which is the relevant region for loading transients.

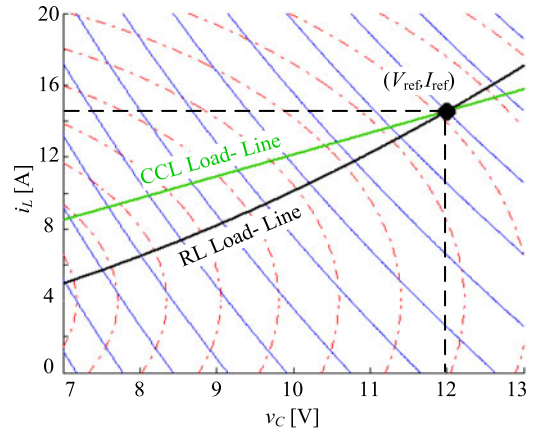


Fig. 13. ON and OFF states trajectories and load line (black) of a boost converter loaded by an RL and the CCL load line from Fig. 12 (green).

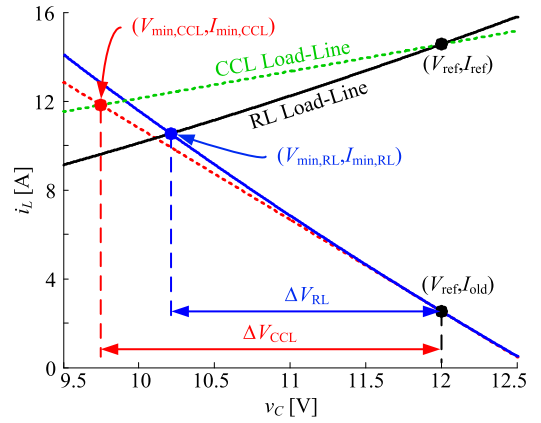


Fig. 14. First ON state trajectories and the load-line intersections for CCL case (dotted) and RL case (solid).

The smallest possible output voltage deviation is extracted from the intersection on the state plane of the ON state trajectory, starting at the previous steady-state point, with the load line. As shown in Fig. 14, the minimum voltage deviation varies with the load type for a load transient of the same magnitude. As can be observed, the minimum voltage deviation point, which is the intersection point of the RL case ($V_{min,RL}$, $I_{min,RL}$), occurs at higher voltage and lower current compared to the intersection of the CCL case ($V_{min,CCL}$, $I_{min,CCL}$), i.e., $\Delta V_{RL} < \Delta V_{CCL}$ and $I_{min,CCL} > I_{min,RL}$. The ON state trajectory for the CCL case is given by

$$i_L = I_{old} - \frac{CV_{in}}{LI_o} (v_C - V_{ref}) \quad (11)$$

where I_o is the new load current, and for the RL case is given by

$$i_L = I_{old} - \frac{RCV_{in}}{L} \ln\left(\frac{v_C}{V_{ref}}\right) \quad (12)$$

and R is the new load resistance.

For an arbitrary operating point (V_{ref} , I_{old}), $V_{min,CCL}$ can be calculated by solving (8) and (11), and is given by

$$V_{min,CCL} = \frac{CV_{in}^2 V_{ref} + LV_{in} I_o I_{old}}{LI_o^2 + CV_{in}^2} \quad (13)$$

where the inductor current at this point is

$$I_{min,CCL} = \frac{I_o V_{min,CCL}}{V_{in}}. \quad (14)$$

For the RL case, the exact solution for the minimum output voltage deviation ΔV_{RL} can only be calculated using numerical methods due to the complexity of the trajectories. By approximating the first ON state trajectory to a straight line, under the assumption that the voltage deviation ΔV_{RL} is relatively small [32], a solution exists and $V_{min,RL}$ and $I_{min,RL}$ are given by

$$V_{min,RL} = \frac{CR^2 V_{in}^2 V_{ref} + LRV_{in} V_{ref} I_{old}}{LV_{ref}^2 + CR^2 V_{in}^2}, \quad (15)$$

$$I_{min,RL} = \frac{V_{min,RL}^2}{RV_{in}}. \quad (16)$$

It should be noted that if (13) and (15) are to be calculated using a low-cost microcontroller in real time, they can be approximated using the approximations detailed in [12].

For the case of the current-deviation-constrained controller, calculation of point where the output voltage is minimal during to transient-mode operation, $V_{min,current}$, is straightforward. The point $V_{min,current}$ can be calculated by equating (11) and (12) to I_{ref} , for the CCL case and RL case, respectively. These two points can be expressed as

$$V_{min,current,CCL} = V_{ref} - \frac{LI_o (I_{ref} - I_{old})}{CV_{in}} \quad (17)$$

$$V_{min,current,RL} = V_{ref} \exp\left(-\frac{L(I_{ref} - I_{old})}{RCV_{in}}\right). \quad (18)$$

V. EXPANSION TO OTHER TOPOLOGIES AND PRACTICAL IMPLEMENTATION

A. Load Current Estimation and Transient Detection

The implementation of the self-tuning estimator of Fig. 15 is based on a look-up-tables (LUTs) and on the estimation of the load current (and from it, the new steady-state inductor current I_{ref}) through a comparison with a measurement of the known current value, named the unity current. The LUT of the estimator is populated during the converter start-up. Over that period, the LUT's entries are stored, i.e., current and voltage threshold values are created, from the measurement of the output voltage derivative during the ON-time of switch M_1 . After the writing of the values in the tables is completed, the output voltage deviation is used as an address (input in of Fig. 15) to determine the LUT's outputs, i.e., V_{th} and I_{th} values.

The process of the output load estimation is shown in Figs. 15–17. Upon the converter power up a generic LUT based on the calculation of (13) is assigned (see Fig. 16). The known current of the protective resistor R_{bld} (also known as bleeding resistor), named unit current I_{unit} , is used for the system calibration and for updating the LUT to comply with the measured values in the system. During this time, the load is disconnected

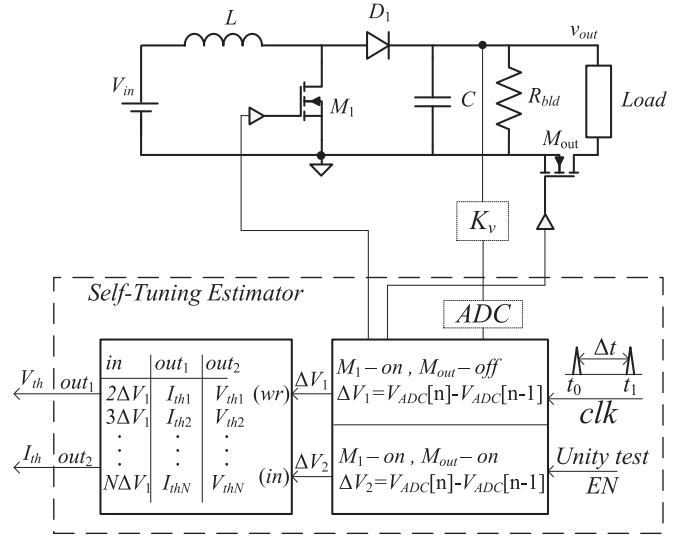


Fig. 15. Block diagram of the self-tuning estimator.

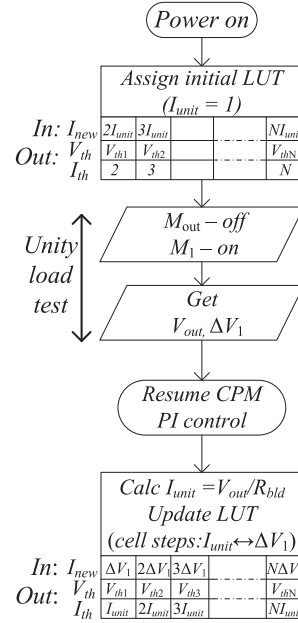


Fig. 16. Flowchart of the unity load test and the LUT population procedure.

from the output of the converter, i.e., switch M_{out} is turned OFF, and the value ΔV_1 , which is proportional to I_{unit} , is measured as

$$\Delta V_1 = v_{ADC}[n] - v_{ADC}[n-1] = \frac{V_{ref}}{R_{bld}} \frac{\Delta t}{C} = I_{unit} \frac{\Delta t}{C} \quad (19)$$

where Δt is the sampling interval, $v_{ADC}[n]$ is the current value of the analog-to-digital converter (ADC) output and $v_{ADC}[n-1]$ the ADC value from the previous sampling cycle. The value ΔV_1 is used to populate the LUT with I_{th} and V_{th} values for the full range of allowable output voltage deviations, i.e., for the initial write process. It can be seen that the value ΔV_1 uniquely determines the relation between the output capacitor voltage deviation and the load current and, therefore, I_{th} values. As shown in Figs. 15 and 16, the threshold values of the inductor

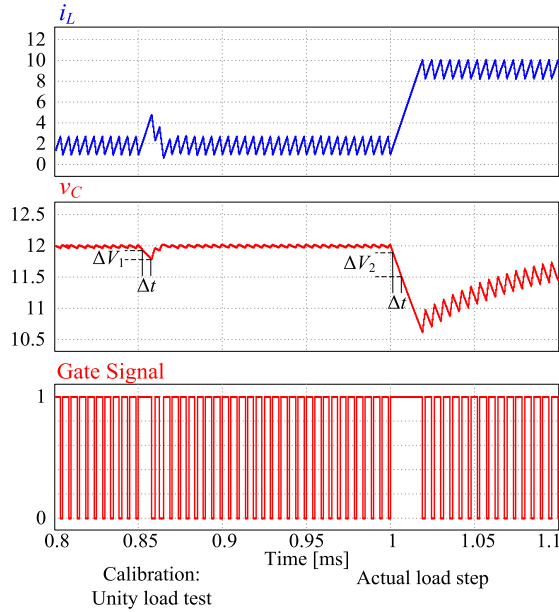


Fig. 17. Calibration process using the unity load test for load and inductor current, followed by a loading transient.

current are written in the table as scaled steps of the measured unit current value. This implies that once the LUT has been populated, V_{th} and I_{th} values will be determined based on the new load current only which eliminates the dependence of the controller on the information of the previous loading conditions (i.e., I_{out_old}). For slow and/or light load transients, i.e., smaller than the quantization steps of the current estimator, the output voltage variations are relatively small and the transient logic is not activated. For those cases, the conventional PI compensator of 0 is sufficiently fast to perform regulation of the output voltage and keep the output voltage deviation under the maximum allowable value. It should be noted that in the LUT population process it is assumed that the information about $D' = 1 - D$ (D is the duty ratio), needed for the calculations of both set of table entries, is known, since

$$I_{ref} = \frac{I_{out_new}}{D'}. \quad (20)$$

The value of D' can be extracted from the feedback loop using a fairly simple counter [11].

Upon the power up of the converter and population of the LUT are completed, the switch M_{out} , usually existing in the applications of interest, is turned ON. During the remaining portion of the converter operation, the LUT is used to produce I_{th} and V_{th} during transient events. As shown in Fig. 15, the input to the table is now the voltage deviation ΔV_2 measured during the ON-time of the main switch M_1 . During a transient event, the load current I_{out_new} is estimated as

$$\frac{\Delta V_2}{\Delta V_1} = \frac{I_{new} + I_{unit}}{I_{unit}} = I_{out_new} \quad (21)$$

and the corresponding values of the threshold current and the voltage are produced by the LUT. These values are then passed to the FCDC controller that is in use. It should be noted that using this approach any output voltage noise is filtered by both the ADC sampling and by the division in (21).

TABLE II
TRANSFORMATIONS OF THE SYSTEM'S PARAMETERS OF SECOND-ORDER
INDIRECT ENERGY TRANSFER CONVERTERS

	Constant Current Load	Resistive Load
Non-inverting buck-boost	$v'_C = v_C + V_{in}$ $i'_L = i_L$ $V'_{in} = V_{in}$ $I'_o = I_o$	$v'_C = v_C + V_{in}$ $i'_L = i_L$ $V'_{in} = V_{in}$ $R' = \frac{v'_C}{v'_C - V_{in}} R$
Buck-boost	$v'_C = V_{in} - v_C$ $i'_L = i_L$ $V'_{in} = V_{in}$ $I'_o = I_o$	$v'_C = V_{in} - v_C$ $i'_L = i_L$ $V'_{in} = V_{in}$ $R' = \frac{v'_C}{v'_C - V_{in}} R$
Flyback	$v'_C = v_C + nV_{in}$ $i'_L = i_L$ $V'_{in} = nV_{in}$ $I'_o = I_o$	$v'_C = v_C + nV_{in}$ $i'_L = i_L$ $V'_{in} = nV_{in}$ $R' = \frac{v'_C}{v'_C - nV_{in}} R$

The unity load test also allows for the identification of the output capacitance and subsequent population of the LUT with V_{th} values (based on the output voltage measurement), in accordance with (13) or (15). Based on the unity load test, the output capacitance can be estimated by

$$C = \frac{V_{ref}}{R_{bld}} \frac{\Delta t}{\Delta V_1}. \quad (22)$$

The comparison of the successive output voltage samples is also used for transient detection, by comparing the sensed output voltage to predefined thresholds values, above and below the output voltage's reference value, in a similar manner to the one presented in [38] and [39]. When the output voltage variations are within the thresholds, the steady state's CPM controller is active, and when the output voltage crosses one of the thresholds, transient is detected. Such method introduces a maximum delay in a transient detection that equals one sampling period. A relatively slow sampling rate may cause delayed transient detection and as a result a delay in turning the transistor ON and increased voltage drop. As a consequence, an error in the voltage threshold detection could occur. This effect is dependent on the load value and the sampling rate. The worst case would be that the sampling is delayed by one sampling cycle (switching period). The additional voltage drop due to delay V_{delay} can be expressed as

$$V_{delay} = \frac{I_{out_new}}{C f_s} \quad (23)$$

where f_s is the switching frequency that equals the sampling frequency. I_{out_new} and C can be estimated by the above-mentioned procedure. For the cases when the delay caused by this detection method is not acceptable, a simple dedicated transient detection circuit, similar to the solution present in [11], can be used.

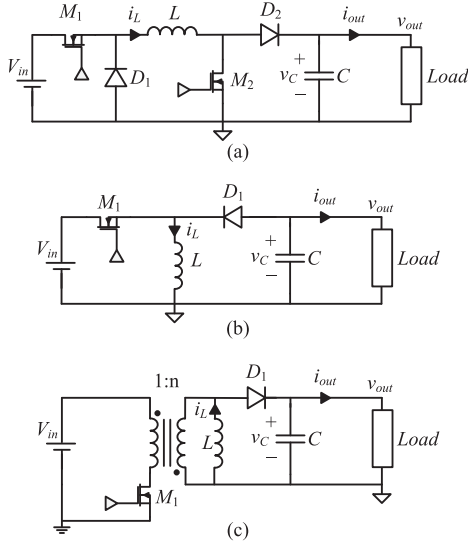


Fig. 18. Second-order indirect energy transfer converters: (a) noninverting buck-boost converter. (b) Buck-boost converter. (c) Flyback converter.

In case the output capacitor has a significant equivalent series resistance (ESR), the voltage threshold V_{th} should be corrected according to the load change and shifted. Given the ESR, its effect may be added as a constant to V_{th} , that is

$$V_{th + ESR} = V_{th} - I_{out, new} ESR. \quad (24)$$

B. Expansion to Other Second-Order Indirect Energy Transfer Converters

By inspection of the state plane for indirect energy transfer converters with two reactive components, high resemblance is found in their ON and OFF state trajectories to a boost converter. For example, in the case of an NIBB converter, the ON state trajectories are exactly matched with the ones in a boost converter and the OFF state trajectories of the NIBB converter are shifted left by a constant value of V_{in} (for the same converter's parameters $-L, C, V_{in}, V_o, P_{out}$). Using this insight, the presented controllers can be used for other converters as well, by applying a simple transformation of the system's parameters and the state variables (v_C, i_L), with respect to the input voltage V_{in} and the load status (I_o for a CCL case and R for an RL case). The core concept is to transform $(v_C, i_L, V_{in}, I_o, R)$ (as defined in Fig. 18) into $(v'_C, i'_L, V'_{in}, I'_o, R')$ and then analyze the converter as if it is a boost converter with the provided stability analysis. The transformation is detailed here for the NIBB converter, and the transformations for other converters are presented in Table II.

The state equations of NIBB converter loaded by an RL are

$$\begin{aligned} \text{on} &: \frac{dv_C}{dt} = -\frac{v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{in}}{L} \\ \text{off} &: \frac{dv_C}{dt} = \frac{Ri_L - v_C}{RC}, \quad \frac{di_L}{dt} = -\frac{v_C}{L} \end{aligned} \quad (25)$$

and the required transformation is as follows:

$$v'_C = v_C + V_{in}, \quad i'_L = i_L, \quad V'_{in} = V_{in}, \quad R' = \frac{v'_C}{v'_C - V_{in}} R. \quad (26)$$

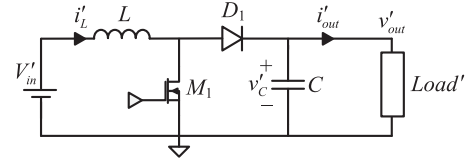


Fig. 19. Boost converter represented with transformed parameters and state variables of other indirect energy transfer converters.

Substituting (26) into (25) yields the state equations of a boost converter loaded by an RL as depicted in Fig. 19:

$$\begin{aligned} \text{on} &: \frac{dv'_C}{dt} = -\frac{v'_C}{RC}, \quad \frac{di'_L}{dt} = \frac{V'_{in}}{L} \\ \text{off} &: \frac{dv'_C}{dt} = \frac{Ri'_L - v'_C}{RC}, \quad \frac{di'_L}{dt} = \frac{V'_{in} - v'_C}{L}. \end{aligned} \quad (27)$$

In a similar manner, the transformations required for a CCL case are

$$v'_C = v_C + V_{in}, \quad i'_L = i_L, \quad V'_{in} = V_{in}, \quad I'_o = I_o. \quad (28)$$

As delineated by the derivation concept, the resultant state equations represent a boost converter with the structure as shown in Fig. 19, and the presented controllers can be applied on.

C. Switching Frequency During Transients

During load transients the three FCDC controllers use a sliding-mode controller to control the state variables in the desired pattern. During this sliding phase, the switching frequency is determined by the hysteresis band of the sliding-mode controller, and not by the steady-state PWM frequency. Therefore, for proper converter's design it is needed to evaluate the switching frequency during the load transients.

The FCDC controllers use two sliding-mode controllers: voltage and current controllers. The voltage controller is used in the voltage-deviation-constrained controller [see (2)], the current controller is used in the current-deviation-constrained controller [see (4)], and the voltage- and current-deviation-constrained controller uses both voltage controller and current controller.

The maximum switching frequency when using the voltage controller with a voltage hysteresis band $\Delta\sigma_v$ occurs when the state variables are proximate to the (V_{min}, I_{min}) point, on the load line, as depicted in Fig. 20(a). The ON-time is given by

$$t_{on, v} = \frac{C\Delta\sigma_v}{I_o} \quad (29)$$

and the OFF-time is given by

$$t_{off, v} = \frac{C\Delta\sigma_v}{I_o - I_{min}} \quad (30)$$

and therefore the maximum switching frequency for the voltage controller $f_{s, v}$ is

$$f_{s, v} = \frac{1}{t_{on, v} + t_{off, v}} = \frac{1}{C\Delta\sigma_v \left(\frac{1}{I_o} + \frac{1}{I_{min} - I_o} \right)}. \quad (31)$$

For the current controller, the current hysteresis band $\Delta\sigma_i$ sets the switching frequency. Here, the maximum switching frequency occurs when the state variables are proximate to the

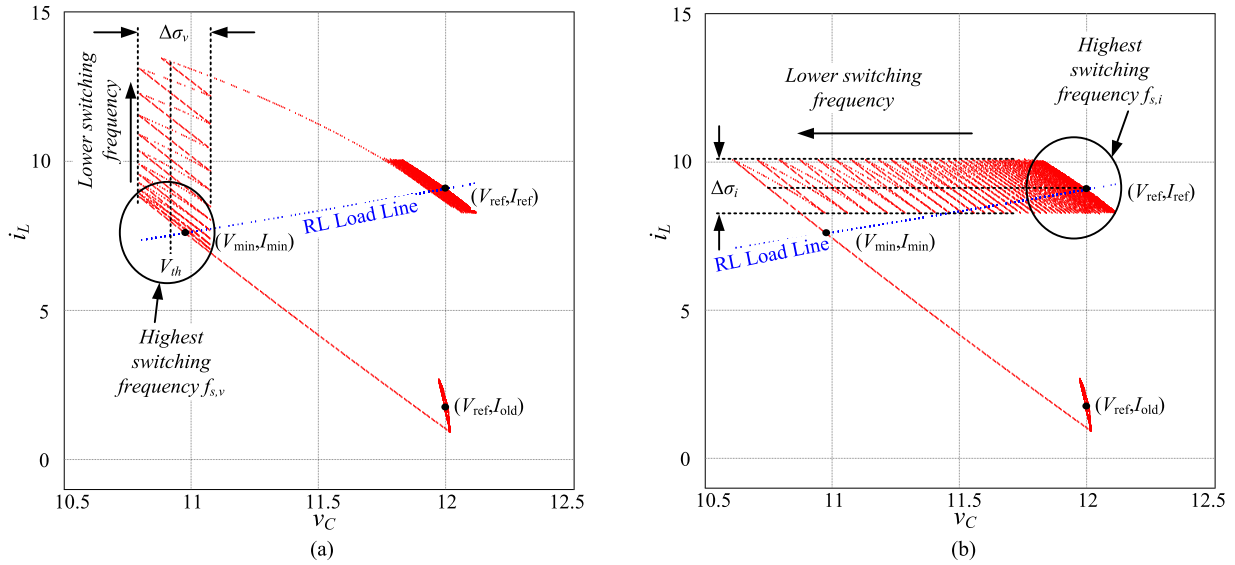


Fig. 20. Maximum switching frequency areas during the sliding phases of the FCDC controllers: (a) voltage controller and (b) current controller.

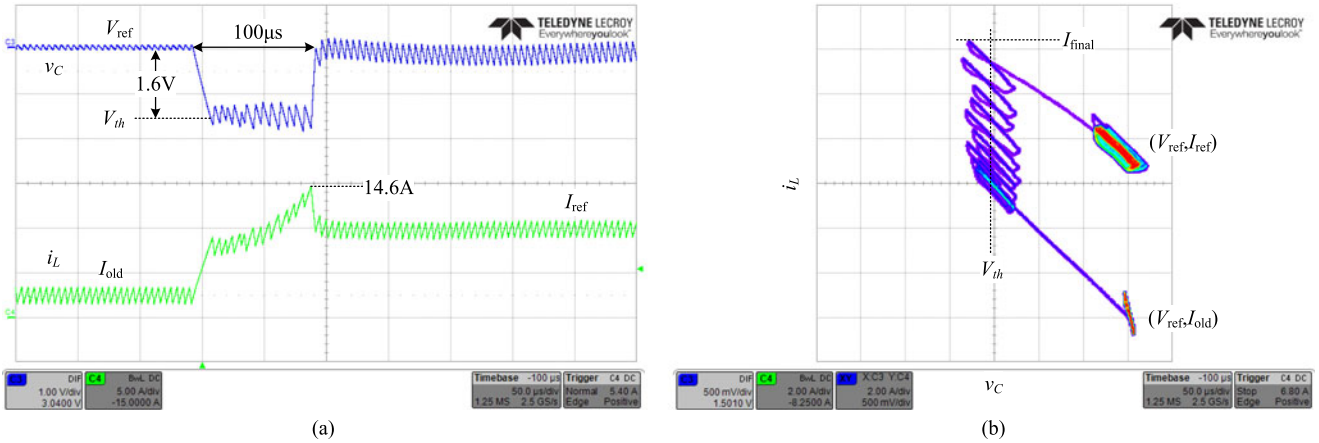


Fig. 21. Boost converter's response and state-plane representation to a 0.5–2.4 A loading transient using the voltage-deviation-constrained controller. (a) Output voltage (top—blue) 1 V/div ac coupled, inductor current (bottom—green) 5 A/div, time scale 50 μ s/div. (b) State-plane representation of inductor current (vertical axis—2 A/div) and output voltage (horizontal axis—0.5 V/div).

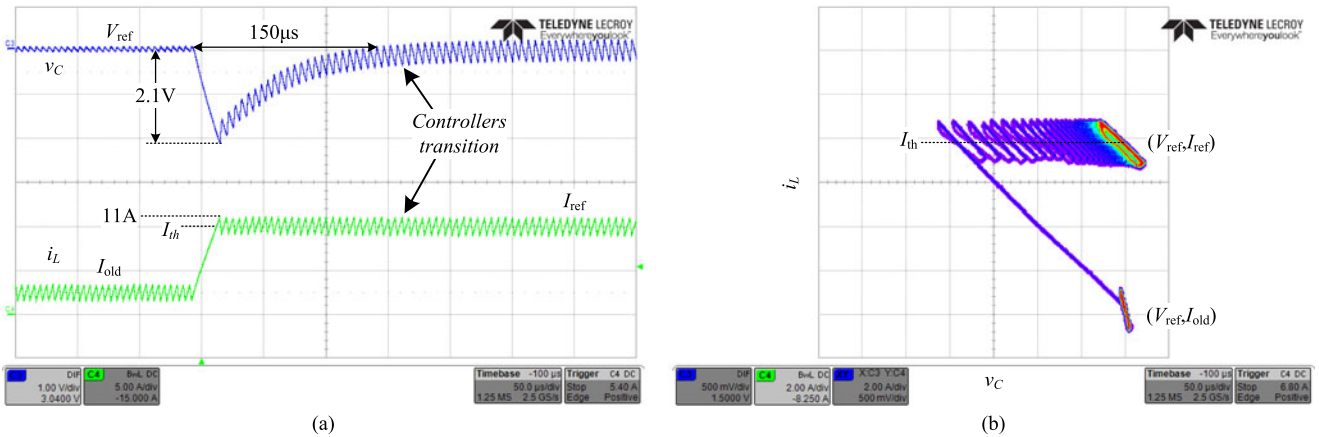


Fig. 22. Boost converter's response and state-plane representation to a 0.5–2.4 A loading transient using the current-deviation-constrained controller. (a) Output voltage (top—blue) 1 V/div ac coupled, inductor current (bottom—green) 5 A/div, time scale 50 μ s/div. (b) State-plane representation of inductor current (vertical axis—2 A/div) and output voltage (horizontal axis—0.5 V/div).

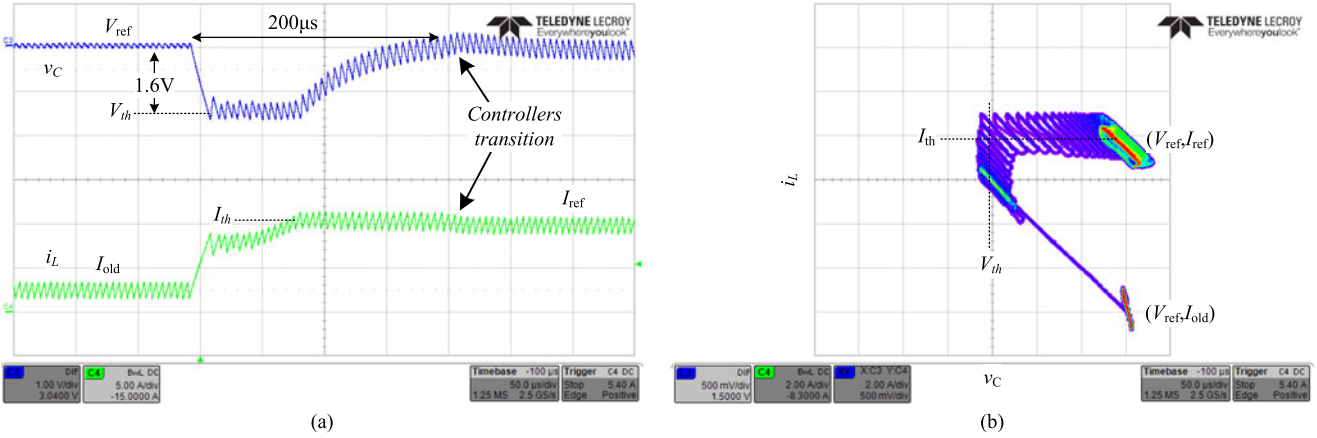


Fig. 23. Boost converter's response and state-plane representation to a 0.5–2.4 A loading transient using the voltage- and current-deviation-constrained controller. (a) Output voltage (top—blue) 1 V/div ac coupled, inductor current (bottom—green) 5 A/div, time scale 50 μ s/div. (b) State-plane representation of inductor current (vertical axis—2 A/div) and output voltage (horizontal axis—0.5 V/div).

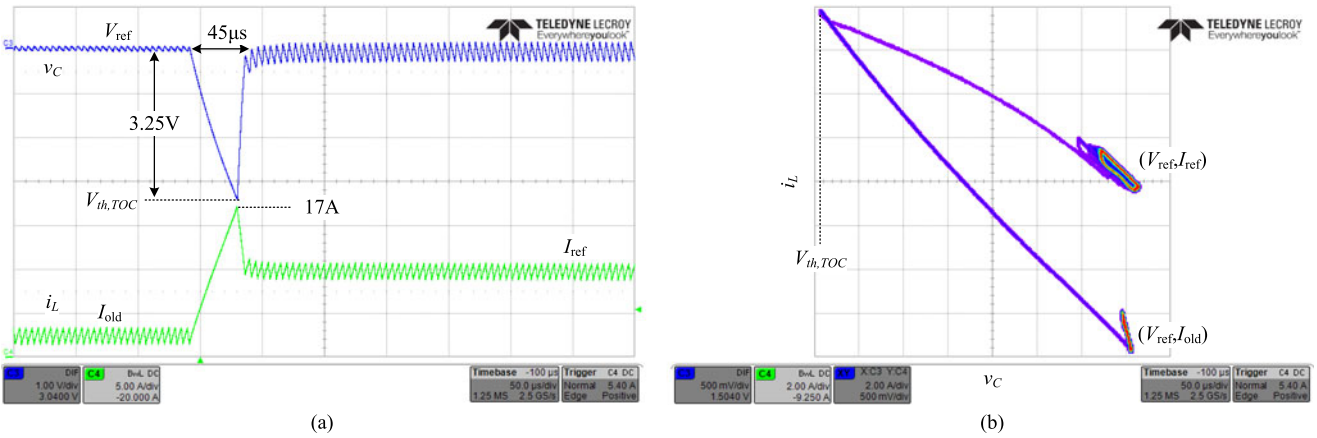


Fig. 24. Boost converter's response and state-plane representation to a 0.5–2.4 A loading transient using time-optimal controller. (a) Output voltage (top—blue) 1 V/div ac coupled, inductor current (bottom—green) 5 A/div, time scale 50 μ s/div. (b) State-plane representation of inductor current (vertical axis—2 A/div) and output voltage (horizontal axis—0.5 V/div).

steady-state operating point, as depicted in Fig. 20(b). The ON-time is

$$t_{on,i} = \frac{L\Delta\sigma_i}{V_{in}} \quad (32)$$

and the off-time is

$$t_{off,i} = \frac{L\Delta\sigma_i}{V_{ref} - V_{in}}. \quad (33)$$

The maximum switching frequency $f_{s,i}$ is given by

$$f_{s,i} = \frac{1}{t_{on,i} + t_{off,i}} = \frac{1}{L\Delta\sigma_i \left(\frac{1}{V_{in}} + \frac{1}{V_{ref} - V_{in}} \right)}. \quad (34)$$

VI. EXPERIMENTAL VERIFICATION

To validate the operation of the FCDC controllers, a 30 W 3.3 V-to-12 V boost converter was built and tested, using a 6.8 μ H inductor, 30 μ F output capacitance, and operating at a switching frequency of 200 kHz. The converter was loaded by an RL type. The FCDC controllers were realized on an all-digital field-

programmable gate array (FPGA) platform [40] including high-performance ADC and digital pulse-width modulator (DPWM) [41] with the addition of one voltage hysteresis comparator.

A dynamic response of the FCDC controllers and time-optimal controller for a loading transient of 0.5–2.4 A is depicted in Figs. 21–24. 0 shows the dynamic response of voltage deviation-constrained controller when V_{th} is set to be slightly lower than V_{min} . With this controller the output voltage deviation is 1.6 V, the peak inductor current is 14.6 A, and the total transient time is 100 μ s. The dynamic response of the current-deviation-constrained controller is shown in Fig. 22 and results in an output voltage deviation of 2.1 V, peak inductor current of 11 A that equals the new steady-state operating point's peak inductor current, i.e., with no current overshoot, and the total transient time is 150 μ s. Fig. 23 shows voltage- and current-deviation-constrained controller. Using this controller, the output voltage deviation sums to be 1.6 V, the peak inductor current is 11 A (equals the new steady-state peak inductor current), and the total transient time is 200 μ s. The dynamic response of the system using a time-optimal controller is depicted in Fig. 24. As can be observed, a faster response with

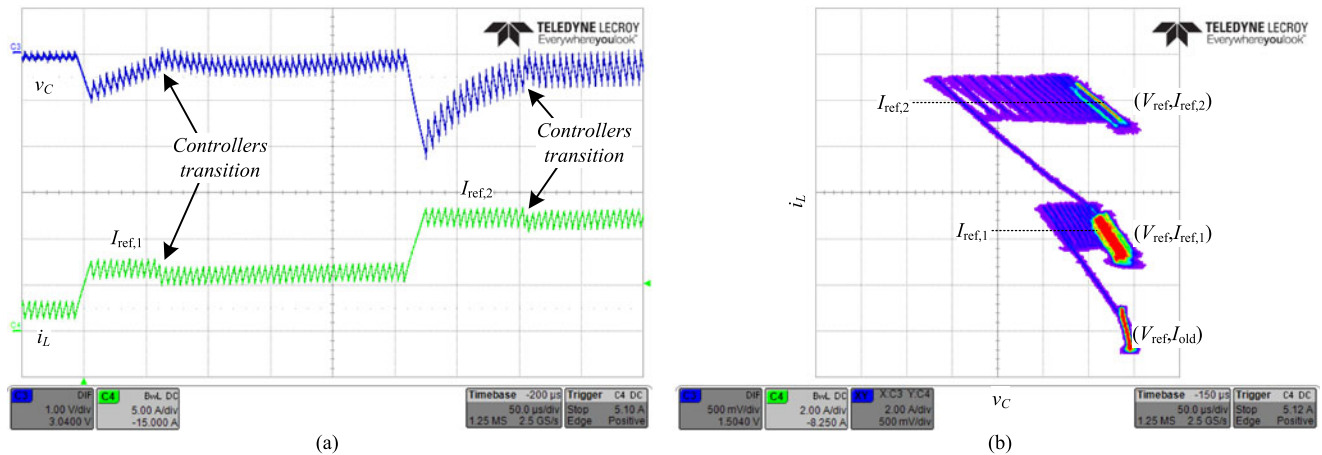


Fig. 25. Boost converter's response and state-plane representation to a 0.5–1.5–3 A consecutive loading transients using the current-deviation-constrained controller. (a) Output voltage (top—blue) 1 V/div ac coupled, inductor current (bottom—green) 5 A/div, time scale 50 μ s/div. (b) State-plane representation of inductor current (vertical axis—2 A/div) and output voltage (horizontal axis—0.5 V/div).

total time of 45 μ s is achieved at the cost of significantly larger output voltage deviation of 3.25 V and high 17 A peak inductor current. To demonstrate the FCDC controllers' automated operation, Fig. 25 shows consecutive loading transients with different magnitudes. As can be observed, the consecutive transients result in different output voltage deviations, but converge to steady state at the end of the transient-mode operation. Also shown in Figs. 22, 23, and 25 are the smooth transitions between the steady-state and transient-mode controllers at the end of transient due to the small current error, as predicted in (5).

VII. CONCLUSION

A fast convergence within constrained output voltage and peak inductor current deviations hybrid controllers for boost-type converters have been presented in this study. The controllers incorporate a steady-state peak CPM controller for steady-state operation and a nonlinear transient-mode controller for load transients. A state-plane and time analysis has been carried out, followed by the controllers' design that is based on the theoretical investigation. The transient-mode controllers implementation is straightforward and simple, consisting of a three-step or two-step transient recovery process, and requires a negligible total of one additional hysteresis comparator. An analysis of the minimum possible output voltage deviation has been presented, providing the required margins for the design of the controllers and the expected voltage drop.

Experimental results of a 30 W 3.3 V-to-12 V boost converter prototype are provided. For loading transients, compared to time-optimal controller, the FCDC controllers produce up to 100% lower output voltage deviation and up to 35% lower peak current, which enables volume reduction of the reactive components, while maintaining short total transient time.

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Or Kirshenboim (S'15) was born in Haifa, Israel, in 1987. He received the B.Sc. and M.Sc. degrees in electrical and computer engineering in 2013 and 2015, respectively, from the Ben-Gurion University of the Negev, Beer-Sheva, Israel, where he is currently working toward the Ph.D. degree in electrical and computer engineering.

His current research interests include digital, non-linear and smart control methods for switch-mode power supply, hybrid voltage regulation solutions, high-voltage conversion ratio converter topologies, pulsed power applications, and batteries balancing topologies.



Mor Mordechai Peretz (S'05–M'12) was born in Beer-Sheva, Israel, in 1979. He received the B.Tech. degree in electrical engineering from the Negev Academic College of Engineering, Beer-Sheva, Israel, in 2003, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the Ben-Gurion University, Negev, Israel, in 2005 and 2010, respectively.

From 2010 to 2012, he was a Postdoctoral Fellow in the Laboratory for Power Management and Integrated SMPS, University of Toronto, Toronto, ON, Canada. In 2012, he joined the Department of Electrical and Computer Engineering, Ben-Gurion University, where he is currently the Director of the Center for Power Electronics and Mixed-Signal IC. His research interests include digital and smart control methods for efficient energy processing, switch-mode power supply (SMPS) miniaturization, mixed-signal IC design of SMPS, modeling and computer-aided design, applications of non-linear magnetics, and renewable energy systems.

Dr. Peretz serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.