Optimal Design of a Voltage Regulator Based on Gyrator Switched-Resonator Converter IC

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***Abstract*— This paper details efficiency analysis and characteristics of a gyrator switched-resonator converter (GSwRC) IC. Followed by an efficiency analysis, this paper introduces an optimized size-efficiency design procedure for IC realization of the converter. In area-sensitive applications, the optimization method combined with the converter's benefits presents an attractive approach for power delivery in point-of-load applications. To verify the analytical framework, two sets of bridge-type GSwRCs prototypes have been evaluated. One is an on-chip bridge GSwRC that has been fabricated in 0.18-μm 5-V CMOS process, according to the principles detailed in this paper, and verified through postlayout analysis and experimental measurements of the fabricated IC. The second prototype is a discrete GSwRC that is used for further validation of the theoretical framework. In addition, the analysis has been verified through a design example of a multiphase resonant switched-capacitor converter. The fabricated IC prototype operation is demonstrated with 1.5 A, delivering up to 2.25 W from 3-V input voltage, with peak efficiency at 85%. A fully monolithic controller to regulate the output voltage is described and implemented on-chip by an automated synthesis process and place-and-route tools.**

***Index Terms*— IC, on-chip voltage regulator, optimization, power supply on-chip, resonant switched-capacitor converter (SCC), size efficiency, switched-resonator converters, zero-current switching (ZCS).**

I. Introduction

PRESENT-DAY microprocessors and other high-performance ICs require an accurate, dynamically scalable supply voltage in the range of 1 V and total current of 10s A/chip [1]–[4]. In addition to the tight voltage regulation requirements, the area-efficiency factor of the point-of-load (PoL) converter is of key importance to ensure the desired performance and to be considered reasonable for commercialization. Improvements of the area-efficiency factor of the PoL converter may enable 3-D power delivery architectures [5]–[7] where the converter is integrated with the load, significantly enhancing dynamic power delivery capabilities.

Conventional approaches to reduce the total volume of voltage regulator modules (VRMs) are carried out by increasing the operating frequency to the 100-MHz range [8]–[11]. By doing so, the integration of magnetics and the decoupling capacitors are more convenient. However, the efficiency and total power that can be processed are limited by the dynamic power consumption at high frequencies. Another area saving concept can be facilitated by resonant-mode converters [12]–[18]. Thanks to their soft-switching features, the efficiency of the converters is not compromised when operating at high frequency.

Switched-capacitor converter (SCC) technology has demonstrated superior power density over switched-inductor converters (SICs) [19]–[24]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited [25]–[29]. A solution that overcomes these challenges has been presented in [30]. There, an additional switching state has been added to balance the charge difference between the input and output rather than introducing losses for voltage regulation, creating a gyrator switched-resonator converter (GSwRC) that disengages the efficiency of the system from the voltage gain. Utilizing this approach allows on-chip integration and operation at reasonable frequencies in the range of 10 MHz without sacrificing performance, further improving the power conversion efficiency.

The classical design of the power processing components for VRMs considers the converter's mode of operation and especially the conversion ratio to optimize the peak efficiency point to the target parameters; for example, in a high conversion ratio buck VRM, the lower transistor of the synchronous rectifier is dominant and would be much larger in size than the top transistor to assure optimal efficiency at the target voltage. In resonant SCC technology, which the GSwRC is based on, using existing design tools, symmetrical switch resistances are assumed for all switching states [31]–[36]. While appropriate for most discrete-component realizations, in area-sensitive applications (and in particular IC implementations), the efficiency characteristics of a GSwRC as a voltage regulator will be on par to other switched-inductor-based candidates, since the converter is not optimized to the target operation [37]. To overcome this, the resistance per switch should be assigned to minimize the die size at the target efficiency. Since the losses that are associated with the

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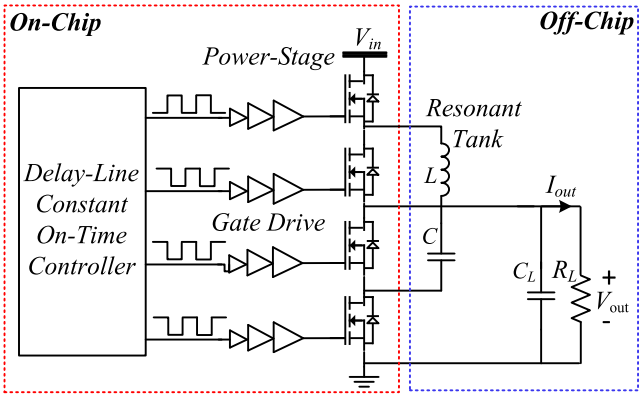


Fig. 1. Circuit diagram of a bridge gyrator-mode switched-resonator converter.

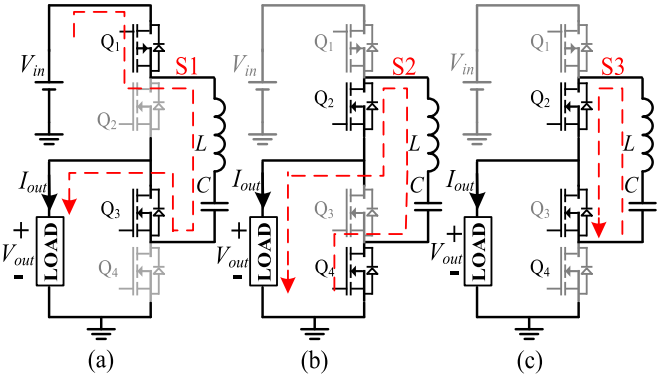


Fig. 2. Bridge GSwRC configuration and operation principle: (a) charge, (b) discharge, and (c) charge balance.

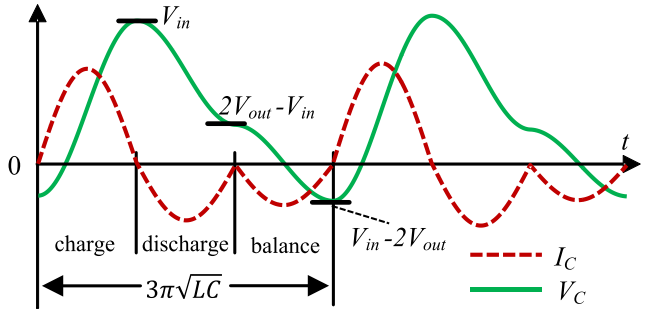


Fig. 3. Typical waveforms for the bridge-type GSwRC.

process, capacitance, and other load-independent losses are fixed per area, and are not affected by partitioning or different segmentations of the transistors within a confined area, the switch's resistance is the primary variable that affects the converter's efficiency. It should be further noted that based on the extensive analysis of the GSwRC and its family derivatives that has been carried out in [30] and [37], for the topology and from a full regulator solution perspective, it has been found that the GSwRC family is superior over SICs in terms of overall volume of the design. A significant reduction in volume in the range of one order of magnitude smaller, thanks to the utilization of very low inductance (enabling air-core or stray inductances) that can be achieved for a GSwRC-based voltage regulator. A further advantage in the context of volume-sensitive application in favor of the GSwRC family is that when regulated by simple hysteretic pulse density modulation (PDM), it features near-ideal response to both loading and unloading transients [37], [52]. This implies that the sizing of the output capacitor filter is carried out by the requirements of the steady-state voltage ripple alone, rather than the worst-case load transient and the system bandwidth (as applied in SICs). As a result, a significant reduction of the system's passives is allowed, setting the GSwRC family as an extremely attractive candidate in a vast variety of volume-sensitive applications.

The objective of this paper is to present an optimal size-efficiency design procedure for the GSwRC when operating as a voltage regulator, and to define the required sizing of the power transistors (and resonant network) based on the target operating point given a finite die size. That is, optimizing the operation of a GSwRC for prescribed die area. It is a further objective of this paper to present a fully monolithic voltage regulator based on GSwRC that is realized by simple constant on-time PDM control (Fig. 1). The new voltage regulator scheme with an optimized power converter demonstrates a reasonably sized solution at a much lower operating frequencies and requires virtually no physical inductors, which may be found beneficial for many applications and enable a smoother transition toward the 3-D power delivery approach.

The rest of this paper is organized as follows. Section II briefly surveys the GSwRC operation. Section III revises some primary guidelines for size optimization, and presents loss analysis and an optimization oriented to a GSwRC operating as voltage regulator. Generalized design procedure and design examples are delineated in Section IV. Section V describes the considerations of an on-chip implementation and a monolithic delay-line-based constant on-time controller. Experimental validation of the design procedure and GSwRC IC prototype are provided in Section VI. Finally, Section VII provides the conclusions.

II. Bridge GSwRC Principle of Operation

The GSwRC-based voltage regulator, presented in [30], has evolved from the conventional soft-switched resonant SCC configuration [12]–[18]. As in the classical bridge design of a voltage dividing SCC [19], [23], [38], [39], the topology includes four switches and a series resonant network. In addition to the classical complementary switching states, demonstrated by Fig. 2(a) and (b), a third state is added which introduces a zero-voltage resonant current path [Fig. 2(c)]. This state is used to balance the residual charge of the flying capacitor, i.e., restore the flying capacitor's voltage to its original state by reversing its polarity.

The operation of the converter shown in Fig. 2 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 3 that illustrates the capacitor voltage V_C and the resonant current I_C for an arbitrary case of an uneven voltage ratio. By turning Q_1 and Q_3 ON, a charge state [Fig. 2(a)] is commenced, in which the resonant tank connects to V_{in} while in series with V_{out}, resonantly charging the flying capacitor from a voltage potential of $V_{\text{in}} - V_{\text{out}}$. After a half-resonant cycle, i.e., at zero current, the switches

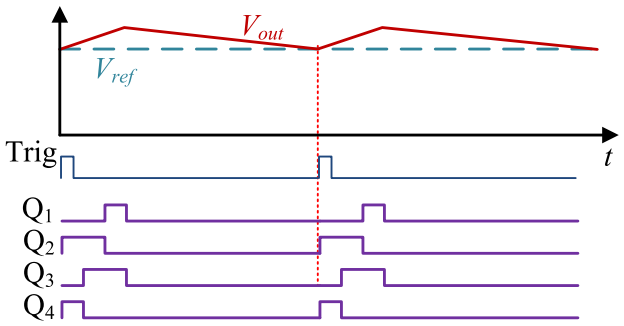


Fig. 4. GSwRC. Waveform relations between comparator inputs and the state signals for a PDM regulation scheme. "Trig" is the signal received from a load comparator; "Blank" is an internal blanking signal to avoid overlapping if subsequent pulses are needed.

are turned OFF and followed by the complementary pair, Q_2 and Q_4 [Fig. 2(b)]. At this point, the resonant tank connects in parallel to the output and discharges the flying capacitor onto the potential of V_{out}. In this example $V_{\text{out}} > 0.5V_{\text{in}}$, so when completing the discharge state after another half-resonant cycle only a portion of the charge is delivered to the output. This results in V_C that is different from its voltage at the starting point of the charge state. By turning Q_2, Q_3 ON [Fig. 2(c)], the resonant tank is short-circuited. This creates the required charge balance and reverses the flying capacitor voltage polarity such that the voltage at the end of the balance state equals the voltage at the beginning of the charge state.

The relationship between I_{out} and V_{in} follows a gyrator behavior [30], [40], [41] and can be expressed as:

$$I_{\text{out}} = 2V_{\text{in}}\text{fC} \tag{1}$$

where f is the repetition frequency of the three operating states. Voltage regulation is obtained by introducing time delay between consecutive sequences, i.e., PDM [42]–[44]. One way to create a simple PDM control is depicted in Fig. 4, by comparing the output voltage to a reference level, triggering the power stage each time the reference is crossed, in a similar manner to constant on-time controllers in discontinuous conduction mode [45], [46]. The system is able to react and compensate for any changes in the input voltage, reference voltage, or the load such that the average output voltage is obtained without over/undershoot. By this method, f is fully controllable and can be of any value, up the continuous operation frequency limit of

$$f_{\max} = (3\pi \text{ZC})^{-1}; \quad Z = \sqrt{L/C}. \tag{2}$$

As in SICs that are regulated by PDM, the rms currents of the GSwRC are relatively higher than those that operate in the continuous conduction mode. As opposed to other PDM SICs, however, in the case of the GSwRC, no additional losses are dominant thanks to the resonant operation mode and the resultant soft switching. A potential challenge that is associated with the higher rms currents is the stress on the flying capacitor, narrowing the selection range of possible capacitors materials to those of lower ESRs. In the context of voltage regulators, however, this limitation is not severe since the typical required capacitance values are in the range of 100s nF. To remain within reasonable sizing of the capacitors, reverse-geometry capacitors, or paralleling several smaller components is recommended.

The inductor, although having a small inductance value, has to sustain relatively high rms currents. However, on the contrary to the magnetics design in SICs, the per-cycle energy that is stored in the inductor is zero. As a result, the main factor of the inductor sizing stems from the core losses, rather than saturation limits. The GSwRC shares the same switch count of other step-up/down realizations such as a noninverting buck–boost with comparable efficiency [30]. Nevertheless, specific comparison to step-down regulators implemented with SICs [18], [47]–[50], demonstrates that although having more switches which may result in larger silicon area, the overall power density of the GSwRC is considerably improved. This is accomplished by a coreless magnetic element which enables simpler integration of the system and by an output filter that is sized to the voltage ripple requirements alone.

III. Loss Analysis and Review on Generalized Optimization

In previous studies, derived from the precursor resonant SCC foundation, symmetrical loop resistances have been assumed for the multiple switching states of the GSwRC [30], [37], [51]–[53]. While appropriate for most discrete-component realization, in area-sensitive applications and in particular for IC implementation, higher attention should be given to the desired resistance per-loop to obtain the target efficiency. Given a typical operation as described earlier for a case where some of the switches carry out more current than others, it may appear that for a finite die size an asymmetric allocation of the of the transistors' on-resistances results in a higher efficiency from which would be obtained by a uniform on-resistance setup. In [54], it has been shown that uniform current distribution throughout the die leads to even power dissipation resulting in minimum losses. Thus, to minimize losses each transistor should be sized based on the rms current through it. It should be noted, however, that in the case of components with different structure or technology properties are to be used (e.g., NMOS and PMOS), a design for uniform current distribution is not sufficient to achieve minimum losses. There, the sizing should take into account the technology characteristics of each device.

The losses of power converters can be categorized in variety of ways [23], [24], [29], [31]–[36], [55]. In the context of this paper, where the main focus is at zero-current switching (ZCS) gyrator-mode switched-resonator converter, the dominant contributors to the power dissipation are the conduction losses. It should be noted that other capacitive related losses such as: gate drive loss and bottom plate capacitance are equal for both symmetrical and optimized partitioning while finite die size is considered. Thus, the main focus is on optimizing the conduction losses versus sizing. Here, loss analysis relies on previous modeling and optimization of SCC and resonant SCC [19], [23], [31], [32], [35], [55]–[58], such that it provides a general framework to analyze performance based on the conduction losses. The conduction losses P_{cond} can be described by the sum of losses from each transistor Q_i, expressed by its

on-resistance $R_{\text{on,Qi}}$ and the rms current $I_{\text{rms,Qi}}$

$$\begin{cases} P_{\text{cond}} = \sum_{i=1}^{N} P_{\text{Qi}} = P_{\text{Q1}} + P_{\text{Q2}} + \cdots + P_{\text{QN}} \\ P_{\text{Qi}} = I_{\text{rms,Qi}}^2 R_{\text{ON,Qi}} = I_{\text{rms,Qi}}^2 \dfrac{K_i}{W_i}; \quad i = 1, 2, \ldots, N \\ K_i = \dfrac{L_g}{\mu c_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})} \end{cases} \tag{3}$$

where μ (mobility), C_{ox} (oxide capacitance), V_{gs} (nominal gate–source voltage), V_{th} (gate threshold voltage), and L_g (gate length) are the device's technology-dependent constants defined here as K_i (i is the switch's index). W_i is the gate width which determines the transistor's resistance alongside K_i. Without losing generality, the analysis of this study refers to a normalized gate length L_g for all devices. Then, the area can be calculated using the width parameter alone.

The die width (and area, assuming normalized length for all devices) that is formed by summation of areas for the individual switches can be expressed as

$$\sum_{i=1}^{N} W_i = W_{\text{total}}. \tag{4}$$

Similar to the analytical approach in [55], by applying the Lagrange multipliers optimization method to minimize (3), and using (4) as the optimization constraint (full details and mathematical proof are given in Appendix A), the optimal values for W_i are derived

$$\frac{W_i}{W_{\text{total}}} = \frac{I_{\text{rms,Qi}}\sqrt{K_i}}{\sum_{i=1}^{N} (I_{\text{rms,Qi}}\sqrt{K_i})}. \tag{5}$$

For convenience of viewing electrical characteristics instead of geometrical ones, (5) can be inverted to represent the optimal resistance ratio, defined here as ψ_i, for a transistor's size with respect to the technology characteristics and rms current

$$\psi_i = \frac{R_{\text{ON,Qi}}}{R_{Q,\text{total}}} = \frac{W_{\text{total}}}{W_i} = \frac{\sum_{i=1}^{N} (I_{\text{rms,Qi}}\sqrt{K_i})}{I_{\text{rms,Qi}}\sqrt{K_i}} \tag{6}$$

where $R_{Q,\text{total}}$ is a theoretical resistance for a single transistor which consists the overall silicon width W_{total} and can be obtained by

$$\psi_i = \frac{R_{\text{ON,Qi}}}{R_{Q,\text{total}}} = \frac{W_{\text{total}}}{W_i} = \frac{\sum_{i=1}^{N} (I_{\text{rms,Qi}}\sqrt{K_i})}{I_{\text{rms,Qi}}\sqrt{K_i}}. \tag{7}$$

Rearranging (5) and (6), the individual resistance per-transistor is obtained as a function of P_{cond}

$$R_{\text{ON,Qi}} = \psi_i \frac{P_{\text{cond}}}{\sum_{i=1}^{N} (I_{\text{rms,Qi}}\sqrt{K_i})^2}. \tag{8}$$

In the context of the GSwRC as the object of this study, the analysis is done under the following assumptions: a relatively high ratio between the circuit's characteristic impedance to the loop resistance (i.e., quality factor $Q = R_{\text{loop}}/Z \gg 5$) of the resonant network, constant output current I_{out}, and that the output voltage ripple is negligibly small. The relationship between the states' rms currents and the average output current I_{out} can be expressed as

$$\begin{cases} I_{\text{rms,S1}} = (\sqrt{A\,\pi\,R_L/4Z})I_{\text{out}} \\ I_{\text{rms,S2}} = |\sqrt{A\,\pi\,R_L/4Z} - \sqrt{A^{-1}\pi\,R_L/4Z}|\,I_{\text{out}};\ A = \dfrac{V_{\text{out}}}{V_{\text{in}}} \\ I_{\text{rms,S3}} = |2\sqrt{A\,\pi\,R_L/4Z} - \sqrt{A^{-1}\pi\,R_L/4Z}|\,I_{\text{out}} \end{cases} \tag{9}$$

where A is the conversion ratio and R_L is the load resistance.

It should be noted that the representation of the load as resistance (i.e., $I - V/R$) is done for algebraic convenience purely, and by no means affect the sourcing characteristics of the GSwRC. The converter has been shown to behave as a current source with gyrator relationship and as such is a very strong candidate to supply modern PoL that their load behavior is as a current source. This has been broadly detailed and demonstrated in [37] and [51]–[53].

Since the converter operates under ZCS conditions, to individually identify the per-transistor contribution to the conduction losses, the rms current of the transistors can be written as a function of (9) as

$$\begin{cases} I_{\text{rms,Q1}} = I_{\text{rms,S1}} \\ I_{\text{rms,Q2}} = \sqrt{I_{\text{rms,S2}}^2 + I_{\text{rms,S3}}^2} \\ I_{\text{rms,Q3}} = \sqrt{I_{\text{rms,S1}}^2 + I_{\text{rms,S3}}^2} \\ I_{\text{rms,Q4}} = I_{\text{rms,S2}}. \end{cases} \tag{10}$$

Assuming the transistors' on-resistances, $R_{\text{ON,Q1}}$ through $R_{\text{ON,Q4}}$, are the dominant resistances per the loop they are active, the total power losses of the converter as a function of the conversion ratio are derived by summation of the losses as follows:

$$P_{\text{loss}} = \frac{\pi R_L}{4Z} \begin{bmatrix} (R_{\text{ON,Q1}} + 5R_{\text{ON,Q2}} + 5R_{\text{ON,Q3}} + R_{\text{ON,Q4}})A \\ +(2R_{\text{ON,Q2}} + R_{\text{ON,Q3}} + R_{\text{ON,Q4}})A^{-1} \\ -2(3R_{\text{ON,Q2}} + 2R_{\text{ON,Q3}} + R_{\text{ON,Q4}})I_{\text{out}}^2 \end{bmatrix}. \tag{11}$$

Substituting (8) and (10) into (11), and after some manipulations, the efficiency of the converter η as a function of A, $R_{Q,\text{total}}$ and ψ can be expressed as

$$\eta = \left[1 + \frac{\pi R_{Q,\text{total}}}{4Z} \begin{pmatrix} (\psi_1 + 5\psi_2 + 5\psi_3 + \psi_4)A \\ +(2\psi_2 + \psi_3 + \psi_4)A^{-1} \\ -2(3\psi_2 + 2\psi_3 + \psi_4) \end{pmatrix} \right]^{-1}. \tag{12}$$

Fig. 5(a) shows the resulting efficiency versus conversion ratio curves of (12), for several cases of on-resistance selection and compares symmetrical sizing with an optimized one. Symmetrical sizing has been plotted by setting equal values for ψ in (12), whereas in the optimized plot the values for ψ are set per-transistor as prescribed earlier by the design guidelines. It can be observed that, near the target voltage ($A = 0.5$) where charge balance of resonant SCC is naturally obtained, the results of both sizing methods coincide. Predicted by the initial conjecture of this study, as the conversion ratio

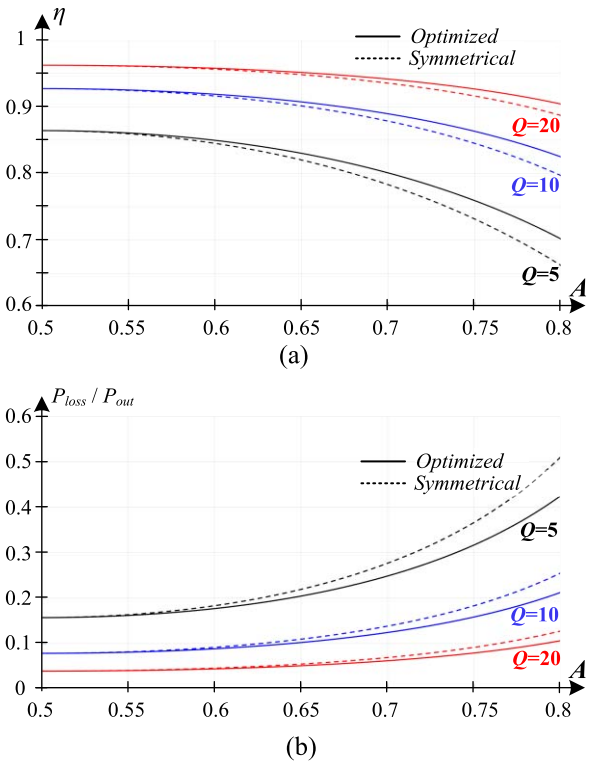


Fig. 5. Theoretical efficiency and losses curves for a bridge GSwRC. Symmetrical (dotted lines) and optimized (solid lines) partition as a function of A, for various values of Q: (a) efficiency and (b) P_{loss} versus P_{out}.

deviates from center, a significant efficiency improvement can be observed in favor of the optimized sizing method. An even more interesting view is described by the normalized power loss factor that is depicted in Fig. 5(b), showing the possible power saving as a result of better area distribution between the transistors. For example, in conversion ratio of 0.75, $Q = 10$ and output power of 10 and 0.5 W of the losses can be trimmed down for the same total area.

IV. Design Examples

Using the above analysis and observations, generalized IC design guidelines to obtain an optimized ratio between size and losses of voltage regulator GSwRC are summarized and then followed by practical design examples. The procedure is as follows.

1) Given target values for $V_{\text{in,min}}$, $I_{\text{out,max}}$and operating frequency f_{max}.
2) Calculate the resonant network parameters C and L by
$$C = I_{\text{out,max}}/2V_{\text{in,min}}f_{\text{max}} \quad L = [(3\pi f_{\text{max}})^2 C]^{-1}. \quad (13)$$
3) By the vendor's process design kit (PDK) obtain the transistors' technology-dependent parameter K_i.
4) Calculate the rms current through each device.
5) Use (6) to calculate ψ_i for each transistor.
6) From the target efficiency η, conversion ratio A, and ψ_i, calculate the theoretical resistance $R_{Q,\text{total}}$
$$R_{Q,\text{total}} = \frac{(\eta^{-1}-1)}{\frac{\pi}{4Z}\begin{pmatrix}(\psi_1+5\psi_2+5\psi_3+\psi_4)A \\ +(2\psi_2+\psi_3+\psi_4)A^{-1} \\ -2(3\psi_2+2\psi_3+\psi_4)\end{pmatrix}}. \quad (14)$$

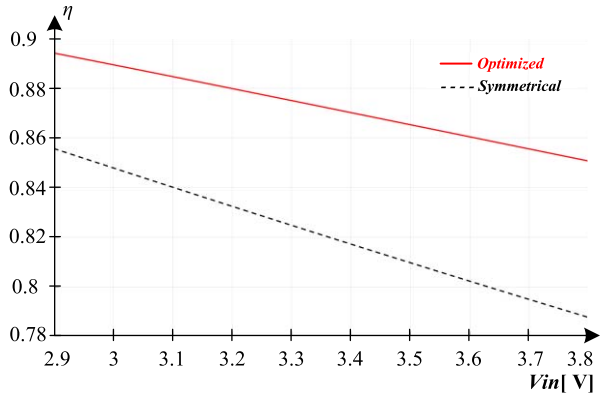


Fig. 6. Theoretical efficiency curves of a bridge GSwRC as a function of V_{in}. Symmetrical (dotted line) and optimized (solid line) partition, with the target parameters: $V_{\text{in,nom}} = 3.3$ V, $V_{\text{out}} = 0.7$ V, $I_{\text{out,max}} = 1$ A, and $f_{\text{max}} = 10$ MHz.

7) Calculate P_{cond} from (7), the optimized on-resistance from (8), and determine the individual silicon width per-transistor by
$$W_i = \frac{K_i}{R_{\text{ON,Qi}}}. \quad (15)$$

To demonstrate and validate the design procedure, two design examples are provided. In the first example, a bridge GSwRC is presented, and the second design example is demonstrated through a more complex design of a multiphase Fibonacci resonant SCC.

A. Bridge Gyrator Switched-Resonator Converter

Given a 0.18-μm CMOS process, technology-dependent parameters are obtained to be $K_1 \approx 8.4$ m$\Omega \cdot$ m and $K_2 - K_4 \approx 3$ m$\Omega \cdot$m. Based on the above analysis, the design example is demonstrated by 0.7-W GSwRC IC with target values of: $V_{\text{in}} = 3.3$ V, $V_{\text{out}} = 0.7$ V, $I_{\text{out,max}} = 1$ A, $f_{\text{max}} = 10$ MHz, and $\eta \approx 87\%$. The resonant network values are calculated as $C \approx 17$ nF and $L \approx 7$ nH. The required resistances as extracted by the optimized procedure $R_{\text{ON,Q1}}$ through $R_{\text{ON,Q4}}$: 75, 11, 15.5, and 12 mΩ, and in terms of silicon widthW_1 through W_4: 112 400, 346 800, 194 300, 249 500 μm, respectively, while the resulting total silicon width is found to be $W_{\text{total}} \approx 903\,000$ μm. Fig. 6 depicts an efficiency prediction for the design example. It can be observed that for the same silicon area, efficiency improvement by 5% can be obtained at nominal input voltage of 3.3 V. A more noticeable benefit can be viewed in terms of overall size, where approximately 30% less silicon area is required to obtain the same efficiency.

An alternative view of the devices optimization is exemplified in Fig. 7 for specific operating conditions of the example on hand. It shows the loss breakdown per-transistor as a function of the device's on-resistance, where the losses have been normalized to the minimal losses that can be obtained under specified operating conditions. As can be observed, for a finite area a minimum point exists per device that exactly satisfies (8). Summation of the minima results it the most compact as well as efficient design per given die size.

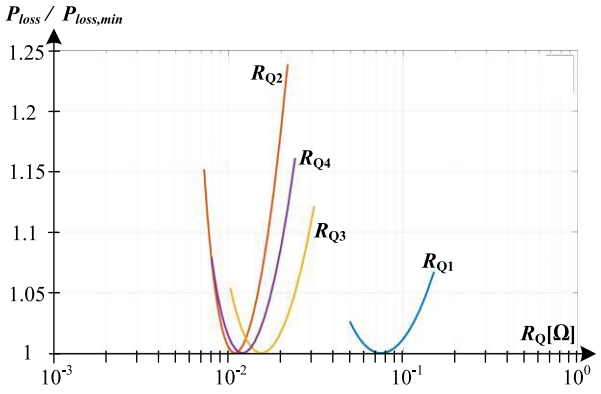


Fig. 7. Minimum losses per die size of the bridge GSwRC's integrated devices, with the target parameters: $V_{\text{in,nom}} = 3.3$ V, $V_{\text{out}} = 0.7$ V, $I_{\text{out,max}} = 1$ A, and $f_{\max} = 10$ MHz.

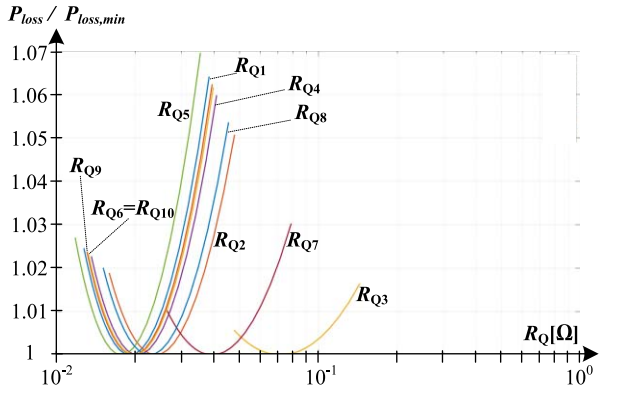


Fig. 9. Minimum losses per die size of a multiphase Fibonacci resonant SCC, with the target parameters: conversion ratio $A = 3/8$, $V_{\text{in}} = 5$ V, $I_{\text{out}} = 1$ A, and $f = 5$ MHz.

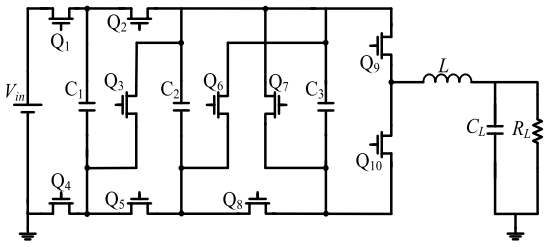


Fig. 8. Multiphase Fibonacci resonant SCC topology. For conversion ratio of 3/8 switching sequences are: state 1: Q_1, Q_5, Q_6, Q_{10}—ON, state 2: Q_2, Q_4, Q_8, Q_9—ON, state 3: Q_4, Q_5, Q_7, Q_9—ON, and state 4: Q_1, Q_3, Q_8, Q_9—ON.

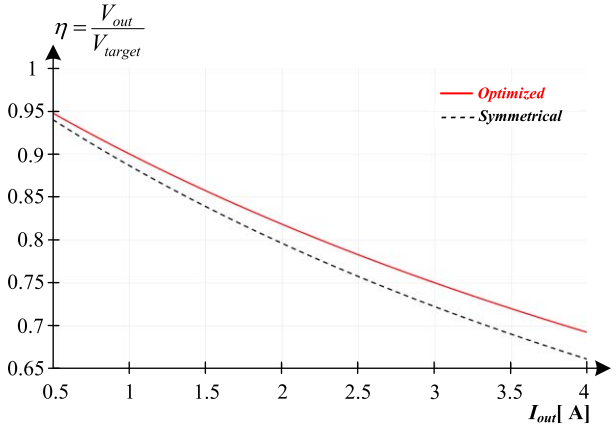


Fig. 10. Efficiency curves of a multiphase Fibonacci resonant SCC as a function of the output current I_{out}. Symmetrical (dotted line) and optimized (solid line) partition, with the target parameters: $V_{\text{in}} = 5$ V, $V_{\text{out}} = 1.875$ V, $I_{\text{out}} = 1$ A, and $f = 5$ MHz.

B. Multiphase Fibonacci Resonant SCC

To further demonstrate the effectiveness of the optimization method, an optimized Fibonacci resonant SCC is examined by simulation and compared to the results of a symmetrical design. The schematic configuration shown in Fig. 8 includes three flying capacitors and four switching states to trim down the output voltage by 3/8 times the input voltage. A multiphase Fibonacci resonant SCC is capable of generating multiple fractional conversion ratios with Fibonacci sequence resolution [19], [58]–[60]. To achieve a desired fractional conversion ratio, a specific switching sequence that interconnects the flying capacitors with summing or subtracting action to the source and the output is applied.

Validation of the optimization procedure is carried out by simulation with the following target parameters: $V_{\text{in}} = 5$ V, conversion ratio of $A = 3/8$, $I_{\text{out}} = 1$ A, $f_{\max} = 5$ MHz, and $\eta = 90\%$. The flying capacitors are chosen to be 60 nF and the inductor is chosen to be 10 nH. The ratios between the switches' rms currents ψ_1–ψ_{10} were obtained by simulation, resulting in $R_{\text{ON,Q1}}$ through $R_{\text{ON,Q10}}$: 19.5, 24.5, 72, 21, 18.2, 20.3, 41, 23, 20.1, and 20.3 mΩ. It can be seen that $R_{\text{ON,Q6}} = R_{\text{ON,Q10}} \approx R_{\text{ON,Q9}}$, this is due to identical rms current through the devices for the targeted conversion ratio. Fig. 9 depicts the normalized losses over various on-resistances of the devices, it can be well observed that the point of minimum losses coincides with the values that have been obtained by the sizing procedure. A further validation of the results, given the case of a Fibonacci converter, can be obtained by comparison to earlier studies [31], [55], [61], which provide a through procedure to extract the required resistance per a given efficiency for SCC and resonant switched-capacitor converter. The optimized die size obtained in this paper coincide with the one derived earlier in the literature. The results of this paper enable further "fine tuning" for the partitioning of the transistors based on the mode of operation while maintaining the optimized die-size.

For a technology-dependent parameter $K \approx 3$ mΩ · m the resulting total silicon width is found to be $W_{\text{total}} \approx 1.2$ mm. It should be further emphasized that for the same die size the resultant efficiency of a symmetrical converter is 88% with on-resistances $R_{\text{ON,Q1}} - R_{\text{ON,Q10}} \approx 21.5$ mΩ. To obtain 90% efficiency (i.e., to meet the target specification listed in the above example and achieved with the optimized procedure of this study) with a symmetrical partition the total silicon width that in required is 1.4 mm, which is approximately 15% overhead.

The results in Fig. 10 show efficiency comparison between a symmetrical and an optimized Fibonacci resonant SCC as a function of the output current I_{out}. It can be observed that for the same silicon area, efficiency improvement by 2% can be obtained for the target operating values, for higher output currents it further improves. Even for complex SCC design

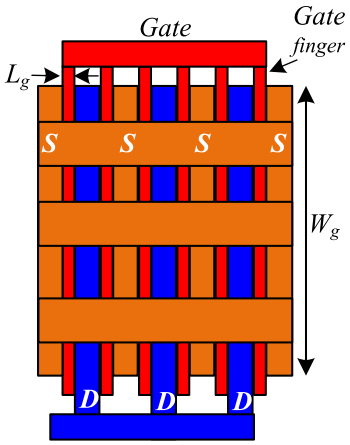


Fig. 11. Simplified structure of a device with paralleled multiple cells.

consisting of ten transistors, by using the IC design guidelines both minimum die area and losses are achieved.

V. IC Implementation

A. GSwRC On-Chip Power-Stage Implementation

The selection of the transistor type depends primarily on the drive configuration. Assuming a conventional ground-referenced driver and that the input voltage is limited to the technology voltage V_{DD}, a PMOS is used for Q_1, while NMOSs are used for Q_2, Q_3, and Q_4, based on the required gate–source threshold voltage to activate the transistor.

To maximize the channel width and to increase current handling capabilities of a 5-V CMOS process transistor, paralleled multifinger cells have been realized, as shown in Fig. 11. The size of a device with multifinger cells is typically defined in terms of the gate boundary $W_i = N_{\mathrm{fi}}\ W_g$, where N_{fi} is the number of fingers for a transistor Q_i, and W_g is the gate width for a single finger [62]. Thick oxide device typically used in high-voltage operation and has a higher R_{ON} per mm^2, therefore results in larger area of the design [63]. In the context of this paper, the maximum input voltage rating is 5 V, a high-voltage thick-oxide device is superfluous for the target performance of the converter. Since voltage blocking is not a constraint for the given maximum input voltage rating, further size consideration in terms of the switch volt-ampere product [55] has a negligibly small effect (or none) on the optimization product. Thus, for the given technology, a standard 5-V-gated thin-oxide device with a generic$W_g = 50\ \mu$m and a breakdown voltage of $\approx$5.5 V has been implemented. Given the PDK W_g and L_g constraints, an accurate and efficient quadrilateral layout of the power stage can be applied. It should be noted that the transistors are connected via a top metal pad, resulting a relatively low parasitic resistance of the conduction and is neglected for the design.

B. Driver Circuitry Implementation

A fully integrated circuit based on buffers with the ability to drive transistors with large gate width has been implemented [64]. Buffers chain is realized by logical effort technique, with a network of three custom designed buffers for each switch. For the technology used in this study, the ratio between the pull-up network and the pull-down network is chosen to be 1.5, to satisfy both reasonable propagation delay and die area. In the context of driving power transistors, the buffers sizing should also be considered due to the relatively higher input capacitances of the driving chain, such that the tapering factor is given by

$$\text{tapering factor} = \frac{C_{\mathrm{gate}}}{C_{\mathrm{input}}} \tag{16}$$

where C_{gate} is the gate capacitance of the power device, C_{input} is the input capacitance of the first buffering stage [63].

To assure a nondistorted input gate signal, the first inverter of the buffers chain has been matched in size to the inverter at the output of the input–output unit. Assuming that the channel length L_g is equal along the driving chain, based on the analytical approach presented in [64] and [65] and on the overall chip area constraints for the tape out, the tapering factor was chosen to be 5. Therefore, the inverters have been realized with increasingly growing factor of 5. In addition, due to the limitations of the chip area, the last buffer stage has been designed with two identical inverters reducing the overall area consumption of each driver. The functionality of the driving stage has been verified using the Cadence Spectre simulator guaranteeing high sourcing–sinking capabilities and reasonable delay time to eliminate any potential distortion. Fig. 12 shows in detail a sized example of a driving stage, where $W_{g,P} = 1.5 \cdot W_{g,N}$.

Since the driver stage is integrated and the control signals are all ground referenced (with gate voltage swing between 0 and 5 V), neither isolation nor level shifters are required. Delineated in Fig. 13 are postlayout measurements

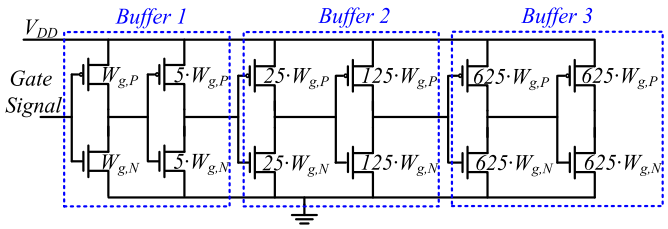


Fig. 12. Schematic of the implemented IC drive circuitry.

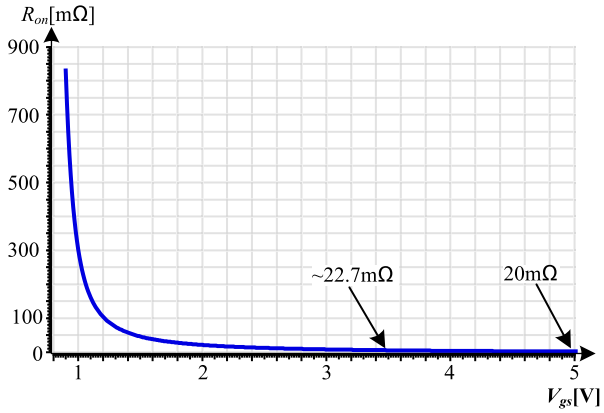


Fig. 13. Postlayout measurements of on-resistance versus gate-to-source voltage for a typical device of the implemented technology.

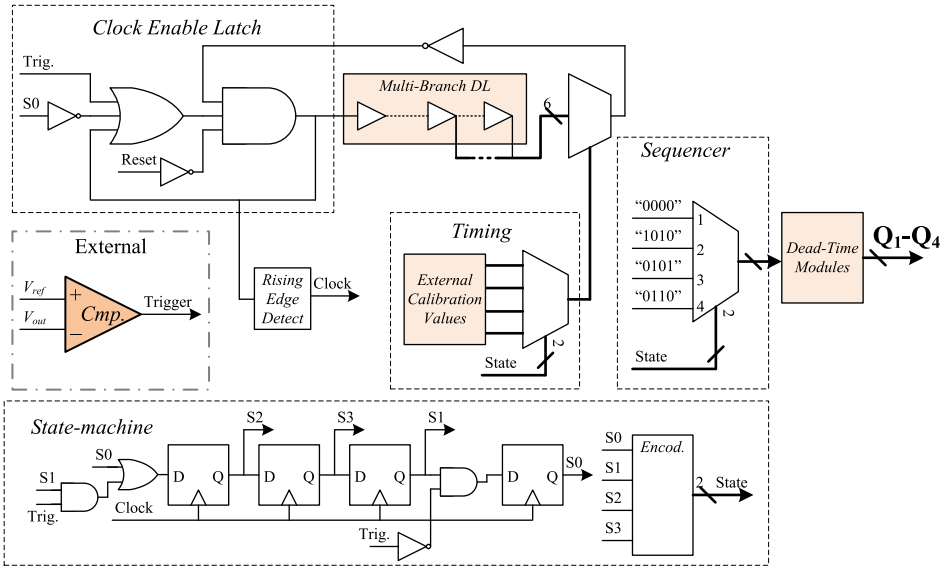


Fig. 14. Schematic of a delay-line-based constant on-time controller.

of the on-resistance $R_{\rm ON}$ of a single device as a function of the gate-to-source voltage $V_{\rm gs}$. It can be observed that for $V_{\rm gs} \approx 3.5$ V, the variation of the on-resistance is by approximately 2.7 mΩ. This implies that even for a worst-case scenario where $V_{\rm in} = V_{\rm DD}$, the driving circuitry is still functional without dramatically increasing the conduction losses.

C. Monolithic Delay-Line-Based Constant On-Time Controller

A fully monolithic controller has been designed and implemented on-chip by an automated synthesis process and place-and-route tools to regulate the output voltage. As described in [37], regulation is facilitated using a single comparator which compares the output voltage to an internal value and triggers the GSwRC when needed. Fig. 14 shows a schematic describing the main components of the control unit.

A flip-flop-based state machine dictates the correct gate sequence to properly operate the power stage. An external comparator creates the variable-frequency PDM trigger signal: the trigger rises when $V_{\rm out}$ falls below $V_{\rm ref}$ and falls back when $V_{\rm out}$ returns above $V_{\rm ref}$. The trigger signal is unmasked when the controller is idle (namely, state S0) where its rising edge is detected to clock the GSwRC power stage to a discharge state (S2) while internally latching the trigger signal to high. This latched signal activates an internal delay ring clock to continue sequencing the power stage to charge balance (S3), followed by charge (S1). The next state is then determined by the trigger status at the clock event: if the external trigger is high S1 will be followed by S3 for continuous switching at $f_{\rm max}$, otherwise the controller will go to S0 and idle.

In addition to defining the correct sequence, the selected state (S0–S3) dictates the length of the ring-clock delay line by a timing calibration mechanism. Soft switching is guaranteed by modifying the individual calibration values for each state, fed by a separate module, or preprogrammed. For the experimental results detailed in this paper, manual calibration was obtained, the calibration module is beyond the scope of this paper and is featured in subsequent publication [66]. Finally, adequate dead time is guaranteed by a break-before-make module based on delay lines. Fig. 15(a) shows a die photograph of the implemented controller, and Fig. 15(b) shows the measured experimental gate logic sequence operating at ~3 MHz produced from the monolithic delay-line controller.

VI. Experimental and Postlayout Verification

Following the design procedure, an IC prototype that implements the bridge GSwRC voltage regulator has been designed and fabricated in 0.18-μm 5-V CMOS process. As discussed in the previous section, the timing controller to regulate the output voltage was implemented by an automated synthesis process and place-and-route tools, directly from the hardware description language representation. To minimize parasitic resistance caused by metallization and bond wires [67], a dual power stage was designed and routed in parallel. The first power stage was designed such that $R_{\rm ON}$ of the power transistors was designed to value of ~20 mΩ, while that the second stage with $R_{\rm ON} \approx 40$ mΩ, the chip micrograph is depicted in Fig. 16(a). It should be emphasized that imperfect characteristics of shuttle packaging limited the available current of the experimental GSwRC IC prototype to the range of 2 A. This, however, does not impose any limitation on the topology neither on the sizing analysis that has been carried out. The fabricated IC prototype was packaged using 24-pin 4×4 mm quad-flat no-leads (QFN) package. The chip connects to a resonant tank which includes a flying capacitor with a value of $C = 50$ nF, total series inductance (including stray) measured to be $L \approx 6$ nH, and total loop resistance of approximately 100 mΩ. Fig. 16(b) depicts the IC prototype on PCB.

Fig. 17(a) shows the open-loop experimental results of the flying capacitor current and voltage, verifying operability of the design. Delineated in Fig. 17(b) is the experimental setup of the flying capacitor current measurement using a Rogowski-type current sensor [68]. It should be noted that

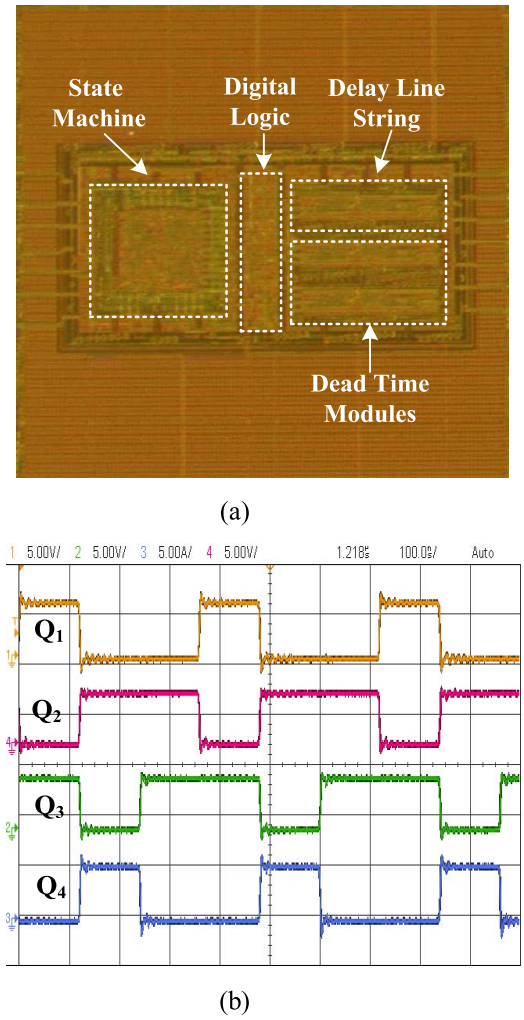


Fig. 15. (a) Die photograph of the controller IC. (b) Experimental gate signals operating at 3 MHz produced from the monolithic controller. Vertical scale: 5 V/div and time scale: 100 ns/div.

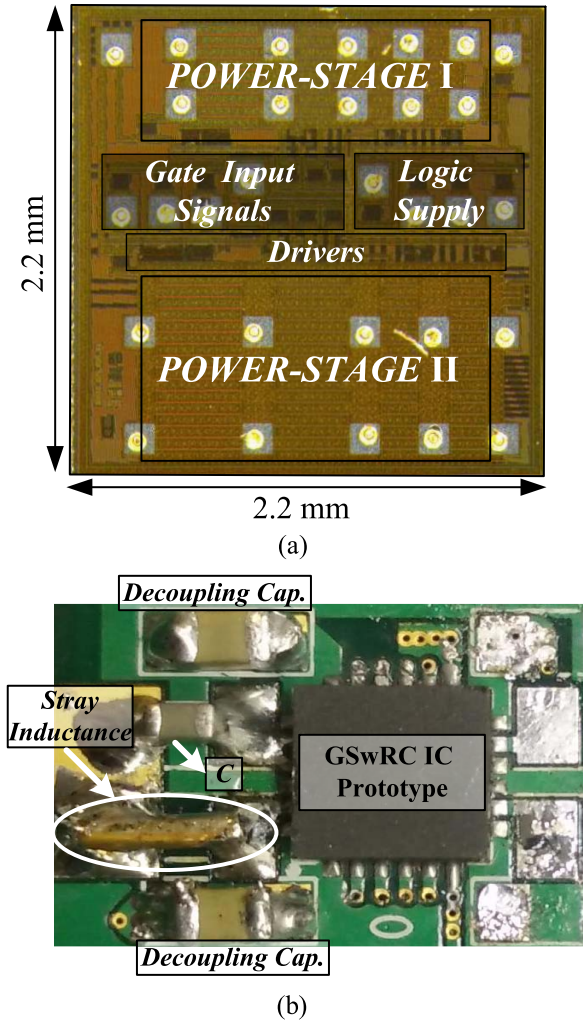


Fig. 16. (a) Chip micrograph of a bridge GSwRC. (b) IC prototype on PCB.

the current waveform is measured on the stray loop inductance with an open probe; therefore, the current waveform revels the current shape but does not calibrated to guarantee true levels. Operating under the above specifications, the converter IC is capable to output power up to 2.25 W, whereas the efficiency is measured to be 85%. These results are in very good agreement with the theoretical predictions. Table I summarizes the experimental measurements and test conditions of the IC prototype.

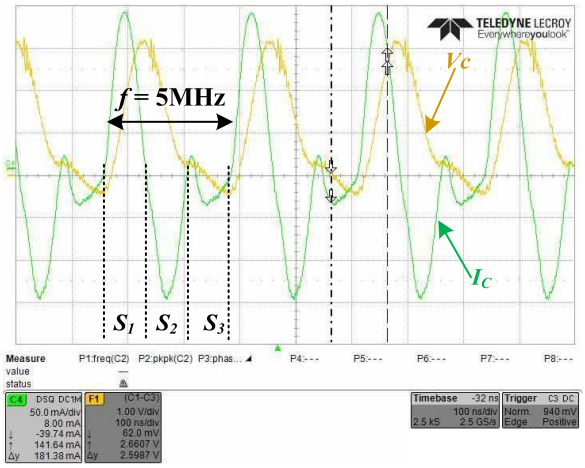
Efficiency curve of the converter IC as function of V_{in} is depicted in Fig. 18. The experiment was carried out by varying the input voltage and compensating the frequency with the timing controller, such that the output power and the output voltage, 2.25 W and 1.5 V, respectively, were kept constant. The experimental measurements tightly follow the results obtained by the simulation as well as the theoretical predictions. As can be observed, lower efficiency can be obtained for higher input voltages. This is primarily due to higher conduction losses at higher conversion ratios. Fig. 19 shows the efficiency of the converter IC as a function the output current I_{out}. As can be seen, in light-load operation, there is a discrepancy between the experimental and simulation results from the theoretical

TABLE I

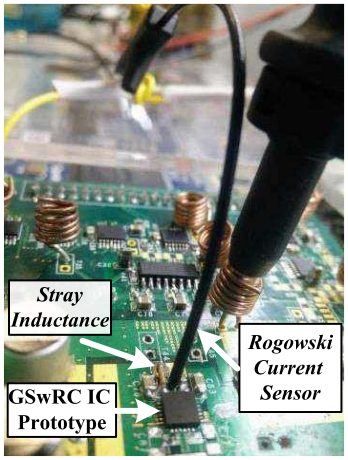
SUMMARY OF IC PROTOTYPE EXPERIMENTAL MEASUREMENTS AND TEST CONDITIONS

Specifications	*Condition/Measurement*
Package	4x4 QFN - MLP
V_{in}	3V
R_{loop}	~100mΩ
V_{out}	1.5V
I_{out}	1.5A
Off Chip resonant tank	6nH, 50nF
Switching Frequency	5MHz
Quality Factor Q	~4
Efficiency	~85%

analysis, this is due to the resonant characteristics of the three states that are not identical, which was not taken into the theoretical model analysis. The experimental measurements also highlight the advantage of the GSwRC operating at light loads. As discussed in detail in Section II, the GSwRC is regulated by PDM, and in light-load operation the effective switching frequency is very low. As a result, the gate drive loss has very little, to no, effect at these conditions. As can be observed from Fig. 19 even for very light-load operation of 20 mA, the efficiency drops only at 4% and maintains a near



(a)



(b)

Fig. 17. (a) Experimental measurements for the switched-resonator flying capacitor voltage (yellow curve) and resonant current (green curve), time scale 100 ns/div. (b) Experimental setup of the resonant current measurement.

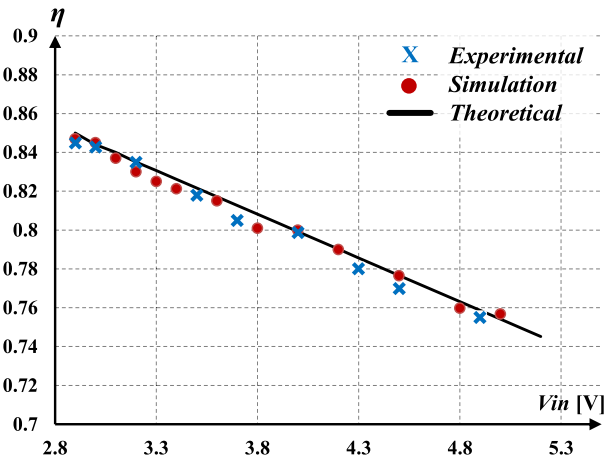


Fig. 18. IC GSwRC prototype efficiency as a function of input voltage V_{in}.

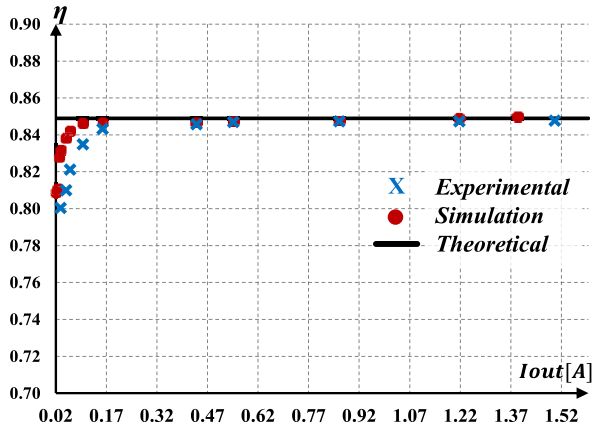
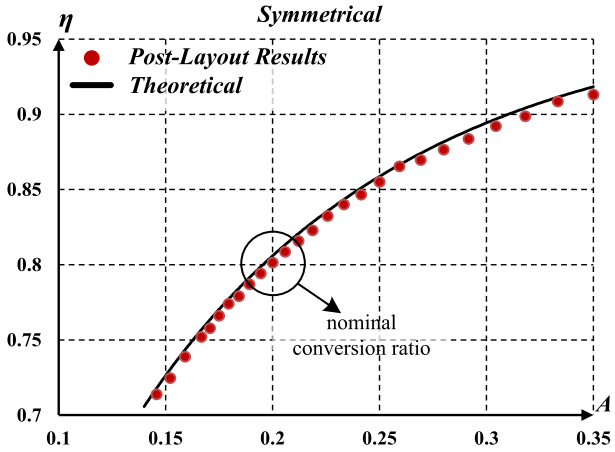
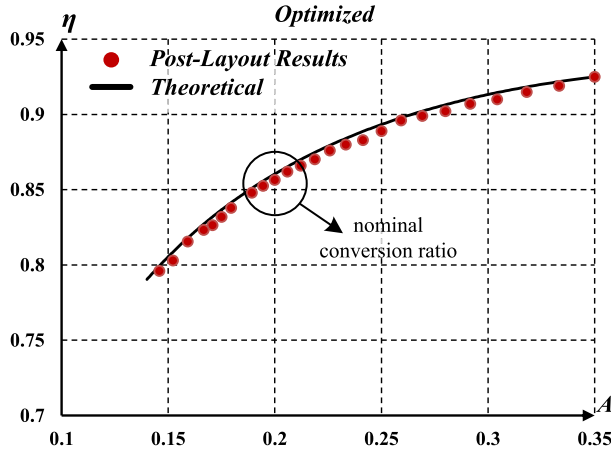


Fig. 19. IC GSwRC prototype efficiency as a function of load current I_{out}.



(a)



(b)

Fig. 20. Postlayout efficiency results as a function of the conversion ratio A with the target parameters: $V_{\text{in}} = 3.3$ V, $V_{\text{out}} = 0.7$ V, $I_{\text{out}} = 1$ A, and $f_{\text{max}} = 10$ MHz. (a) IC GSwRC at symmetrical partition $R_{\text{ON}} \approx 20$ mΩ. (b) Optimized IC GSwRC design whereas $R_{\text{ON,Q1}}$ through $R_{\text{ON,Q4}}$: 75, 11, 15.5, and 12 mΩ.

constant efficiency over the entire operation range, virtually identical to the normal operation mode.

Fig. 20 shows the postlayout efficiency comparison between a symmetrical and an optimized IC GSwRC designs (comprehensive analysis presented in Section IV-A) with the following nominal operating conditions: $V_{\text{in}} = 3.3$ V, $V_{\text{out}} = 0.7$ V, and $I_{\text{out}} = 1$ A operating at 10 MHz. The solid line shows theoretical predicated efficiency whereas the

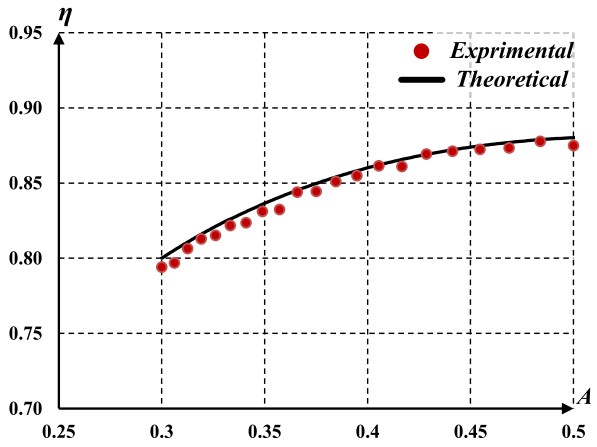


Fig. 21. Discrete bridge GSwRC prototype experimental efficiency measurements as a function of the conversion ratio A with the target parameters: $V_{\text{in}} = 5$ V, $V_{\text{out}} = 1.5$ V, $I_{\text{out,max}} = 1.8$ A, and $f_{\text{max}} = 3.5$ MHz. Whereas $R_{\text{ON,Q1}}$ through $R_{\text{ON,Q4}}$: 55, 30, 40, and 30 mΩ.

dotted markers show the postlayout outcomes. In Fig. 20(a), theoretical and postlayout efficiency results of the IC GSwRC prototype are depicted. At nominal conversion ratio $A \approx 0.21$ the efficiency is measured to be 81%, the theoretically predicted efficiency behavior is well validated by postlayout analysis. Fig. 20(b) presents efficiency outcomes of an optimized design; it can be well observed that for the same die size in the region of the target operating values, the measured efficiency of the optimized design is higher by approximately 5% than the symmetrical design. For higher conversion ratios, the dominance of the optimized design is well noticed, while a significant area saving is achieved with the optimization routine.

To further validate the optimization procedure, a discrete bridge GSwRC prototype has been built and tested. Following the design procedure for the target parameters: $\eta \approx 80\%$, $V_{\text{in}} = 5$ V, $V_{\text{out}} = 1.5$ V, and $I_{\text{out,max}} = 1.8$ A operating at maximum switching frequency of 3.5 MHz. By the optimization guidelines, the obtained on-resistances were $R_{\text{ON,Q1}} - R_{\text{ON,Q4}}$: 70, 25, 42, and 28 mΩ. Due to a lack of variety of discrete components, the discrete bridge GSwRC prototype has been realized with the following on-resistances: 55, 30, 40, and 30 mΩ. Theoretical and measured efficiency curves of the prototype as a function of the conversion ratio are shown in Fig. 21. It can be observed that even though the switches' on-resistances are not identical, but in the range of those obtained by the design procedure, the measured efficiencies are virtually identical to the theoretical analysis over wide range of operating conditions.

VII. Conclusion

An optimal size-efficient design methodology for the IC realization of a gyrator-mode switched-resonator converter has been presented, based on the target operating conditions and physical characteristics of the integrated devices. Following the size-optimization procedure, this paper details the efficiency analysis and characteristics of a bridge GSwRC operating as a voltage regulator. The optimization method has been demonstrated with two design examples, and its effectiveness is experimentally verified with a fully monolithic GSwRC fabricated in 0.18-μm CMOS process. The analysis has been meticulously verified by postlayout simulations and experiments and found to be in very good agreement with the theoretical predictions. In addition, a fully monolithic control system is described and implemented on-chip by an automated synthesis process and place-and-route tools to regulate the output voltage of the converter IC.

For various conversion ratios, postlayout analysis of both symmetrical and optimized GSwRC design tightly follows the theoretical predictions. To further validate the optimization method, a discrete bridge GSwRC prototype has been built and tested, and the measured results well verified over a wide range of operating conditions. The experimental measurements also further strengthen the advantages of the GSwRC ability to maintain virtually constant efficiency curve for load variations, in particular when operating at light loads. At 20-mA loading, the efficiency drops only at 4%.

Significant area saving highlights the benefit of the optimization method, providing a design-intuitive procedure to improve the size-efficiency factor based on the target operating conditions. For a given finite die-size by designing optimized GSwRC IC, in the region of the target operating values 5% efficiency improvement can be obtained for the fabricated IC. Furthermore, in terms of overall die size approximately 30% less silicon area is required to obtain the same efficiency. Combined with the topology benefits, a GSwRC voltage regulation scheme presents an attractive alternative to the SICs, in particular in area-sensitive application, and establishes the foundations for better power delivery concepts for PoL applications.

Appendix

By utilizing the Lagrange multipliers optimization on (3), while using (4) as the optimization constraint results in

$$\begin{cases} f = P_{\text{cond}} = \dfrac{I_{\text{rms},Q_1}^2 K_1}{W_1} + \dfrac{I_{\text{rms},Q_2}^2 K_2}{W_2} \\ \qquad + \cdots + \dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N} \\ g = (W_1 + W_2 +, \ldots, +W_N) = W_{\text{total}} \end{cases}$$

Lagrange Multipliers Method:

$$\begin{cases} \nabla f(W_1, W_2, \ldots, W_N) = \lambda \nabla g(W_1, W_2, \ldots, W_N) \\ g(W_1, W_2, \ldots, W_N) = W_{\text{total}} \end{cases} \tag{17}$$

this yields

$$\begin{cases} 1: \dfrac{\partial f}{\partial W_1} = \lambda \dfrac{\partial g}{\partial W_1} \Rightarrow -\dfrac{I_{\text{rms},Q_1}^2 K_1}{W_1^2} = \lambda \\ 2: \dfrac{\partial f}{\partial W_2} = \lambda \dfrac{\partial g}{\partial W_2} \Rightarrow -\dfrac{I_{\text{rms},Q_2}^2 K_2}{W_2^2} = \lambda \\ \qquad \vdots \\ N: \dfrac{\partial f}{\partial W_N} = \lambda \dfrac{\partial g}{\partial W_N} \Rightarrow -\dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} = \lambda \end{cases} \tag{18}$$

which results in the following equilibrium equality:

$$\frac{I_{\text{rms},Q_1}^2 K_1}{W_1^2} = \frac{I_{\text{rms},Q_2}^2 K_2}{W_2^2} = \cdots = \frac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} \tag{19}$$

the equality in (19) can thus be rewritten as

$$\begin{cases} \dfrac{I_{\text{rms},Q_1}^2 K_1}{W_1^2} = \dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} \\ \dfrac{I_{\text{rms},Q_2}^2 K_2}{W_2^2} = \dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} \\ \dfrac{I_{\text{rms},Q_3}^2 K_2}{W_3^2} = \dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} \\ \vdots \\ \dfrac{I_{\text{rms},Q_{N-1}}^2 K_{N-1}}{W_{N-1}^2} = \dfrac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} \end{cases}$$

$$\Rightarrow \begin{cases} W_1 = W_N \dfrac{I_{\text{rms},Q_1}\sqrt{K_1}}{I_{\text{rms},Q_N}\sqrt{K_N}} \\ W_2 = W_N \dfrac{I_{\text{rms},Q_2}\sqrt{K_2}}{I_{\text{rms},Q_N}\sqrt{K_N}} \\ W_3 = W_N \dfrac{I_{\text{rms},Q_3}\sqrt{K_3}}{I_{\text{rms},Q_N}\sqrt{K_N}} \\ \quad \vdots \\ W_{N-1} = W_N \dfrac{I_{\text{rms},Q_{N-1}}\sqrt{K_{N-1}}}{I_{\text{rms},Q_N}\sqrt{K_N}} \end{cases} \tag{20}$$

or in a generic manner

$$W_i = W_N \frac{I_{\text{rms},Q_i}\sqrt{K_i}}{I_{\text{rms},Q_N}\sqrt{K_N}}. \tag{21}$$

Substituting (21) into (4), and after some manipulations, W_{total} can thus be expressed as a function of W_N, the rms currents and the technology technology-dependent parameters K_i

$$\begin{aligned} &W_{\text{total}} \\ &= W_N \left(1 + \frac{1}{I_{\text{rms},Q_N}\sqrt{K_N}} \left(I_{\text{rms},Q_1}\sqrt{K_1} \right.\right. \\ &\qquad \left.\left. + \cdots + I_{\text{rms},Q_{N-1}}\sqrt{K_{N-1}}\right)\right) \\ &= W_N \left(\frac{\overbrace{I_{\text{rms},Q_N}\sqrt{K_N} + I_{\text{rms},Q_1}\sqrt{K_1} + \cdots + I_{\text{rms},Q_{N-1}}\sqrt{K_{N-1}}}^{\sum_{j=1}^{N} I_{\text{rms},Q_j}\sqrt{K_j}}}{I_{\text{rms},Q_N}\sqrt{K_N}} \right) \\ &= W_N \left(\frac{\sum_{i=1}^{N} I_{\text{rms},Q_i}\sqrt{K_i}}{I_{\text{rms},Q_N}\sqrt{K_N}} \right). \end{aligned} \tag{22}$$

Rearranging (22), W_N can expressed as

$$W_N = W_{\text{total}} \left(\frac{I_{\text{rms},Q_N}\sqrt{K_N}}{\sum_{i=1}^{N} I_{\text{rms},Q_i}\sqrt{K_i}} \right). \tag{23}$$

Finally, by substituting (23) into (21), a generalized expression of the individual silicon width W_i with respect to the total die-size can be expressed as

$$\begin{cases} W_i = W_{\text{total}} \dfrac{I_{\text{rms},Q_N}\sqrt{K_N}}{\sum_{i=1}^{N} I_{\text{rms},Q_j}\sqrt{K_i}} \dfrac{I_{\text{rms},Q_i}\sqrt{K_i}}{I_{\text{rms},Q_N}\sqrt{K_N}} \\ = W_{\text{total}} \dfrac{I_{\text{rms},Q_i}\sqrt{K_i}}{\sum_{i=1}^{N} I_{\text{rms},Q_i}\sqrt{K_i}}; \quad i = 1, 2, \ldots, N. \end{cases} \tag{24}$$

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