Fully Integrated Digital Average Current-Mode Control Voltage Regulator Module IC

Eli Abramov, *Student Member, IEEE*, Timur Vekslender, *Student Member, IEEE*, Or Kirshenboim, *Student Member*, and Mor Mordechai Peretz, *Member, IEEE*

***Abstract*— This paper introduces a fully integrated 12-to-1.xV voltage regulator module IC. A fully synthesizable digital two-loop controller has been realized through hardware description language tools. Several new IP blocks have been developed and described in detail: a window delay-line-based analog to digital converter (DL-ADC), two independent PI compensators with shared hardware for calculations, high-resolution digital pulsewidth modulation (PWM), and a programmable dead-time module. To fully exploit the benefits of digital electronics, reduce power consumption, and save area, all units of the digital controller have been designed through asynchronous architecture, eliminating the need of high-speed clock. High-performance synchronized, fixed frequency, PWM operation is enabled by a digital programmable time-base generator and system governor, which has been developed as well. In addition, to extend the capabilities of the window DL-ADC to support the full range of the load with minimal hardware penalty, adaptive reference of the current compensation is introduced. The mixed-signal IC has been fabricated on a 0.18-μm 5-V CMOS process. It incorporates the digital controller and periphery as well as a synchronous buck power stage, including a drive circuitry that enables operation up to several megahertz from a 12-V input. The digital core has been realized by an automated synthesis process and place-and-route tools, resulting in an effective silicon area of 0.16 mm^2. Experimental results of the fabricated IC operating in closed loop are provided, demonstrating the performance and benefits of the new controller for meeting the requirements of tight output voltage regulation over wide load range.**

***Index Terms*— Average current-mode (ACM) control, dc–dc converters, digital control, power management IC, power system on-chip, pulsewidth modulation (PWM), voltage regulator module (VRM).**

I. Introduction

FOLLOWING the rapid growth in computing power and in particular for portable electronics, the specifications and restrictions on the power delivery have been significantly tighten to assure compact, light, energy efficient, and economical power sources. In voltage regulator module (VRM) and point-of-load applications, the requirements also extend to the transient response and to the closed-loop system performance. The efforts to accommodate these challenges range from the selection of the power devices, frequency of operation, through new topologies for switch-mode power supplies (SMPS), controller types, and more [1]–[5]. In recent years, the technology for on-chip integration of the power devices with the controller [6] and further advancements for co-packaging of the reactive components [7], [8] have enabled a new generation of compact, efficient, and economical VRMs.

In the worldwide trend of integration, digital design is predominant with several advantages such as convenience of the design, flexibility, scalability, and potential performance improvements. However, in power electronics and, particularly, in VRM applications, analog-oriented integration and analog controllers are the leaders [9], [11]. The main reason is that wide control bandwidth can be obtained without a significant penalty in the die area or power consumption. In order for a digital controller to be attractive and compete with an analog one, a low supply voltage process is preferred. This, however, introduces a tradeoff for a monolithic design, where the "real estate" for the power devices is rather costly, especially for over 5-V input. The main limiting factor of digital technology in integrated power processing applications is, therefore, that the controller architecture has not been optimized to the operation of the SMPS, but uses rather generalized cores to execute very specific tasks. It would be extremely efficient if the digital controller is *specifically tailored to the set of tasks required by the SMPS and can be realized through a simple design flow, with competitive sizing, on a similar process of the power devices*—this has been pursued in this paper.

State-of-the-art solutions that present architectures of integrated digital controllers propose several modifications of the two main peripheral units, i.e., the analog to digital converter (ADC) and the digital pulsewidth modulation (PWM) (DPWM) [12], [13]. One of the technology enablers can be identified as the use of delay lines (DL) as the primary building block for the ADC and DPWM. By doing so, the power consumption and a significant portion of the controller can be trimmed down without compromising performance [4], [13], [14], demonstrating the potential of the digital design. However, in many of the design modifications, it is required to custom design the delay cells, converting the design back to the analog domain, and losing some of the scalability features. Operation of digital controllers in either voltage mode (VM) or mixed-signal

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The authors are with the Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beersheba 8410501, Israel (e-mail: eliab@post.bgu.ac.il; timurv@post.bgu.ac.il; orkir@post.bgu.ac.il; morp@ee.bgu.ac.il).

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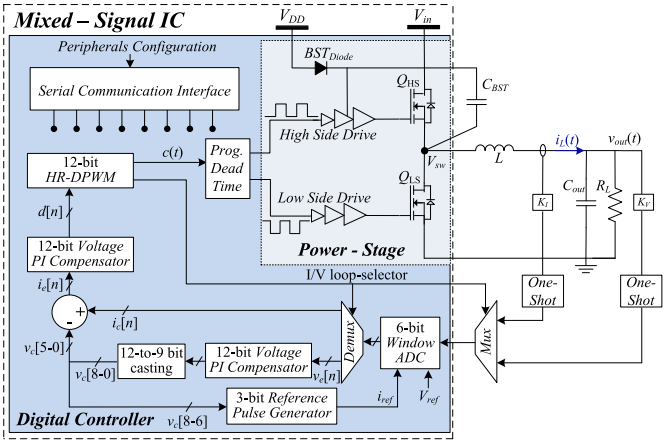

Fig. 1. Monolithic synchronous buck converter with the fully digital ACM PWM controller.

peak current-programmed mode (PCM) have been demonstrated in a variety of approaches [4], [7], [15]. There, the focus has been placed on creating an alternative to the conventional ADC and DPWM peripherals.

With the rise in the popularity of integrated VRMs, the recent evolution of methods for online efficiency optimization [13], [16], and current sharing for multiphase stages, where the information of the average current is essential, the advantages of average current-mode (ACM) control approach are becoming more apparent [17], [18]. Especially, in the case that it can be realized without additional hardware penalty. In addition, in ACM approach, some of the building blocks are identical for both the voltage and current loops, and therefore by using the same hardware, a significant reduction of the resources is achievable. For example, using the same ADC for sampling both voltage and current is an attractive attribute to save silicon area, lower power consumption, and reduce the complexity of the design. Through the evolution of digital controllers for SMPS, PCM control has been preferred over ACM that has been somewhat avoided. Nevertheless, identified by its advantages and moreover, by streamlined design methodology, ACM is recognized and gains popularity in recently released firmware-based (e.g., DSP) ACM controllers for single and multiphase such as [19]–[21]. There, the compensator is set by the operating conditions [19] and improves on a cycle-by-cycle basis [20], [21]. A primary challenge that stands, however, is to develop and realize a hardware efficient controller design that reduces the area and power consumption of the controller without compromising on the performance.

The objective of this paper is to introduce a new, ultracompact, digital architecture for ACM DPWM control that is entirely realized through hardware description language (HDL), i.e., by pure digital means without additional custom design. It is a further aim of this paper to detail the design of the integrated power stage for an input voltage range of 12 V, and finally, to present a fully monolithic VRM IC, as detailed in Fig. 1. The final IC architecture incorporates an integrated synchronous buck power stage that is realized by 5-V-gated lateral diffused MOS (LDMOS) power devices that have been designed to sustain up to 18 V and the required bootstrapped drive circuitry. The digital two-loop controller includes two independent discrete-time compensators that operate with joint hardware for calculations, a dual-channel 6-b DL-based window ADC that is realized without any analog hardware, a custom dual-frequency 12-b DPWM and system governor, a programmable dead-time unit, and a serial communication interface.

The rest of this paper is organized as follows. Section II describes the principle of operation of the new digital ACM controller. Section III details the architectures for the main units of the controller. Extension of a window ADC as a full-scale ADC with minor hardware penalty, to sample the inductor current with high accuracy throughout the full-load range, is delineated in Section IV. The IC implementation of the mixed-signal design, with emphasis on the power stage, and the digital core is described in Section V. Experimental results of the fabricated VRM IC are reported in Section VI. Section VII concludes this paper.

II. Digital Average Current-Mode Controller

Many current-programmed controller architectures reported in the literature or as commercial applications prefer the PCM method over ACM [6], [18], [21]. One of the main arguments for this is that PCM can achieve superior dynamics and offer cycle-by-cycle protection with simpler hardware. However, it has been shown in previous studies that the implementation of digital PCM requires significant hardware resources, mainly due to oversampling of the inductor current (significantly higher than the switching frequency) that is required to provide accurate current information and avoid limit-cycle oscillations [6], [23], [24]. In ACM control on the other hand, the required sampling is in the rate of the switching frequency, drastically reducing the resources required and simplifies the design [18]. From digital design perspective, the digital hardware requirements of ACM are equivalent or even lower than those of VM control due to the fact that shared hardware can be used for both current and voltage loops, since the compensation schemes may be of similar simple PI type (discussed in detail in Section III). To obtain high bandwidth using VM control, a proportional—integral—differential compensator is required and in terms of digital design, which may translate into higher hardware requirements. It should be noted, however, that since only one state variable is sensed in VM control, it is more economical in terms of the sensing circuitry. Adding the fact that no high-speed mixed-signal design or inductor current oversampling is required and it can be designed entirely by HDL description, ACM control becomes an attractive compensation type with benefits such as: less design efforts, lower hardware resources, and reduced power consumption of the overall system.

The principle of operation for the new digital ACM controller that has been realized in this paper is described with the aid of Figs. 2 and 3, which show a conceptual block diagram of the control system and a fundamental timing diagram, respectively. As can be seen in Fig. 2, the controller follows the classical two-loop ACM design with an all-digital outer

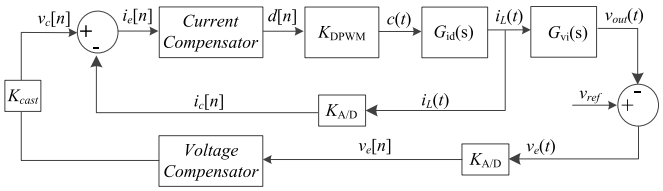

Fig. 2. Conceptual block diagram of the control system.

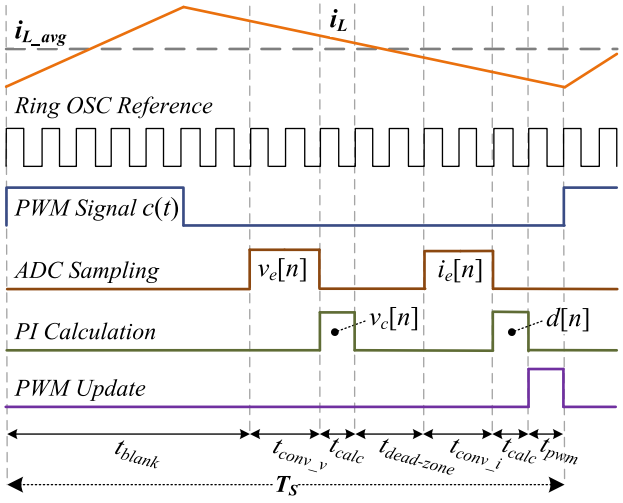

Fig. 3. Timing sequence of a typical steady-state switching cycle for the digital ACM.

voltage and inner current loops. The voltage loop creates a digital reference $v_c[n]$ based on the error signal of the voltage loop $v_e[n]$, for the average current value. The current error signal $i_e[n]$ is the input to a current loop compensator that generates the duty command $d[n]$ which is then sent to the DPWM, and a pulsewidth modulated signal $c(t)$ is created.

As detailed in Section III, each of the fundamental units has been implemented as an asynchronous hardware, using DLs and combinatorial circuits. By doing so, a significant portion of complex and power-hungry hardware for timing and high-speed synchronization is eliminated. Since DPWM is still a synchronized process, a system governor is employed to provide time base to the switching cycle and trigger the sequential operation of the functional blocks within the switching cycle. As can be seen in Fig. 3, the DPWM signal is sectioned into 16 equal intervals per switching period, which are derived from a DPWM based on an internal ring oscillator. The system governor also provides a programmable frequency selection by the number of intervals per switching period.

To facilitate sampling with high signal-to-noise ratio, it is preferred that the sampling event is triggered sufficiently away from the switching action [17], [25], [26]. Fortunately, within the context of VRMs, the ON time takes a relatively small portion of the switching period, allowing noise-clean sample throughout most of the cycle duration. In this paper, given a target conversion ratio, a blanking time window t_{blank} (see Fig. 3) is set from the beginning of the cycle to the trigger action of sampling the output voltage. Following a short period of $t_{\text{conv\_v}}$ to allow conversion of the ADC, a sample of the

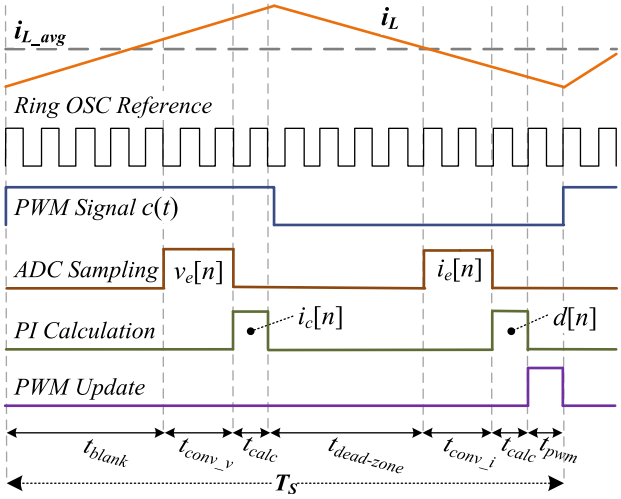

Fig. 4. Timing sequence waveforms of the controller for a possible switching cycle during loading transient. Adaptive tuning of t_{blank} to avoid sampling within the switching instance.

output voltage is obtained and a digital error signal $v_e[n]$ is generated. In the following interval t_{calc}, the current reference signal $v_c[n]$ is calculated by the voltage compensator.

It should be further emphasized that in the case of a load transient event or other circumstances that may lead to a significant increment of the ON time beyond t_{blank}, the sampling instance may slide onto the switching action. This undesirable case can result in an incorrect or noisy sampling. One possible practice to overcome this is by dual-edge modulation which provides relatively fast transients response [17], [18], [27]. Another possible practice to guarantee that the sampling event will not occur in the vicinity of the switching action is illustrated in Fig. 4, which shows an adaptive trimming of t_{blank} [25], [26]. In this paper, a programmable blanking period is used. The hardware is equipped with the possibility to set the blanking time based on loaded information on startup through the serial peripheral interface (SPI) periphery.

Since the same hardware is used for sampling of both the output voltage and inductor current, time multiplexing is employed. Sampling of the current takes place during the OFF time and is preceded by the interval $t_{\text{dead\_zone}}$ to allow the hardware multiplexers to switch between the ADC channels. Following a similar conversion interval $t_{\text{conv\_}i}$, a current error $i_e[n]$ is obtained and then the new duty command $d[n]$ is generated and is ready to be loaded onto the DPWM unit at t_{pwm}, before the beginning of the new switching period. It should be noted that average current sensing can be obtained with or without extra filtering of the inductor current. This is since the current information is obtained through one sample per cycle approach, thus filtering out the ripple information [28], [29]. It should be noted that the sampled current information not necessarily equals to its average value. This is due to the inductor current ripple and the location of the sampling with respect to the cycle and the instantaneous duty ratio, which results in an offset of the sampled value from the average. To accurately obtain the exact average value, many parameters are needed to the controller, which

significantly complicates its implementation. In addition, there is no apparent benefit, in terms of the regulation capability, from knowing the exact average value. The control scheme uses two control loops for current and output voltage, and as a result, any offset in the current sample is compensated by the voltage loop.

III. Digital Controller Architecture

The realization of the digital controller, shown in Fig. 1, relies on three key building blocks:

1) a dual-channel 6-b DL-based window ADC to obtain a sample of both the output voltage and inductor current;
2) a 12-b PI compensators generating the current reference $v_c[n]$ and duty-ratio command $d[n]$ signals;
3) a 12-b hybrid high-resolution DPWM (HR-DPWM) that generates the gate drive signals for $Q_{\rm HS}$ and $Q_{\rm LS}$ with a programmable dead-time option.

In the following it is assumed, without loss of generality, that the system's parameters are known or can be extracted or measured, i.e., information available on the input voltage $V_{\rm in}$, output voltage $V_{\rm out}$, output capacitance $C_{\rm out}$, inductor L and its dc resistance $R_{\rm DCR}$, the nominal load current $I_{\rm out}$, and the peripherals units gains.

A. Voltage and Current Compensator Design

As in any classical two-loop control method for PWM converters in which the effect of the state variables can be decoupled, the computational effort and the hardware complexity of the compensators can be reduced to a first-order system, resulting in PI-type compensation scheme [22], [30]. As mentioned in Section II, a major benefit of digital ACM control is the potential hardware sharing, and in this paper, a digital PI compensation has been realized for both the voltage and current loops with shared hardware (multiplier) on the basis of one sample per cycle [6], [25], [31]. There, a simple hardware realization can be achieved, resulting in the reduced power consumption and silicon area. Taking into account a sampling delay of one switching cycle, the compensator can be expressed by the difference equation as [31], [32]

$$v_c[n] = v_c[n-1] + a v_e[n] - b v_e[n-1] \tag{1}$$

where a and b are the compensator coefficients. Applying a conservative compensation design to assure stability with reasonable dynamics [33]–[35] and under the assumption that the inner loop is with a higher bandwidth than the outer loop, the coefficients can be calculated as

$$a = k_p, \quad b = k_p(1 - T_s/T_i) \tag{2}$$

where T_i is the integrator time constant which determines the compensator's zero, i.e., $T_i = 1/2\pi f_0$, and k_p is the compensator's proportional gain. The compensator coefficients are set so that the closed-loop goals for each loop are achieved for both phase margin and control bandwidth. The controller gain with respect to the control-to-output response of the loop determines the bandwidth, while the location of the PI's zero controls the phase margin. To satisfy stability with prescribed phase margin φ_m, the frequency of the compensator's zero f_0 is set using the following expression [22]:

$$f_0 = f_c\sqrt{\frac{1-\sin(\varphi_m)}{1+\sin(\varphi_m)}} = \frac{1}{2\pi T_I}. \tag{3}$$

Next, the control bandwidth is determined by setting the proportional gain k_p as the gain value at the target crossover frequency f_c for each loop, i.e., the gain values of k_{pI} and k_{pV} are inversely proportional to the overall gain of the inner current and outer voltage loops, respectively. With the aid of Fig. 2, the current compensator proportional gain k_{pI} can be found as

$$K_{PI} = \frac{1}{G_{\rm id}(s) K_I K_{\rm A/D} K_{\rm DPWM}} \tag{4}$$

where K_I is the gain due to the current sensing, $K_{\rm A/D}$ and $K_{\rm DPWM}$ are the gains of the peripheral units of the current loop, and $G_{\rm id}(s)$ is the control-to-output transfer function of the inner current loop, for buck converter it is given by

$$G_{\rm id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{\rm in}}{sL + R_{\rm DCR}} \tag{5}$$

where $V_{\rm in}$ is the input voltage, L is the inductor value, and $R_{\rm DCR}$ is the dc resistance of the inductor.

By substituting (5) into (4), and setting $s = 2\pi f_{cI}$ at the target crossover frequency of the current loop, (4) can be rewritten as

$$k_{pI} = \frac{2\pi f_{cI} L + R_{\rm DCR}}{V_{\rm in} K_i K_{\rm A/D} K_{\rm DPWM}}. \tag{6}$$

Next, in a similar manner to the current compensator, with the aid of Fig. 2, the voltage compensator proportional gain k_{pV} can be found as

$$k_{pV} = \frac{1}{G_{\rm vi}(s) K_V K_{\rm A/D} K_{\rm cast} \frac{1}{K_I K_{\rm A/D}}} \tag{7}$$

where K_V is the gain due to the voltage divider on the output voltage, and $K_{\rm cast}$ is the gain due to the matching between the number of bits of the voltage compensator and the accumulator (see Fig. 2). $G_{\rm vi}(s)$ is the control-to-output transfer function of the outer voltage loop, given by

$$G_{\rm vi}(s) = \frac{v_{\rm out}(s)}{v_c(s)} = R_L \frac{sC_{\rm out}R_{\rm ESR} + 1}{sC_{\rm out}R_L + 1} \tag{8}$$

where R_L is the load resistance and $R_{\rm ESR}$ is the equivalent series resistance of the output capacitor $C_{\rm out}$.

The design of the compensators, prior to the implementation, has been validated through Matlab simulations as a complete closed-loop system with a 12V-to- 1.5 V buck converter at a nominal output current of 1.5A, operating at 1.25 MHz where $L = 2.2\ \mu$H and $C_{\rm out} = 50\ \mu$F ($R_{\rm DCR} =$ 10m Ω; $R_{\rm ESR} = 2$ mΩ). The target closed-loop parameters were: for the inner (current) loop a crossover frequency of 250 kHz and phase margin of approximately 50o whereas for the outer (voltage) loop the crossover frequency has been aimed at 120 kHz with phase margin of 80°. The simulation results for the frequency responses of both loops are depicted in Fig. 5a and Fig. 5b. It should be emphasized that the

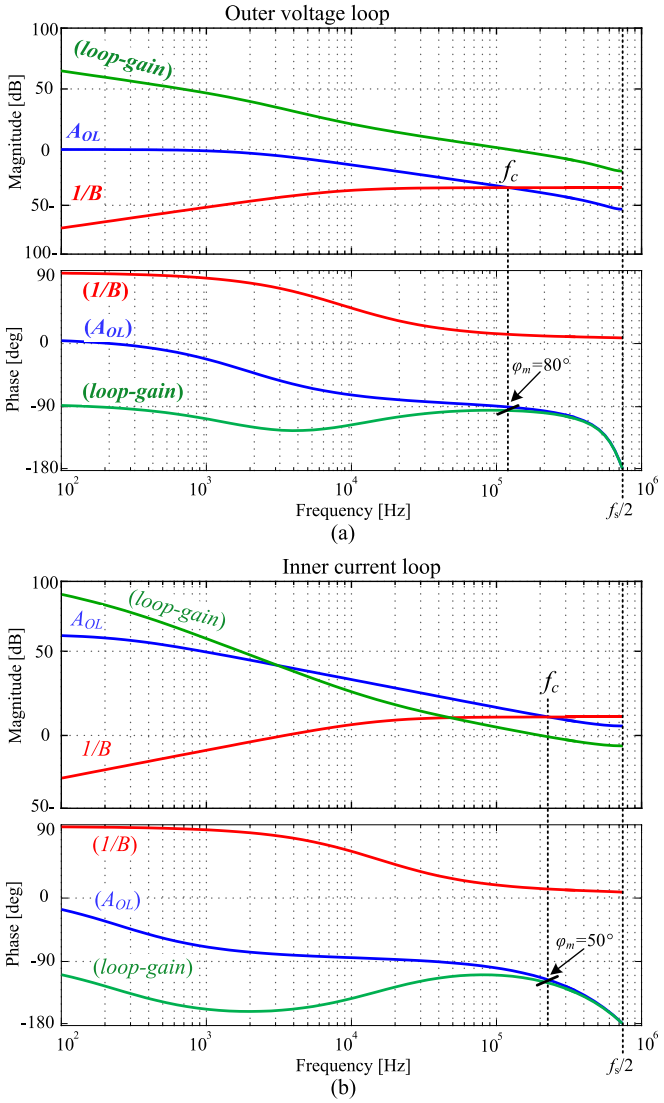

Fig. 5. Frequency responses of control-to-output A_{OL} (blue curves), inverse compensator $1/B$ (red curves), and the loop gain (green curves). (a) Outer voltage loop. (b) Inner current loop. Crossover frequency is marked f_c.

frequency responses shown in Fig. 5 are for the discrete-time representation of the control-to-output transfer functions, whereas a single-sample per cycle as well as computation delays are considered [25], [36]. The procedure of extracting the coefficients values based on the exact information of the converter'fs control-to-output response is based on an autotuning algorithm developed and detailed in [37]. Following the above analysis and observations, the discrete-time compensators coefficients have been found to be:

$$\begin{aligned} \text{current loop} \rightarrow a_I &= 0.24, \quad b_I = 0.2069 \\ \text{voltage loop} \rightarrow a_V &= 39.27, \quad b_V = 34.34. \end{aligned} \tag{9}$$

Since the final IC should function as a stand-alone device, the compensators' hardware architecture includes a small volatile memory, as a part of the serial communication interface (custom SPI in this paper) that is preprogrammed with a set of default values for the coefficients a and b according to (9). On startup, the default coefficient values can be used or a new set of coefficients can be loaded to the controller through the SPI. Then, the SPI internally communicates with the compensator units and loads the set of values per compensation loop. A benefit of this embedded feature is that the same controller hardware can be used with different power-stage configurations and parameters. Another reason for this feature is to support future development steps of online auto-tuning and adaptive control [26], [38]–[41].

B. Window DL-ADC

To achieve good regulation accuracy, a reliable sensing of the state variables is essential. In the digital domain, this requirement translates into a relatively HR measurement around the operating point. This has been facilitated in this paper by a window ADC [6], [13], [18], [42], where a small quantizer around the target point provides an accurate measurement with modest hardware. By doing so, the size can be significantly reduced, but more importantly, many of the full span linearity concerns of full-scale ADCs are removed. As oppose to many variations in the literature that use DLs for ADCs [5], [6], [42], the window ADC of this paper has been developed on the basis of standard-cell technology without any modifications.

The on-chip ADC, quantizes the difference between the sampled signal of $v_{\mathrm{out}}(t)$ or $i_L(t)$ and an internal reference V_{ref} or i_{ref}, respectively. The architecture of the 6-b window DL-ADC that is shown Fig. 6(a), follows a two-step conversion: a voltage-to-time conversion using a one-shot timer [43], followed by time-to-digital conversion using DL built of a string of digital buffers with fixed propagation time. Schematic of the one-shot timer is shown in Fig. 6(b), whereas the *RC* timing network is implemented off-chip. As can be observed, the one shot comprises of two input signals: one input V_{TRG} connects to the NOR operator and is used to trigger a timed output pulse V_{INV}. The second input receives the continuous-time (analog) sampled signal [$v_{\mathrm{out}}(t)$ or $i_L(t)$] to be used as the bias voltage for the *RC* timing network. Under steady-state conditions, V_{TRG} is low and the output of the NOR (V_{C1}) is high, thus the voltage node V_{C2} is pulled high through the resistor R up to the sampled signal level. As a result, timed output pulse of the one shot V_{INV} is pulled down to ground. Once the input trigger V_{TRG} is high, both V_{C1} and V_{C2} discharge to ground, and as a result, V_{INV} goes high. Due to the feedback between the output and input of the one shot, the NOR operator holds V_{C1} low. After the triggering event, the system settles down to steady state, as the voltage at node V_{C2} is pulled high since the capacitor C is now charged through R. The one-shot timer generates an output pulse that its duration is inversely proportional to the amplitude of sampled signal. The relationship between the generated pulselength T_{pulse} and the analog input signal can be expressed as

$$T_{\mathrm{pulse}} = \mathrm{RC} \cdot \ln\left(\frac{V_{\mathrm{DD}}}{V_{\mathrm{sample}} - V_{\mathrm{th}}}\right) \tag{10}$$

where V_{DD} and V_{th} are the logic and threshold voltages, respectively, and $V_{\mathrm{sample}}$is the value of the sampled signal [$v_{\mathrm{out}}(t)$ or $i_L(t)$].

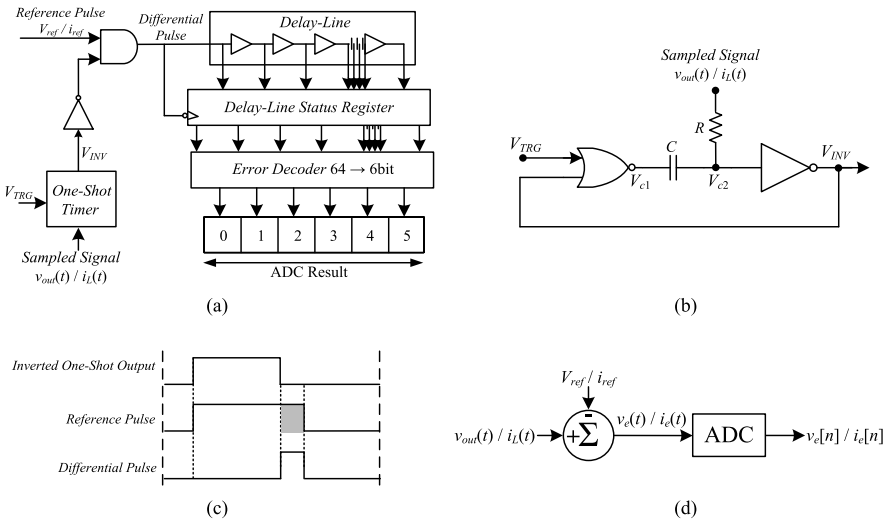

Fig. 6. (a) Simplified architecture of a 6-b window DL-ADC. (b) Schematic of the one-shot timer. (c) Timing diagram. (d) Equivalent functional block diagram of the window ADC.

By inserting the inversed one-shot output (sampled signal) and the reference pulse to an AND operator, a short pulse that represents the time difference between the pulses is obtained. This short pulse [named *differential pulse*, see Fig. 6(c)] duration is then calculated by the DL string to quantify the difference between the sampled signal and a reference value. At the end of the conversion, the differential pulse triggers the DL status register, which latches synchronously with respect to falling edge of the differential pulse. The residual time is captured as a thermometer code and then translated to a binary value. This implementation for a window ADC inherently includes subtraction between the sampled signal and a reference signal, as demonstrated in the equivalent diagram shown in Fig. 6(d). Therefore, no additional hardware is required to subtract the sampled signal from the reference signal and the difference is directly quantized. In addition, since the differential pulse is significantly shorter than the one shot or reference pulses, a shorter DL string is needed and it is independent of the pulses total duration.

C. Hybrid High-Resolution Digital Pulsewidth Modulator

In the context of digitally controlled SMPS, HR-DPWM is essential to avoid undesirable limit-cycle oscillations [44]–[46]. The conventional approach to implement HR-DPWM is by a fast-clocked counter-comparator scheme [13], [45], [47]. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n \cdot f_s$. This translates to increased power consumption and more complex design to realize the high-speed circuitry. Another approach to realize an HR-DPWM is based on tapped DL scheme [5], [6], [14]. In this method, the power consumption is reduced, but the required silicon area of the design grows exponentially with the number of resolution bits. Another potential design challenge of the tapped DL method is the design of the delay elements (DEs). In this paper, a combination of both methods [5], [48], [49] has been employed, i.e., by incorporating a coarse-counting block and then fine tuning it to the target delay. This allows a new hybrid design concept that is based on relatively lower operating frequency of the system governor with fine counting asynchronous DL. Furthermore, the new hybrid HR-DPWM can be implemented by compact standard cells, which enable direct synthesis. In addition, the silicon area as well as power consumption are reduced significantly.

A simplistic way to generate a DPWM signal using a time-delay method requires phase-detection-type operation between a reference signal and a delayed one. To increase accuracy and reduce the silicon area, the use of short delays (less than half switching cycle) is preferred. An exclusive-or operator is a simplistic phase detector, with narrow but sufficient dynamic range of half-cycle (180°); therefore, it is an ideal candidate to carry out the task. To accommodate the dynamic range, half-cycle padding is realized based on the duty-ratio command as follows. Assuming a given reference time base DCC_0 and a delayed signal $\mathrm{DLY}_{\mathrm{Fine}}$, the DPWM output for $D < 0.5$ can be obtained as

$$D < 0.5 \rightarrow c(t) = \left\{ \begin{array}{cc} \mathrm{DCC}_0 \oplus \mathrm{DLY}_{\mathrm{Fine}}; & t < T_s/2 \\ \text{'0'}; & T_s/2 \le t \le T_s \end{array} \right\} \Leftrightarrow \mathrm{DCC}_0 \& \overline{\mathrm{DLY}_{\mathrm{Fine}}} \quad (11)$$

and for $D \ge 0.5$ the padding is adjusted as

$$D < 0.5 \rightarrow c(t) = \left\{ \begin{array}{cc} \text{'1'}; & t < T_s/2 \\ \mathrm{DCC}_0 \oplus \mathrm{DLY}_{\mathrm{Fine}}; & T_s/2 \le t \le T_s \end{array} \right\} \Leftrightarrow \mathrm{DCC}_0 | \overline{\mathrm{DLY}_{\mathrm{Fine}}} \quad (12)$$

from (11) and (12), the combined logic is simplified to few basic operators.

The next challenge in generating the DPWM signal is to create a delayed signal from the reference with high resolution, but with simple hardware. This has been facilitated by a combined coarse-fine digital counter, as described in Figs. 7 and 8, which also show the conceptual architecture and timing diagram for the HR-DPWM unit that has been realized in this paper. As can be seen, it consists of three

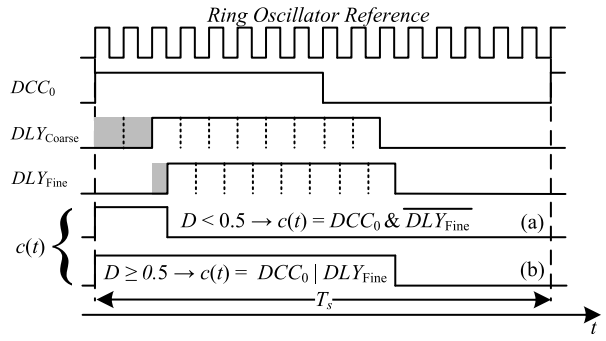

Fig. 7. HR-DPWM operation for cases. (a) $D = 15.5\%$; d[11-0] = "**0**01010000000." (b) $D = 65.5\%$; d[11-0] = "**1**01010000000."

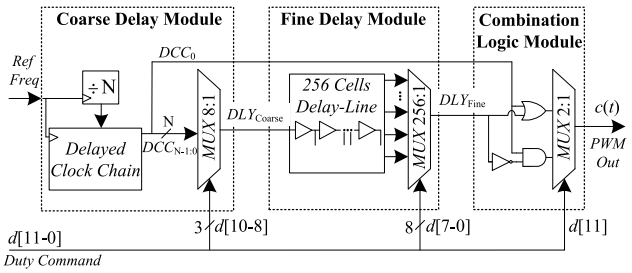

Fig. 8. Simplified architecture of 12-b HR-DPWM.

functional blocks: a coarse delay module, a fine-delay unit, and a logic block. The 12-b digital word for the duty ratio d[11-0] is distributed within the three modules. The course delay block is fed by a reference clock (generated by a ring oscillator) and three upper bits d[10-8], it generates two signals; first is a time base DCC_0, also used for the switching period. The second is a coarse-delayed version of the time base DLY_{Coarse} with time intervals derived from the reference clock as prescribed by d[10-8]. The latter is facilitated by a delay clock chain [50]. The fine-delay unit is a string of 8-b-long DL that finely adjusts DLY_{Coarse} by the number of DEs as specified by d[7-0], creating the HR delayed signal DLY_{Fine}. The logic block applies the required operation of either (11) or (12) on DCC_0 and DLY_{Fine} based on the MSB d[11]. The switching frequency of the HR-DPWM can be expressed as function of the number of bits and the propagation time of a single DE $t_{pd,DE}$(of the fine-delay module) as

$$f_s = \frac{1}{t_{pd,\mathrm{DE}} 2^{N+M}}; \begin{cases} N - \text{number of course bits} \\ M - \text{number of fine bits.} \end{cases} \quad (13)$$

D. Programmable Dead Time

To facilitate switching of the power devices without shoot through, it is necessary to control the gate-driving signals with proper dead time, such that the power transistors Q_{HS} and Q_{LS} (Fig. 1) turn ON does not overlap. Another important task of an adjustable dead-time unit is to improve the efficiency of the converter [51]; therefore, a programmable dead-time module has been developed. It consists of a string of 200 DEs connected to an eight-channel multiplexer, as shown in Fig. 9. In a similar manner to the compensators' coefficients setup, the dead time t_{DT}, set within the SPI memory register with initial default value, and can be programmed from 1 up to 40 ns.

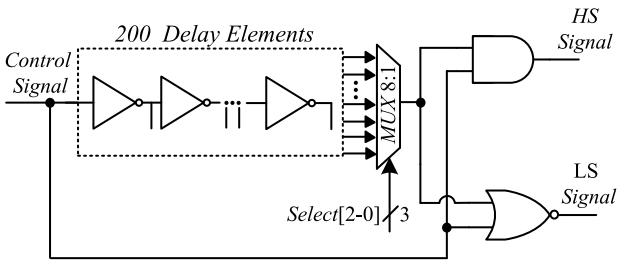

Fig. 9. Schematic of a programmable dead-time module based on DL.

IV. Full-Load Range Current Compensation Loop

Accurate acquisition of the state variables by the ADC is a major factor to facilitate a reliable compensation loop. Selection of the type of an ADC to be used primarily depends on the compensation type and the set of tasks required. Requirements for accuracy, resolution, dynamic range, acquisition, and conversion time may significantly vary with respect to the control scheme. For voltage regulation purposes, aside for a case that requires rapid voltage scaling, a window-based ADC with relatively narrow range is sufficient since the control objective is for regulation around a fixed or slow-changing reference value. However, the current compensator tracks the inductor current through the entire range of the load (from zero to nominal value), and therefore requires a full-scale and accurate ADC to support the wide variety of loading conditions and fast-changing dynamics. Since a window-type ADC has relatively limited range, its use in the current compensation loop sets a tradeoff in either poor current definition for the full-load range or high current definition for a narrow load range. Both options are not viable for a high-performance SMPS. In several commercial digital controllers, such as [19], [52], and [53] with comparable performance, the current sensing is obtained by a full-scale fast ADC or by the full-range ADC that is also used for protection purposes. Variable reference setting is used based on the expected operation range of the load.

In this paper, to exploit the advantages of the window DL-ADC compared to a full-scale ADC, a new approach that extends the acquisition range to a full-scale has been developed. That is, to use a window DL-ADC to accurately obtain the information of the inductor current for the full-load range, with the addition of simple hardware to the current compensation loop. Utilizing this method, a single window DL-ADC unit is used for both output voltage and inductor current, retaining the all-digital controller realization concept of this paper, and further reducing the overall hardware and silicon area of the controller. The core concept is to generate an *adaptive reference value* (reference pulse) with respect to the status of the inductor current value, such that the sampling window of the ADC is in the vicinity of the instantaneous inductor current. In current-mode control, the current reference is created by the output of the voltage-loop compensator $v_c[n]$

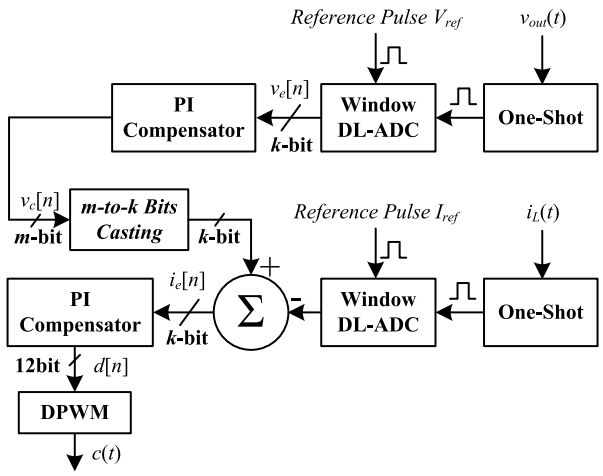

Fig. 10. Simplified block diagram of a current compensation loop with a constant current reference value.

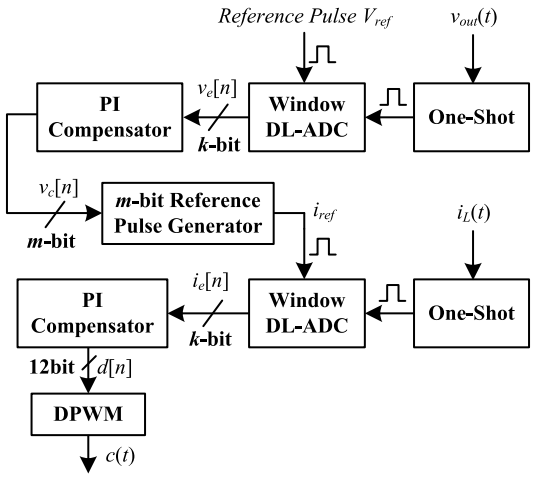

Fig. 11. Simplified block diagram of a current compensation loop with an adaptive current reference.

and provides the required information of the dynamic change that should be performed on the current reference value for the window DL-ADC. The current reference varies with respect to $v_c[n]$, similar to conventional analog current-mode control.

Fig. 10 depicts a simplified block diagram of the voltage and current compensation loops for the case that a window DL-ADC with a constant reference value for the voltage and fixed sampling window for the current. It should be noted that for the simplification of the illustration, two window DL-ADC blocks are illustrated, but in the practical realization, only one dual-channel window DL-ADC unit is used, sampling both the output voltage and inductor current. Here, to calculate the current error $i_e[n]$, the difference between the inductor current and a constant reference I_{ref} (which represents the fixed offset of the sampling window) is sampled and then subtracted from $v_c[n]$ to obtain the current loop reference. As mentioned earlier, this approach limits the dynamic range of the inductor current due to the limited dynamic range of the conventional window DL-ADC.

In the modification of this paper, $v_c[n]$ is used as the reference value for the inductor current, as described in Fig. 11.

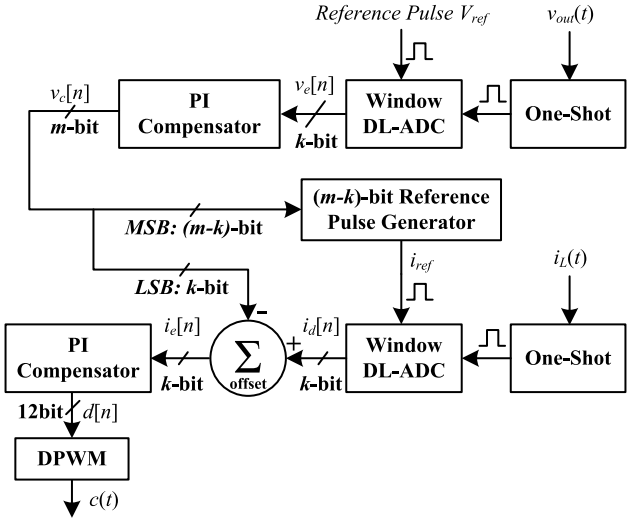

Fig. 12. Simplified block diagram of a current compensation loop with an adaptive current reference obtained by a segmented reference pulse generator.

Since the window DL-ADC employs time representation for its conversion, a reference pulse generator is added to convert $v_c[n]$ into an adaptive reference pulse. This approach provides an adaptive current reference that is generated based on the information of the required current reference, given by $v_c[n]$. By doing so, the window DL-ADC is used for the full-load range of the converter. The resolution of the reference pulse generator determines the resolution of the inductor current. This implies that the effective current resolution is given by

$$\frac{I_{L,\max} - I_{L,\min}}{2^m} \left[\frac{A}{\text{Bit}}\right] \tag{14}$$

where $I_{L,\max}$ and $I_{L,\min}$ are the maximum and minimum values of the inductor current, and m is the number of bits of the reference pulse generator.

To obtain high resolution of the inductor current and avoid undesired oscillations, the value of m should be set sufficiently higher than variation per bit of the voltage loop [54], [56]. This translates into relatively high hardware resources for the implementation of the reference pulse generator. To overcome this obstacle and simplify the design for the reference pulse generator, a new low-resources segmented reference generator has been realized, as demonstrated in Fig. 12. The segmented reference generator splits the value of $v_c[n]$ to MSBs and LSBs representation. The MSBs are used as the input for a low-resolution reference pulse generator for the window DL-ADC to facilitate a coarse-tuned current reference, while the LSBs are used as an offset that is subtracted from the output value of the window DL-ADC for fine tuning. By doing so, the value of $v_c[n]$ can be tuned to exactly match the current sample. For the description of the new approach's operation, steady-state is assumed, i.e., both the current and voltage errors are zero and the value of $v_c[n]$ corresponds to the actual inductor current. Due to the low resolution of the reference pulse, the output of the window DL-ADC $i_d[n]$ is nonzero. To compensate for this nonzero value of $i_d[n]$, the LSBs of $v_c[n]$ are subtracted from it, and the current error $i_e[n]$ is zero. Segmentation of the

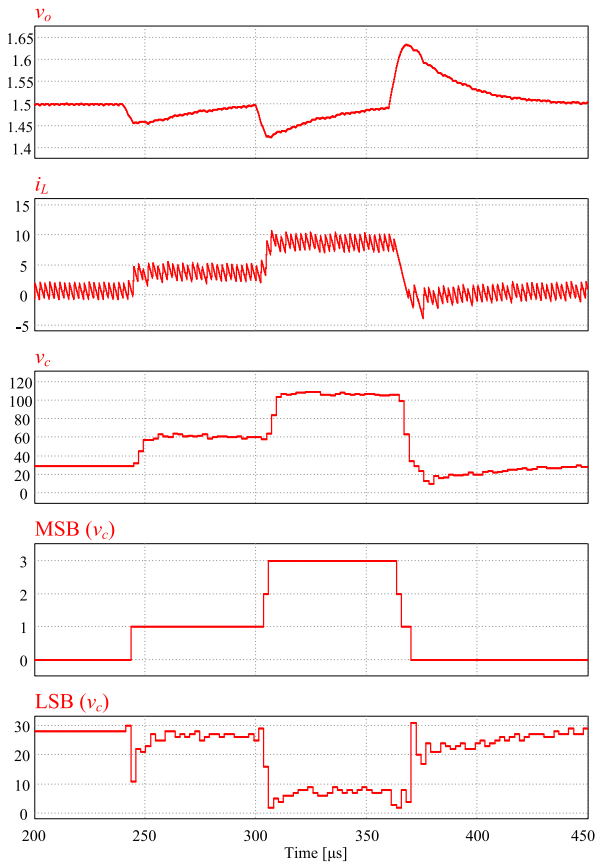

Fig. 13. Loading and unloading transients of a buck converter with the window DL-ADC and the segmented reference pulse generator.

MSBs and LSBs depends on the value of m and the number of bits of the window DL-ADC, defined by k. The minimal number of MSB bits is m-k, which guarantees that the value obtained by the window DL-ADC will not saturate due to its limited dynamic range of k bits. The selection of a minimum number of MSB bits results in the leanest and most efficient hardware requirements due to the fact that the pulse generator resolution is the lowest.

To verify the operation of the adaptive current reference with the segmented reference pulse generator and window DL-ADC for the full-load range, a PowerSim, Inc., simulation has been conducted. From the simulation results that are shown in Fig. 13, it can be observed that under various load transients the inductor current exactly follows the value of $v_c[n]$ for the full-load range with the window DL-ADC used to sample the inductor current. Also shown are the values of the two MSBs and five LSBs in decimal basis, i.e., for this case $m = 7$ and $k = 5$. The MSBs are used to change the reference pulse as a coarse reference tuning, and the LSBs are subtracted from the window DL-ADC result in order to maintain fine tuning of the reference. During steady state, there is no change in the MSBs, and the current reference is finely tuned exclusively by the LSBs. In the event of a load transient, a larger change in the current reference value is required, i.e., in $v_c[n]$, and therefore, the MSBs vary while the LSBs maintain the fine control of this reference to preserve it with high resolution.

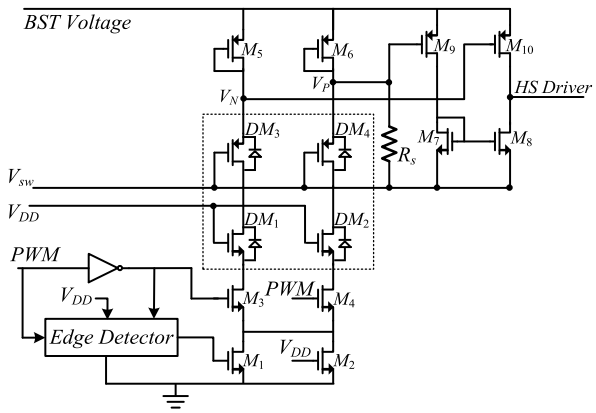

Fig. 14. High-voltage level shifter circuit.

V. Mixed-Signal IC Implementation

The mixed-signal IC of the VRM shown in Fig. 1 integrates power, analog, and digital circuits on one die. To satisfy proper operation, several layout constraints such as adding guard rings and isolation wells between devices have been employed to reduce coupling noise and undesired holes/electrons injections. This section primarily focuses on IC implementation, design considerations of the power stage, and the digital blocks' implementation procedure.

A. Power-Stage Implementation

The mixed-signal IC's synchronous buck power stage is constructed by N-channel devices for both the high-side (HS) switch and low-side switch. In this paper, these are realized by a 5-V-gated LDMOS power device [56]. The use of LDMOS allows higher voltage swing operation of a monolithic dc–dc converter, since its typical breakdown voltage is higher than the standard 5-V CMOS device. Each switch has a dedicated driving stage designed with a 5-V CMOS, whereas Q_{HS} transistor requires a bootstrap driver and floating level shifter configuration to overcome the limitations of a standard CMOS device breakdown voltage. The architecture and considerations of the HS level shifter is discussed in Section V-B. The driving stages have been realized by four dedicated custom designed buffers with high sinking-sourcing capabilities.

The switches have been designed symmetrically with an ON-resistance of 35 mΩ. The effective gate width W_g of the switches is 200 000 μm, obtained based on the target operating point derived from [57]. Each switch is constructed from 4000 fingers [58], creating a symmetrical quadrilateral layout pattern.

B. High-Side Level Shifter

The HS transistor is driven by a bootstrap configuration to assure proper driving signals of the power stage. By realizing such approach, the voltage drop on the level shifter is potentially a full rail-to-rail voltage swing from $V_{\text{in}}+5$ V to ground, damaging the CMOS device. One approach to overcome this issue is by designing the level shifter circuit with LDMOS devices only, which results in a significant larger die size and higher power consumption. The design approach implemented in this paper is shown in Fig. 14. It merges both CMOS and

LDMOS, such that several LDMOS devices (DM_1–DM_4) are used only in critical branches for absorbing high-voltage drop. A unique feature of the level shifter develop in this paper is that it does not require biasing circuitry for its operation and relies on the logic rail alone. This has been accomplished by appropriate sizing of transistors M_1 and M_2 with respect to V_{DD}, creating a self-biased level shifter circuit. The level shifter circuit is divided into three main subunits. First, an edge detector triggers the level shifter whenever the PWM signal changes. Second, the shifting unit constructed by DM_1–DM_4 to absorb the high-voltage drop to assure that the stress on M_1–M_4 does not exceed 5 V. Finally, a differential pair that saturates the differential change between V_P and V_N, such that the PWM signal voltage levels, V_{DD} and ground, are shifted to V_{sw} and $V_{sw} + 5$ V, respectively. The output signal of the differential pair controls the floating drive circuitry of the HS transistor.

The resistor R_s is added between V_{sw} and the positive branch V_{plus} of the shifting unit branches in order to intentionally cause a slight voltage difference between the branches. By doing so, the gate of the HS transistor is normally pulled down eliminating false enable or shoot-through current scenario that may be a result of an undesired noise. It should be noted that the value of R_s also determines the offset voltage between the branches. The matching of the differential pair's transistors M_9 and M_{10} primarily depends on the process variations [59]. This has been addressed in the layout stage by using common-centroid technique for M_9 and M_{10}, where M_7 and M_8 are also highly matched to achieve accurate active load operation [60]. Additionally, isolating guard rings to improve the noise immunity of the diff pair have been added.

C. Digital Implementation of ACM Controller

The realization of the digital controller relies on a digital implementation flow, using vendor's standard cells only. The digital implementation is carried out through two main steps. In the first step, the controller's units are described in HDL as stand-alone units for the simplicity of the verification and behavioral functionality simulations. Then, each unit is synthesized using synthesis and timing verification tools into an optimized gate-level representation, given a set of design constraints (such as skew and jitter and power consumption). The layout of each unit was generated by an automated place-and-route process. In the second step, all the units have been integrated together onto the higher hierarchy of the digital controller. Finally, the digital controller has been integrated with the power and analog units, creating the finalized digital ACM buck converter IC. The main characteristics of the digital controller including the digital core active area and current draw are summarized in Table I. It should be further emphasized that the controller's design scales with the technology, such that its overall area and power consumption can be significantly reduced by implementing it to a deeper sub-micrometer process.

To achieve good PWM regulation with digital control, and to avoid limit-cycle oscillations, it is required that the resolution of the DPWM is sufficiently high with respect to the resolution of the ADC [44]–[46]. This translates into a limitation on the maximum switching frequency that can be obtained by the digital controller, which then affects the overall size of the controller and the performance in closed loop. For a given $t_{pd,DE}$ of a single DE that equals 200 ps and a desired DPWM resolution is 12-b, using (13), the obtained switching frequency f_s is 1.25 MHz. From (13), it can be seen that f_s is inversely proportional to DPWM resolution, such that decreasing the resolution by a single bit will increase f_s by a factor of two. For the case of the lower operating frequency (620 kHz), the time base of 200 ps is preserved [46], [61], and implies that for 620 kHz, the DPWM resolution is increased by a single bit.

TABLE I
DIGITAL CONTROLLER MAIN CHARACTERISTICS

IC Block / Digital Core	*0.18μm CMOS*
Supply voltage	5V
$t_{pd,DE}$ buffer	200ps
DPWM resolution	12-bits
DPWM nominal frequency	1.25MHz
DPWM Si area	0.03 mm^2
ADC resolution	6-bit
ADC conversion time	20ns
ADC Si area	0.022 mm^2
PI calculation time	< 40ns
PI Si area	0.034 mm^2
Digital core current-draw	58μA/MHz
Effective digital core Si area including Ring-Oscillator, Dead-Time and SPI	0.16 mm^2

TABLE II
SUMMARY OF THE MIXED-SIGNAL IC CHARACTERISTICS

Specifications	*Value/Type*
Package	5x5 QFN - MLP
V_{in}	12V
Power-stage R_{on} LS/HS	~120mΩ, ~200mΩ
V_{out}	1.5V
Off Chip L, C_{out}	2.2μH, 50μF
Switching frequencies f_s	1.25MHz, 620kHz
Total chip Si Area	4.4mm^2

VI. CLOSED-LOOP EXPERIMENTAL VERIFICATION

A fully integrated digital ACM control VRM IC has been designed and fabricated in a 0.18-μm 5-V CMOS process; the chip micrograph is shown in Fig. 15(a), and Fig. 15(b) depicts the mixed-signal IC prototype on a printed circuit board (PCB). To demonstrate the operation of the digital controller and to validate closed-loop operation, the mixed-signal IC has been verified with experimental results, whereas the IC connects to an external filter of $L = 2.2$ μH and $C_{out} = 50$ μF. The VRM IC has been tested under two operating frequencies of 1.25 MHz and 620 kHz with a 12-V input. Experimental kelvin resistance measurements of the packaged IC converter report approximately 120 and 200 mΩ for the low side (LS) and HS switches, respectively. The deviation between the target ON-resistances (~35 mΩ) and the measured ON-resistances can be explained by bond wires and package limitations [62]. Table II summarizes the mixed-signal VRM IC main characteristics.

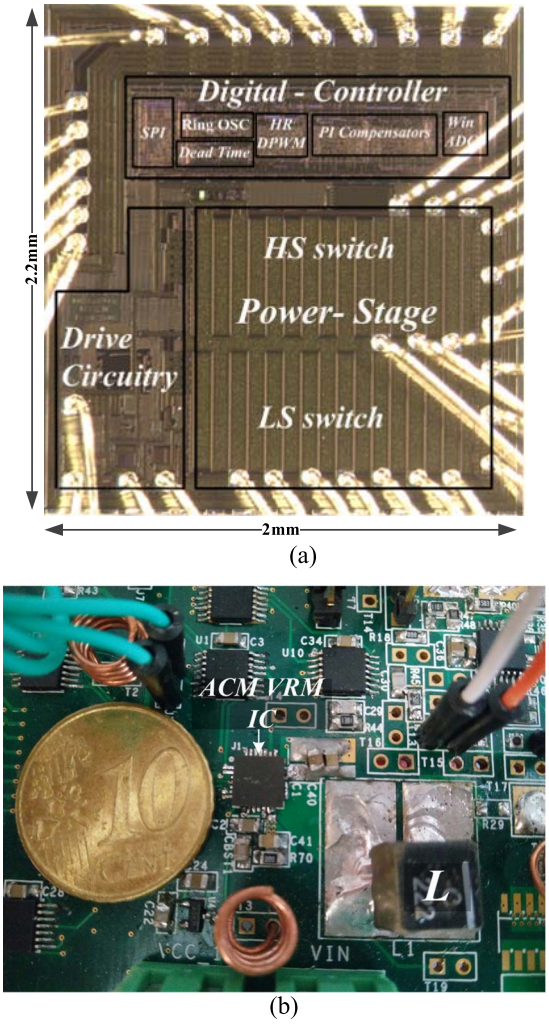

Fig. 15. (a) Micrograph of the fabricated fully integrated digital ACM control 12-to-1.x V VRM IC. (b) Chip prototype on PCB.

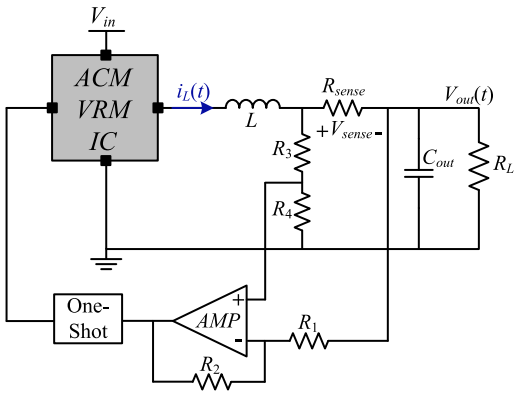

Fig. 16. Simplified circuit diagram of the current-sensing setup.

The current sensing for the inner current loop is obtained by an off-chip series–sense resistor setup [63], [64]. A precise power metal strip [64] sense-resistor R_{sense} has been inserted in series with the inductor, as shown in Fig. 16. Series-sense resistor is an accurate, simple, and cost-effective sensing technique with a stable temperature behavior. However, since the resistor is placed in the power path of the dc–dc converter,

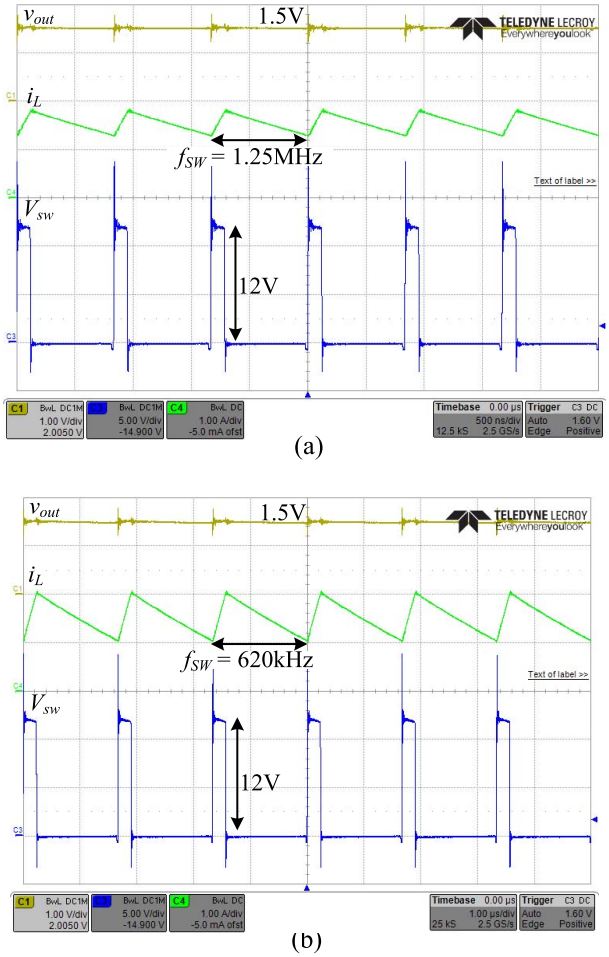

Fig. 17. Experimental steady-state results with a duty ratio of 0.125, whereas output voltage (top—yellow) 1 V/div, inductor current (middle—green) 1A/div, switching node voltage V_{sw} (bottom—blue) 5 V/div. (a) f_s = 1.25 MHz, time scale 500 ns/div. (b) f_s = 620 kHz, time scale 1 μ s/div.

potentially, a considerable amount of power can be dissipated through the resistor. Therefore, in this paper, $R_{\text{sense}} = 10$ mΩ has been chosen. Inductor current I_L is sensed by measuring the voltage difference V_{sense} across R_{sense}

$$V_{\text{sense}} = I_L R_{\text{sense}} \tag{15}$$

where sensed signal V_{sense} is amplified by the difference amplifier configuration to voltage levels suitable for the one-shot timer and controller operation.

Fig. 17 shows experimental steady-state waveforms of the closed-loop system, for 12-V input at 1.25-MHz and 620-kHz operation, and a duty ratio of 0.125. For both operating frequencies, smooth low-to-high and high-to-low transitions operation can be observed, validating the proper operation of the HS level shifter.

Experimental load transient responses of the VRM IC with a constant current reference value (nonadaptive current compensation loop) are shown in Figs. 18 and 19. Load transient events of 1.5 A and $V_{\text{out}} = 1.5$ V with operating frequency of $f_s = 1.25$ MHz are depicted in Fig. 18. An output voltage

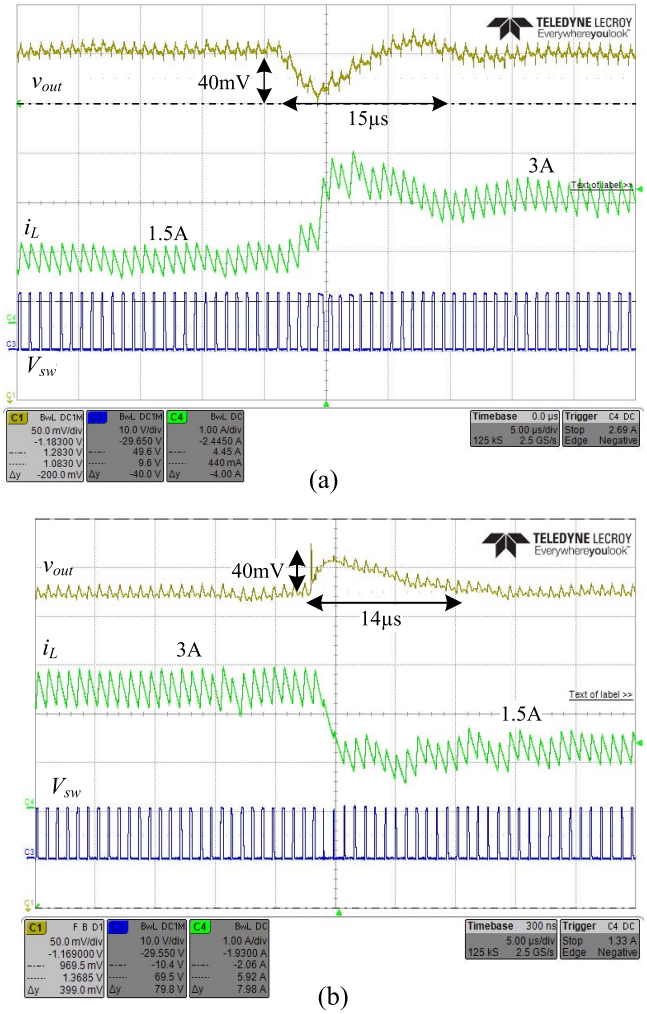

Fig. 18. Experimental results of 1.5-A (a) loading and (b) unloading transient events operating at 1.25 MHz, time scale 5 μs/div. Output voltage (top—yellow) 50 mV/div, inductor current (middle—green) 1 A/div, switching node voltage V_{sw} (bottom—blue) 10 V/div.

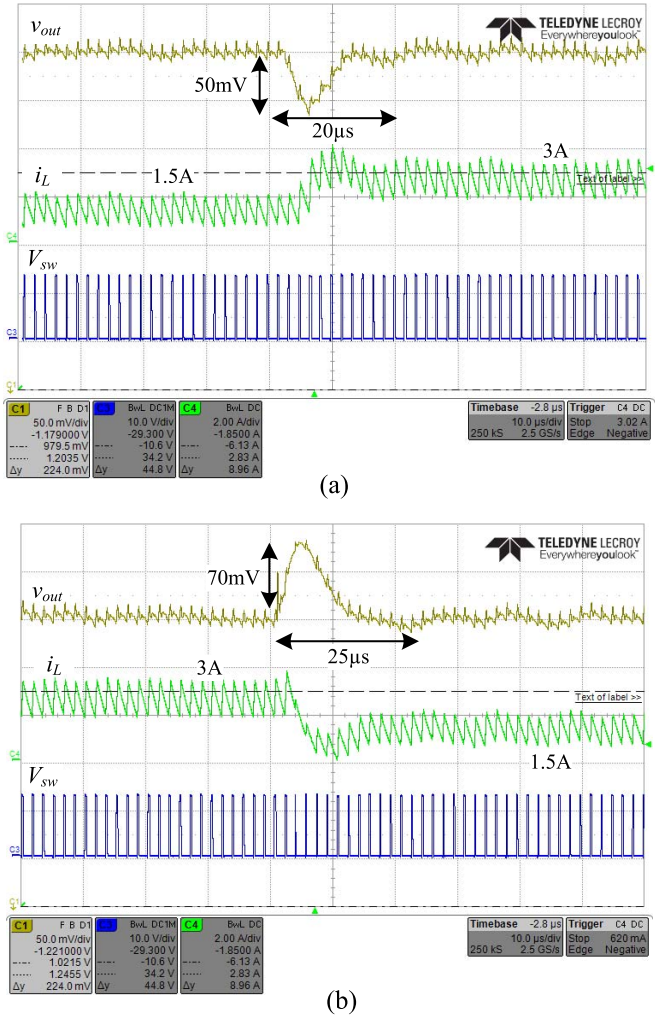

Fig. 19. Experimental results of 1.5-A (a) loading and (b) unloading transient events operating at 620 kHz, time scale 10 μs/div. Output voltage (top—yellow) 50 mV/div, inductor current (middle—green) 2 A/div, switching node voltage V_{sw} (bottom—blue) 10 V/div.

undershoot of 40 mV has been measured with a settling time of 15 μs. Fig. 18(b) shows the response of the converter to 1.5-A unloading transient, from 3 to 1.5 A. As can be observed, the output voltage overshoot is 40 mV, and 14 μs is the time it takes for the system to set back to the steady state. For operating frequency $f_s = 620$ kHz (Fig. 19), the loading transient event resulted in 50-mV undershoot and a settling time of 20 μs, whereas for the unloading event, the output voltage overshoot has been measured to be 70 mV and 25 μs for the settling time. Although rapid dynamics were not a primary objective of this paper, it can be observed that for both operating frequencies at the load transient events, the output voltage is well regulated with reasonable and comparable performance. It should be noted that due to the use of a constant current reference and the limited dynamic range of the window DL-ADC, the load transients' magnitudes were limited to 1.5 A. It can also be seen from Fig. 19 that the recovery from a loading transient is facilitated with moderate duty ratio increase, which may appear as limitation of the duty-ratio generation. The recovery pattern is a result of moderate bandwidth and gain settings of the controller that have been prescribed to satisfy a first-order type recovery when operating at lower switching frequency, and does not stem from limitations of the hardware. This assertion backed up the results of Fig. 18 which show better higher boosting of the duty ratio, for the same load transient, as a result of higher allowed controller gain when operating at higher switching frequency.

To further validate the new digital ACM controller approach and demonstrate the operation for a wider range of load changes, the experimental setup has been reassembled with $L = 1.5$ μH and $C_{\text{out}} = 300$ μF. Fig. 20 shows load transients of 5 A, at 12-to-1.5-V regulation. It can be observed that for 5-A loading transient [see Fig. 20(a)], the output returns to regulation within 60 μs and an overall output voltage undershoot of 80 mV. For 8- to 3-A unloading transient event [see Fig. 20(b)], the output voltage overshoot sums to be 85 mV, while the system settles down back to the steady-state conditions within 70 μs. As can be observed, well-regulated responses are obtained with reasonable and comparable dynamics.

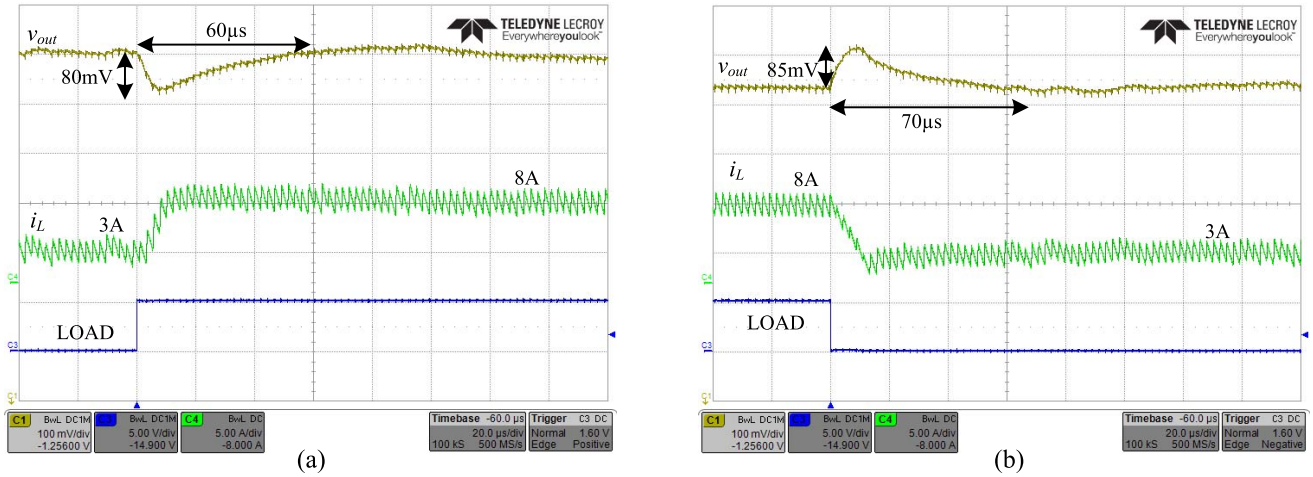

Fig. 20. Experimental results of 5-A load transient events transient responses. (a) Loading. (b) Unloading. Output voltage (top—yellow) 100 mV/div, inductor current (middle—green) 5 A/div. Time scale 20 μs/div. CH3—load step signal.

VII. Conclusion

A fully integrated digital ACM control 12-to-1.xV VRM IC has been presented. The mixed-signal design incorporates a two-loop digital controller with a monolithic power stage. In the controller design, three main components have been developed: a dual-channel ADC, 12-b HR-DPWM, and two independent PI compensators with a joint arithmetic core. Furthermore, by adding simple hardware to the current compensation loop, a new approach for window ADC with the ability to operate at full-load range has been developed and presented. The new low-resources window ADC combined with the compensators' shared hardware characteristics demonstrates a reasonably sized solution for IC control schemes, and enable smother transition toward the implementation of an entire digital controller. The VRM IC has been designed and fabricated on 0.18-μm 5-V CMOS process, operation demonstrated at 1.25 MHz and 620 kHz, and is capable of handling a 12-V input with tight output voltage regulation. The controller has been implemented on-chip by pure digital means without additional custom designs, resulting in the total silicon area of 0.16 mm^2, whereas the total silicon area of the chip is 4.4 mm^2. Various experimental results of the closed-loop operation demonstrated the performance and benefits of the new digital ACM controller approach over wide load range, and in particular in terms of area and power saving.

References

[1] J. Sun, D. Giuliano, S. Devarajan, J. Q. Lu, T. P. Chow, and R. J. Gutmann, "Fully monolithic cellular buck converter design for 3-D power delivery," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 3, pp. 447–451, Mar. 2009.

[2] E. A. Burton *et al.*, "FIVR—Fully integrated voltage regulators on 4th generation Intel Core SoCs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 432–439.

[3] P. S. Shenoy *et al.*, "A 5 MHz, 12 V, 10 A, monolithically integrated two-phase series capacitor buck converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 66–72.

[4] Z. Lukic, N. Rahman, and A. Prodić, "Multibit Σ-Δ PWM digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1693–1707, Sep. 2007.

[5] B. J. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[6] O. Trescases, A. Prodić, and W. T. Ng, "Digitally controlled current-mode DC–DC converter IC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 219–231, Jan. 2011.

[7] S. M. Ahsanuzzaman, A. Prodić, and D. A. Johns, "An integrated high-density power management solution for portable applications based on a multioutput switched-capacitor circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4305–4323, Jun. 2016.

[8] S. Sugahara, K. Yamada, M. Edo, T. Sato, and K. Yamasawa, "90% high efficiency and 100-W/cm^3 high power density integrated DC–DC converter for cellular phones," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1994–2004, Apr. 2013.

[9] Y. Qiu, J. Sun, M. Xu, K. Lee, and F. C. Lee, "Bandwidth improvements for peak-current controlled voltage regulators," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1253–1260, Jul. 2007.

[10] N. Keskar and G. A. Rincon-Mora, "Self-stabilizing, integrated, hysteretic boost DC-DC converter," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2004, pp. 586–591.

[11] Y. Panov and M. M. Jovanović, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.

[12] G.-Y. Wei and M. Horowitz, "A low power switching power supply for self-clocked systems," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, Aug. 1996, pp. 313–317.

[13] A. V. Peterchev, J. Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 356–364, Jan. 2003.

[14] Y. Halihal, Y. Bezdenezhnykh, I. Ozana, and M. M. Peretz, "Full FPGA-based design of a PWM/CPM controller with integrated high-resolution fast ADC and DPWM peripherals," in *Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Jun. 2014, pp. 1–6.

[15] A. Parayandeh, B. Mahdavikkhah, S. M. Ahsanuzzaman, A. Radić, and A. Prodić, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in *Proc. IEEE Energy Convers. Conf. Expo. (ECCE)*, Sep. 2011, pp. 1229–1235.

[16] S. H. Kang, D. Maksimović, and I. Cohen, "Efficiency optimization in digitally controlled flyback DC–DC converters over wide ranges of operating conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3734–3748, Aug. 2012.

[17] J. Chen, A. Prodić, R. W. Erickson, and D. Maksimović, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[18] H. Peng and D. Maksimović, "Digital current-mode controller for DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2005, pp. 899–905.

[19] *EM2130x01QI 30A PowerSoC Datasheet*, document 12873, Intel Enpirion Power Solutions, accessed: Dec. 2016. [Online]. Available: https://www.altera.com/enpirion

[20] *SI9136 Multi-Output Power-Supply Controller*, document 70818, Vishay Siliconix, accessed: Dec. 2014. [Online]. Available: http://www.vishay.com
[21] *Digital Dual-Phase Synchronous Buck Controller Datasheet*, document pv3012, Rohm Semiconductors, accessed: 2015. [Online]. Available: http://www.rohm.com
[22] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer, 2001.
[23] S. Chattopadhyay and S. Das, "A digital current-mode control technique for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1718–1726, Nov. 2006.
[24] Y.-S. Jung, "Small-signal model-based design of digital current-mode control," *IEE Proc.-Electr. Power Appl.*, vol. 152, no. 4, pp. 871–877, Jul. 2005.
[25] M. M. Peretz and S. Ben-Yaakov, "Time-domain design of digital compensators for PWM DC-DC converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 284–293, Jan. 2012.
[26] M. M. Peretz and S. Ben-Yaakov, "Time-domain identification of pulse-width modulated converters," *IET Power Electron.*, vol. 5, no. 2, pp. 166–172, Feb. 2012.
[27] K. Lee, P. Harriman, and H. Zou, "Analysis and design of the dual edge controller for the fast transient voltage regulator," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2009, pp. 1184–1189.
[28] D. Maksimović and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.
[29] R. B. Ridley, "A new small-signal model for current-mode control," Ph.D. dissertation, Elect. Eng., Virginia Polytech. Inst., Blacksburg, VA, USA, Nov. 1990.
[30] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioural relationships," *Int. J. Electron.*, vol. 77, no. 5, pp. 731–746, 1994.
[31] M. Ilic and D. Maksimović, "Digital average current-mode controller for DC–DC converters in physical vapor deposition applications," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1428–1436, May 2008.
[32] M. M. Peretz and S. Ben-Yaakov, "Revisiting the closed loop response of PWM converters controlled by voltage feedback," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2008, pp. 28–64.
[33] R. B. Ridley, B. H. Cho, and F. C. Y. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators (power supply circuits)," *IEEE Trans. Power Electron.*, vol. PEL-3, no. 4, pp. 489–498, Oct. 1988.
[34] G. F. Franklin and J. D. Powell, *Digital Control of Dynamic Systems*. Reading, MA, USA: Addison-Wesley, 1998.
[35] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with *LCL* filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380–388, Feb. 2009.
[36] V. Yousefzadeh, N. Wang, Z. Popovic, and D. Maksimović, "A digitally controlled DC/DC converter for an RF power amplifier," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 164–172, Jan. 2006.
[37] T. Vekslender, E. Abramov, O. Kirshenboim, and M. M. Peretz, "Hardware efficient digital auto-tuning average current-mode controller," in *Proc. IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Jul. 2017, pp. 1–8.
[38] B. Miao, R. Zane, and D. Maksimović, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1093–1099, Sep. 2005.
[39] A. Kelly and K. Rinne, "A self-compensating adaptive digital regulator for switching converters based on linear prediction," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2006, pp. 712–718.
[40] Z. Zhao, H. Li, A. Feizmohammad, and A. Prodić, "Limit-cycle based auto-tuning system for digitally controlled low-power SMPS," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2006, pp. 1143–1147.
[41] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of digitally controlled buck converters based on relay feedback," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2005, pp. 2140–2145.
[42] G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari, "Delay-line-based analog-to-digital converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 6, pp. 464–468, Jun. 2009.
[43] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ, USA: Wiley, 2010.
[44] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.
[45] H. Peng, A. Prodić, E. Alarcon, and D. Maksimović, "Modeling of quantization effects in digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 208–215, Jan. 2007.
[46] M. M. Peretz and S. Ben-Yaakov, "Digital control of resonant converters: Resolution effects on limit cycles," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1652–1661, Jun. 2010.
[47] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 1997, pp. 21–28.
[48] V. Yousefzadeh, T. Takayama, and D. Maksimović, "Hybrid DPWM with digital delay-locked loop," in *Proc. IEEE Comput. Power Electron. (COMPEL)*, Jul. 2006, pp. 142–148.
[49] A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, "High-efficiency multiple-output DC-DC conversion for low-voltage systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 3, pp. 252–263, Jun. 2000.
[50] J. D. Kershaw, *Digital Electronics: Logic and Systems*. Belmont, CA, USA: Wadsworth, 1976.
[51] J. A. Abu-qahouq, H. Mao, H. J. Al-atrash, and I. Batarseh, "Maximum efficiency point tracking (MEPT) method and digital dead time control implementation," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1273–1281, Sep. 2006.
[52] EXAR. *40 V Quad Output Digital PWM/PFM Universal PMIC*. Accessed: Dec. 2014. [Online]. Available: https://www.exar.com/product/power-management/universal-pmics/universal-pmics/xr77129
[53] *Digital Multi-Phase Controller With PMBus Interface for VR12.5*, document 3910, MPS, Sep. 2015. [Online]. Available: https://www.monolithicpower.com
[54] A. K. Singha, S. Kapat, S. Banerjee, and J. Pal, "Nonlinear analysis of discretization effects in a digital current mode controlled boost converter," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 3, pp. 336–344, Sep. 2015.
[55] S. Kapat, "Selectively sampled subharmonic-free digital current mode control using direct duty control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 3, pp. 311–315, Mar. 2015.
[56] K. Sung and T. Won, "High-side N-channel LDMOS for a high breakdown voltage," *J. Korean Phys. Soc.*, vol. 58, no. 5, pp. 1411–1416, 2011.
[57] M. Rodríguez, Y. Zhang, and D. Maksimović, "High-frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May 2014.
[58] A. Yoo, M. Chang, O. Trescases, and W. T. Ng, "High performance low-voltage power MOSFETs with hybrid waffle layout structure in a 0.25 μm standard CMOS process," in *Proc. 20th Int. Symp. Power Semiconductor Devices IC's*, May 2008, pp. 95–98.
[59] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA, USA: McGraw-Hill, 2001.
[60] A. Hastings, *The Art of Analog Layout*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2001.
[61] M. M. Peretz and S. Ben-Yaakov, "Digital control of resonant converters: Frequency limit cycles conditions," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2009, pp. 1705–1708.
[62] E. Abramov, A. Cervera, and M. M. Peretz, "Optimal design of a voltage regulator based resonant switched-capacitor converter IC," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 692–699.
[63] H. P. Forghani-Zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, vol. 2. Aug. 2002, pp. 577–580.
[64] *Components and Methods for Current Measurement*, document 30304, Vishay Siliconix, accessed: Aug. 2015. [Online]. Available: http://www.vishay.com

Eli Abramov (S'15) received the B.Sc. degree in electrical and electronics engineering from the Sami Shamoon College of Engineering, Beersheba, Israel, in 2006, and the M.Sc. degree in electrical and computer engineering from Ben-Gurion University of the Negev, Beersheba, in 2016, where he is currently pursuing the Ph.D. degree with the Center for Power Electronics and Mixed-Signal IC.

His current research interests include power and analog IC, mixed-signal integration for power management systems, power system on-chip, and digital control techniques for power converters.

Timur Vekslender (S'15) received the B.Sc. degree in electrical and electronics engineering from the Sami Shamoon College of Engineering, Beersheba, Israel, in 2013, and the M.Sc. degree in electrical and computer engineering from Ben-Gurion University, Beersheba, in 2017.

He is currently a Senior ASIC Design Engineer with the Research and Development Center, Western Digital Corporation, Omer, Israel. His current research interests include digital control techniques for power converters, mixed-signal IC design for power management systems, power system on-chip, and digital implementation.

Or Kirshenboim (S'15) was born in Haifa, Israel, in 1987. He received the B.Sc. and M.Sc. degrees in electrical and computer engineering from Ben-Gurion University of the Negev, Beersheba, Israel, in 2013 and 2015, respectively, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

His current research interests include digital, nonlinear and smart control methods for SMPS, hybrid voltage regulation solutions, high-voltage conversion ratio converter topologies, pulsed power applications, and batteries balancing topologies.

Mor Mordechai Peretz (S'05–M'12) was born in Beersheba, Israel, in 1979. He received the B.Tech. degree in electrical engineering from the Negev Academic College of Engineering, Beersheba, in 2003, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from Ben-Gurion University of the Negev, Beersheba, in 2005 and 2010, respectively.

From 2010 to 2012, he was a Post-Doctoral Fellow with the Laboratory for Power Management and Integrated SMPS, University of Toronto, Toronto, ON, Canada. In 2012, he joined the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, where he is currently the Director of the Center for Power Electronics and Mixed-Signal IC. His current research interests include digital and smart control methods for efficient energy processing, switch-mode power supplies (SMPS) miniaturization, mixed-signal IC design of SMPS, modeling and computer-aided design, applications of nonlinear magnetics, and renewable energy systems.

Dr. Peretz serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.