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Closed-Loop Design and Transient-Mode Control for a Series-Capacitor Buck Converter

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***Abstract* - This paper explores the large-signal and small-signal dynamics of a series-capacitor (SC) buck-type converter and introduces an optimal closed-loop control scheme to accommodate both the steady-state and transient modes. As opposed to a conventional buck converter, where time-optimal control is realized by a single on-off cycle, in the SC-buck topology there is a need to distribute the switching phases to satisfy the charge-balance of the series-capacitor. The new control method merges a voltage-mode controller for steady-state operation and a non-linear, state-plane based transient-mode controller for load transients. A detailed principle of operation of the SC-buck converter is provided and explained through an average behavioral model and state-plane analysis. The operation of the controller is experimentally verified on a 20W 12V-to-1V converter, demonstrating voltage-mode control operation as well as minimum-deviation and time-optimal responses for load transients.**

Keywords— Time-optimal control, state-space control, dc-dc converters, voltage regulation.

I. INTRODUCTION

IN recent years, a significant effort is made to enhance the performance of voltage regulator modules (VRMs) for high-performance integrated circuits that operate with low supply voltage and high current. Tight output voltage regulation, high efficiency, and accommodating load transients are key factors in the design of the switch-mode power supplies (SMPS), in particular for high step-down conversion ratio applications. Several converter topologies and circuit extensions have been discussed in the literature to minimize the size of passive components and improve the dynamics of the VRM. One direction of VRM implementation is based on multi-phase interleaved converters, allowing high frequency operation and size reduction at the cost of complex control for current sharing [2]-[3]. Another approach is by multi-level converters where the lower component stress allows better sizing of the components and efficiency improvement [4], [5].

The series-capacitor (SC) buck converter, also known as a double step-down two-phase buck converter, originally presented in [6] and revised in [7]-[11], merges a two-phase interleaved buck converter with a switched-capacitor front-end and by doing so allows high frequency operation in the MHz range and better system dynamics with reduced components' stress. Additional attractive features of the SC-buck converter are natural current sharing between the phases and effectively doubling the switches' on-time, which make it suitable for high conversion ratio applications.

Recent studies have quantified the attributes of the SC-buck topology at high frequency [12], [13] and demonstrated improved light load efficiency when operating in DCM [14]. Further extensions presented a two-phase, four-inductor, converter which emphasizes its current sharing feature when the power is distributed between multiple phases [15]. Although the converter's topology has been widely and thoroughly investigated [9], dynamic analysis and digital controller design for the topology and its derivatives have not been systematically explored. It would be a further value to examine the converter suitability for time-optimal controller assignment in order to be considered attractive for VRM applications.

The objective of this study is therefore to investigate the dynamic features of a SC-buck converter and to introduce an optimal closed-loop digital controller that merges a voltage-mode compensation for steady-state operation and a non-linear control law for load transients, as detailed in Fig. 1. In this study, two modeling approaches are presented, the first is by an average-behavioral model to examine the small-signal control-

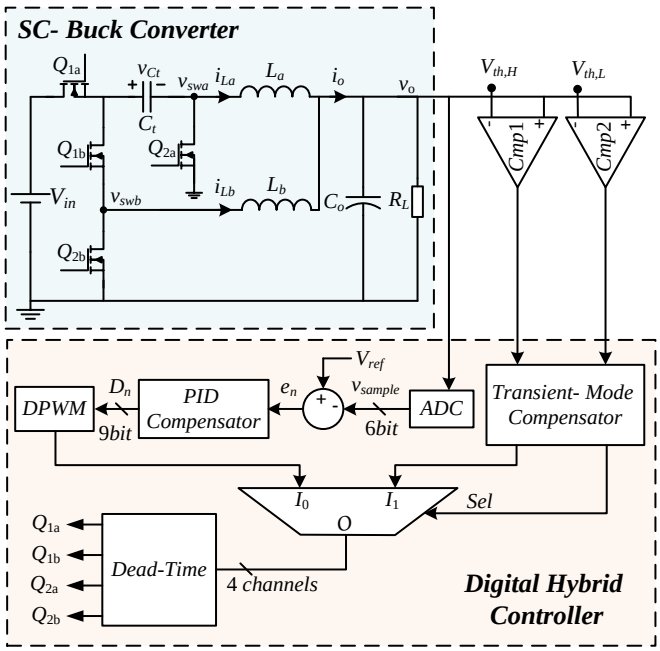

Fig. 1. SC-buck converter and a hybrid controller

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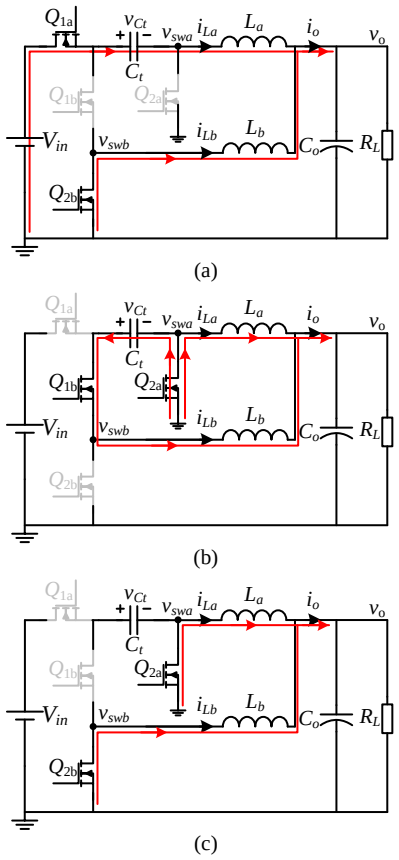

Fig. 2. Current paths in switching-states of the SC-buck converter: (a) State-1, (b) State-3, (c) State-2 and State-4.

to-output response and design a discrete-time voltage-mode controller. The second method is to obtain a state-space representation which will be the basis for the design of a non-linear minimum-deviation and time-optimal controllers for load transients. The design and definition of the non-linear controllers are significantly more challenging in the context of the SC-buck converter since they involve four state-variables compared to two state-variables in the case of a conventional buck converter.

The rest of the paper is organized as follows: Section II describes the steady-state operation of the converter, extracts an average-behavioral model representation, and provides a design procedure of a discrete-time voltage-mode compensation scheme, with survey and discussion on the effects of sampling and compensation on multi-phase type buck converters. Section III provides a large-signal analysis and state-space modeling, minimum-deviation control algorithm, effect of the series-capacitor on the transient performance and potential remedies using a time-optimal control algorithms of the SC-buck converter and detailed simulation results. Fully detailed and demonstrated experimental setup of the all the key novelties are presented in Section IV. Section V concludes the paper.

II. Steady-State Operation and Voltage-Mode Controller

The description of the SC-buck converter is assisted by the topology structure and typical waveforms, as shown in Fig. 2 and Fig. 3, respectively. The steady-state operation is similar to

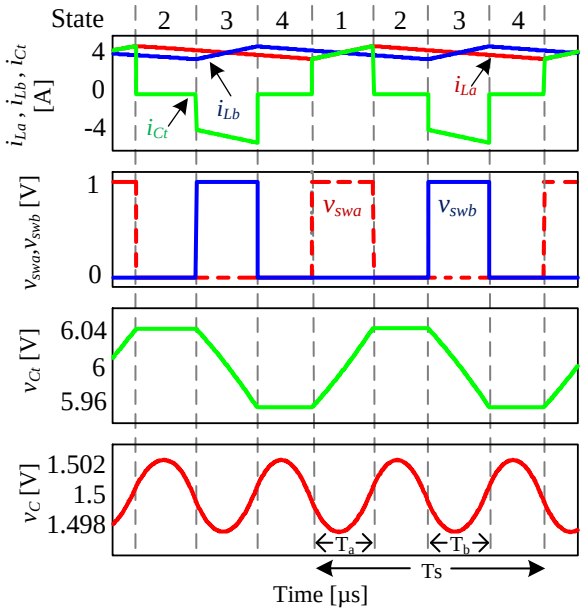

Fig. 3. Typical waveforms of a SC-buck converter.

that of an interleaved, two-phase buck converter with a slight difference that the back-end converter is fed by a series-capacitor C_t that is charged to approximately $V_{in}/2$. The duty-ratio for both phases (a and b) is identical and each phase is time-interleaved with a 180° phase delay. As a result, four switching-states are identified. In state-1, Q_{1a} and Q_{2b} are on, resulting in v_{swa} that equals $V_{in}/2$ and the inductor current i_{La} ramps up with a slew-rate of $(V_{in}/2-V_o)/L_a$ and i_{Lb} ramps down with a slew-rate of $-V_o/L_b$. In state-2, Q_{1a} is turned off, Q_{2a}, Q_{2b} are on, and the operation resembles a conventional buck converter in off state. In state-3 Q_{2a} and Q_{1b} are on, C_t acts as the source for phase b, and the inductor current i_{Lb} ramps up with a slew-rate of $(V_{in}/2-V_o)/L_b$ while i_{La} ramps down with a slew-rate of $-V_o/L_a$. State-4 is identical to state-2. Charge balance of C_t is naturally maintained by this operation allowing both charge and discharge action per cycle [7], and for equal on-times of phase a and b, this naturally stabilizes v_{Ct} to half the input voltage.

Following the switching sequence and assuming CCM operation, the behavioral operation of the converter is obtained by averaging [16]-[17]. The average voltage across the inductors, $\langle v_{La} \rangle$, $\langle v_{Lb} \rangle$ and the average capacitor current $\langle i_{Ct} \rangle$ can be expressed as:

$$\langle i_{Ct} \rangle = D_a i_{La} - D_b i_{Lb} \tag{1}$$

$$\langle v_{La} \rangle = D_a \left(V_{in} - V_{Ct} \right) - V_o \tag{2}$$

$$\langle v_{Lb} \rangle = D_b V_{Ct} - V_o \ , \tag{3}$$

where $D_a=T_a/T_s$ and $D_b=T_b/T_s$ are the duty-ratios related to the conduction time of Q_{1a} and Q_{2a}, respectively. V_o is the output voltage and T_s is the switching period.

Fig. 4 shows a graphical representation for an average-behavioral model as described by (1)-(3). As mentioned earlier, the duty-ratios for both phases are equal, i.e. $D_a=D_b=D$. By

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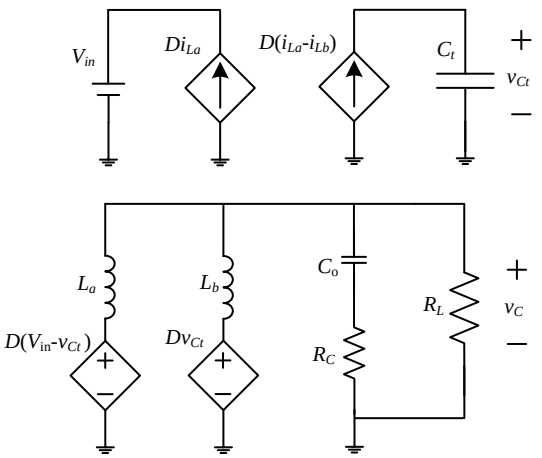

Fig. 4. Average-behavioral model of the SC-buck converter.

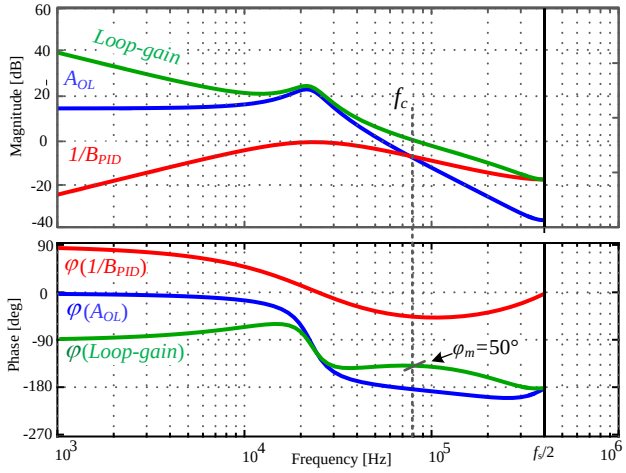

Fig. 5. Frequency responses of: control-to-output A_{OL} (blue), inverse compensator $1/B_{PID}$ (red), and the Loop-Gain (green). Crossover frequency is marked f_c.

applying small-signal linearization, the full control-to-output transfer function can be obtained. To simplify the expressions, V_{Ct} is assumed constant by small-ripple approximation [18], resulting in a control-to-output expression of the form:

$$\frac{v_o}{d}(s)=\frac{\frac{V_{in}}{2}\left(sC_oR_c+1\right)}{s^2\frac{C_o\left(L_a\parallel L_b\right)}{R_L}\left(R_L+R_c\right)+s\left(C_oR_c+\frac{L_a\parallel L_b}{R_L}\right)+1} \quad (4)$$

As can be observed from (4), this expression is similar to the control-to-output response of a classical two-phase buck converter with half the input voltage. A typical frequency response of (4) is depicted in Fig. 5 along with the required compensator that its design is detailed in the next sub-section.

A. Closed-Loop Discrete-Time Compensator Design

To satisfy the requirements for loop-gain stability and high bandwidth, the crossover frequency f_c of the closed-loop system is chosen to be one tenth of the switching frequency while the target phase margin is set to be above 50°. Based on the control-to-output transfer function behavior, the setting of the target parameters in this way guarantees suitability for PID compensation scheme [19]. The extraction of the PID coefficients (a,b,c) is based on the methodology that has been presented in [20] with minor adjustments to a frequency-domain design. The design procedure is as follows:

- Specify the crossover frequency fc and the phase margin of the desired closed-loop A_{CL}(s) frequency response based on a knowledge of the control-to-output response A_{OL}(z).
- Obtain the denominator of A_{CL}(z) by a pole-zero matching s-to-z transformation.
- Derive the numerator of A_{CL}(z) such that the closed-loop response is of second order system [20].
- Derive the transfer function of an ideal compensator B_{ideal}(z) that yields the desired closed-loop response.
- Obtain the response of a template PID compensator B_{PID}(z) from the first three samples of the ideal compensator B_{ideal}(z) by evaluation of difference equations.

The designed PID compensator has been validated through Matlab simulations as a full closed-loop system with a 12V-to-1V SC-buck converter, operating at 800 KHz (L_a=L_b=0.5 µH; C_t=10 µF; C_o=200 µF). The target closed-loop parameters are crossover frequency of 80 KHz and phase margin of 50°. Fig. 5 shows the frequency response of the converter (blue), the $1/B_{\text{PID}}$ of the PID compensator (red) and the loop-gain (green), where the expressions for these discrete transfer functions are given in (5). It should be noted that the time delay due to the discrete implementation is taken into account and causes an additional phase shift at high frequencies close to $f_s/2$ [20].

$$A_{OL}(z)=\frac{0.0416z+0.0007382}{z^2-1.959z+0.9661}$$
$$B_{PID}(z)=\frac{15.34z^2-27.77z+12.59}{z^2-z} \quad (5)$$
$$LG(z)=\frac{0.6381z^3-1.144z^2+0.5032z+0.009292}{z^4-2.959z^3+2.925z^2-0.9661z}$$

B. Sampling and Compensation

In conventional operation of switch-mode converters, the correction command (which can be the duty-ratio, on-time, off-time or frequency) is obtained once every switching cycle. As a result, in the context of control and modeling their dynamic behavior, such converters can be viewed as sample-data systems [21], [22]. This attribute fundamentally relates to the synchronized operation of the converter and therefore, variations within the switching cycle are so-called transparent to a linearized compensation scheme. In single-phase converters, it is considered superfluous to obtain information of the state-variable (e.g. the output voltage) more than once per switching cycle [23], [24]. On the other hand, in multiphase and interleaved converters, the correction rate of the control command can be expedited by a factor of the number of units that are employed, effectively improving the control bandwidth [25], [26]. That is, while each of the units operates at the base frequency, the effective frequency at which the system can be updated is multiplied by the number of units that are affecting the state-variable under regulation.

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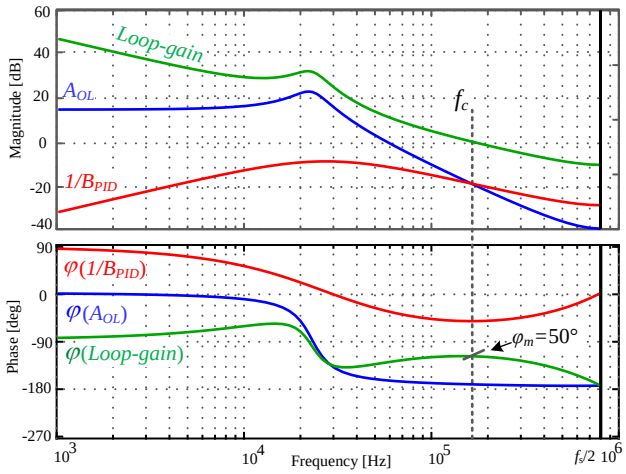

Fig. 6. The frequency responses for sampling the output at $2f_s$: control-to-output A_{OL} (blue), inverse compensator $1/B_{PID}$ (red), and the Loop-gain (green). Crossover frequency is marked f_c.

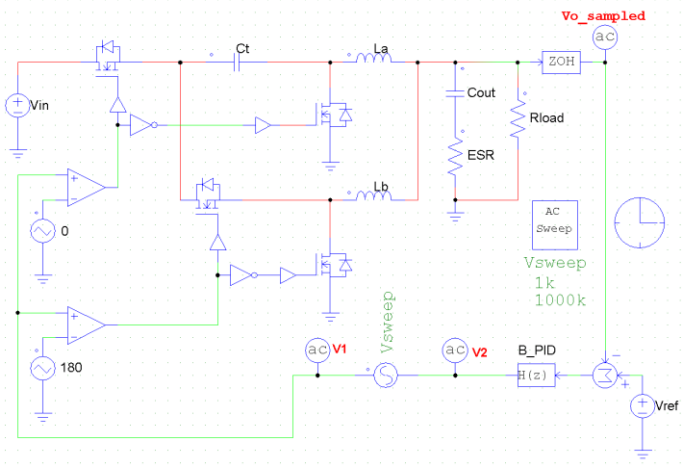

Fig. 7. PSIM simulation circuit setup for obtaining the small-signal frequency response using a cycle-by-cycle simulation.

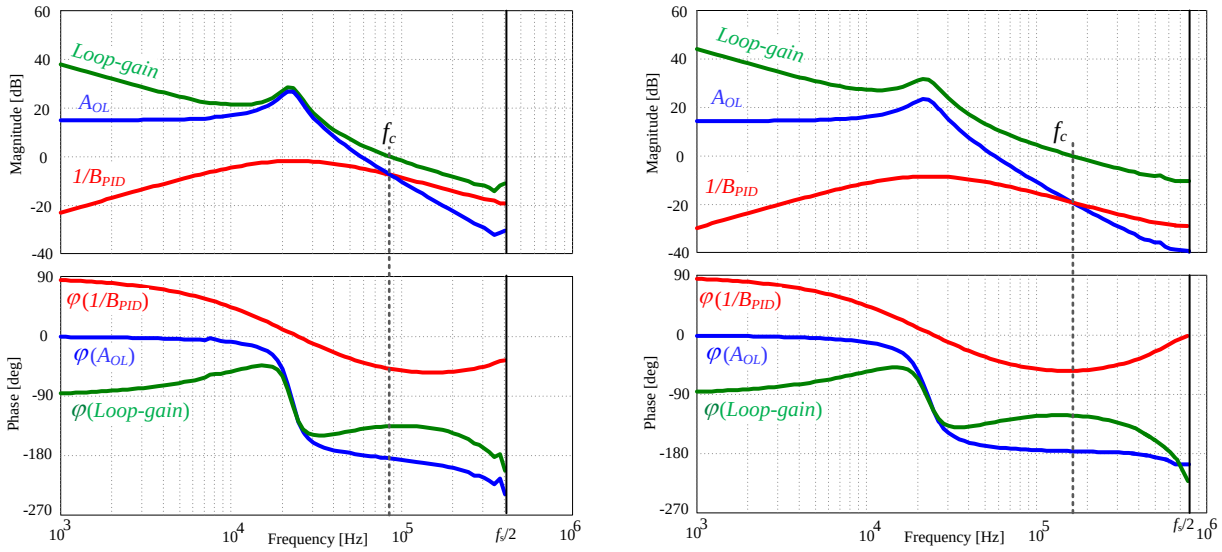

Fig. 8. Small-signal frequency response obtained by a cycle-by-cycle simulation for: (a) sampling and compensation at f_s, (b) sampling and compensation at $2f_s$.

As opposed to a conventional single-phase converter, the operation of the SC-buck converter and the effect on the output voltage resembles more an interleaved one. The duty-ratio command can be updated twice per switching cycle since each of the phases is shifted by 180°, effectively doubles the rate that the output voltage can be regulated. The observer, i.e. in the case of digital realization the ADC, samples the output voltage at its ripple frequency of $2f_s$, and therefore the design of the controller can be fully optimized to achieve a loop-gain with higher bandwidth. The effect on the control-to-output frequency response can be viewed by comparing Figs. 5 and 6, which demonstrate double bandwidth of the loop-gain from 80 KHz (Fig. 5) to 160 KHz as shown in Fig. 6 because of sampling and compensation at $2f_s$.

To verify the results that have been predicted theoretically and plotted using Matlab, a small-signal frequency response of the SC-buck has been extracted through a cycle-by-cycle simulation using PSIM. The simulation circuit setup is depicted in Fig. 7, where V_{sweep} is the excitation for the ac-sweep, the open-loop is given by $A_{OL}=V_{o\_sampled}/V_1$, the controller is given by $B_{PID}=V_2/V_{o\_sampled}$ and the loop-gain is given by $LG=V_2/V_1$. The resultant frequency responses for sampling and compensating at f_s and $2f_s$ are shown in Fig. 8(a) and Fig. 8(b), respectively. As can be observed, the results are in excellent agreement with the theoretical analysis.

Fig. 9 shows the different timing diagrams for the compensator operation for the case where the output voltage is sampled and the duty-ratio command is updated at the base frequency (Fig. 9(a)), and the case where the output voltage is sampled and the duty-ratio command is updated twice in every switching cycle (Fig. 9(b)). It can be seen that the higher sampling frequency reduces the time delay response of the controller from a maximum of T_s to a maximum of $T_s/2$, since in every instance there is a phase that can respond to a change in the duty-ratio command from the controller. It is important to note that this modification can be applied on the compensator of the SC-Buck converter without major hardware changes in the digital controller.

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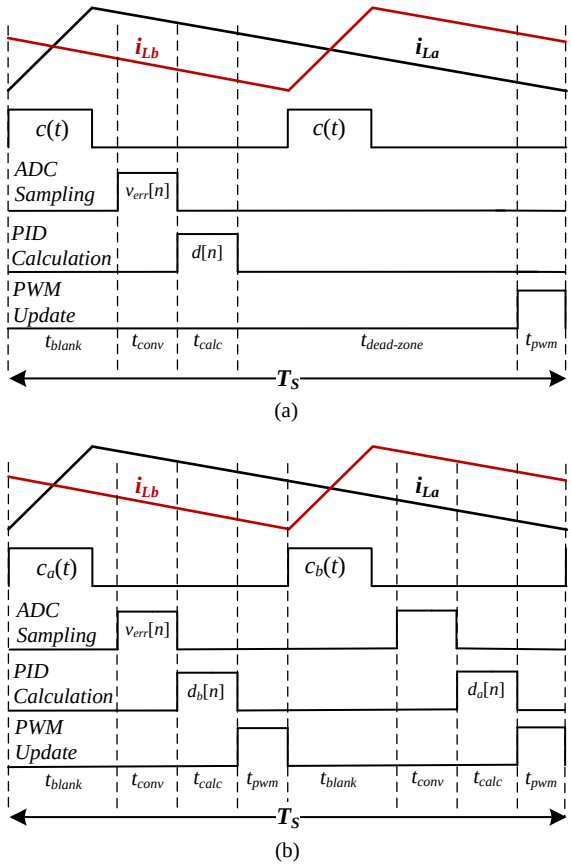

Fig. 9. Comparison of timing sequence: (a) one sample per switching period, (b) two samples per switching period.

To evaluate the difference between sampling once every cycle and twice every cycle, a simulation case study of an 800 KHz SC-buck converter response to a 10A loading transient has been conducted and its results are shown in Fig. 10. It can be observed that, due to the higher loop-gain bandwidth, the output voltage undershoot is reduced from 100mV to 60mV, and the settling time has been trimmed from 25µs down to 12µs when sampling at $2f_s$.

III. State-Space Representation, Minimum-Deviation Control and Time-Optimal Control

To further enhance the performance of the SC-buck converter when dealing with load transients, it is essential to obtain the information of the possible state-trajectories of the converter in order to recover to the new steady-state operating point from a load transient. To facilitate the desired rapid recovery of the converter, a transient-mode controller is used in addition to the steady-state controller. In this study, a voltage-mode controller is assumed for steady-state operation and therefore the objective of the transient-mode controller is to minimize the output voltage deviation and/or recovery time of the converter in load transients, i.e. to generate a minimum-deviation [27], [28] or time-optimal responses [29]-[37]. This approach of using a dedicated transient-mode controller to handle load transients significantly reduces the burden and design requirements from the steady-state controller since it does not handle any load transients by itself. This way, the design of the steady-state controller can be loosen since it only has to maintain a zero voltage error at steady-state and handle the small mismatch

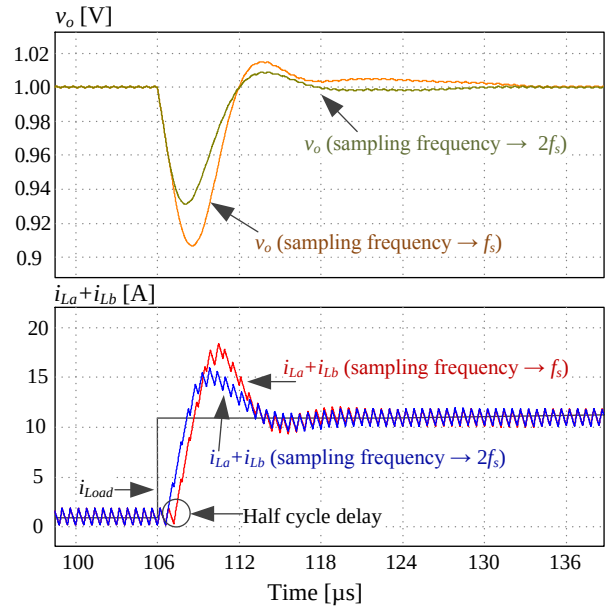

Fig. 10. Simulation results showing the differences in a 10A loading transient response between the cases of using a sampling frequency of f_s and $2f_s$.

between the inductors currents and load current that may occur at the end-of-transient instance. Unlike a conventional two-phase buck converter, in the SC-buck converter case, charge balance of the series-capacitor must be satisfied during the transient time to allow smooth transition back to the steady-state operation. This implies that the 'simple' on-off time-optimal cycle as carried out by many applications would not hold in this case and, as a matter of fact, would worsen the overall performance.

To realize the required switching sequence, the first task is to map the behavior of the state-variables with respect to the new load conditions [38]-[41], then the required switching sequence can be derived from the trajectories' map of the state-variables on the state-plane. It should be noted that for simplicity of the following analysis, parasitic components, e.g. ESR and ESL, are neglected since it is found that they have relatively minor effect [42].

The state equations for state-1 can be expressed as:

$$\frac{dv_C}{dt} = \frac{1}{C_o}\left(i_{L_a} + i_{L_b} - \frac{v_C}{R_L}\right), \tag{6}$$

$$\frac{di_{L_a}}{dt} = \frac{V_{in} - v_{Ct} - v_C}{L_a}, \qquad \frac{di_{L_b}}{dt} = \frac{-v_C}{L_b}, \tag{7}$$

Substituting (6) into (7) and after some manipulations, the expression for i_{La} can be expressed as:

$$i_{L_a} = i_{L_a}(0) - \frac{L_a}{L_b}\frac{V_{in}/2 - v_C}{v_C}\left(i_{L_b} - i_{L_b}(0)\right), \tag{8}$$

where $i_{La}(0)$ and $i_{Lb}(0)$ are the inductors' currents at the beginning of state-1. As can be seen in (8), the current difference of i_{La} - $i_{La}(0)$ depends on the current difference of i_{Lb} - $i_{Lb}(0)$. It should be noted that since the same on-time is used for both states 1 and 3, the series-capacitor voltage automatically converge to $V_{in}/2$ [11], which is a typically the desired design.

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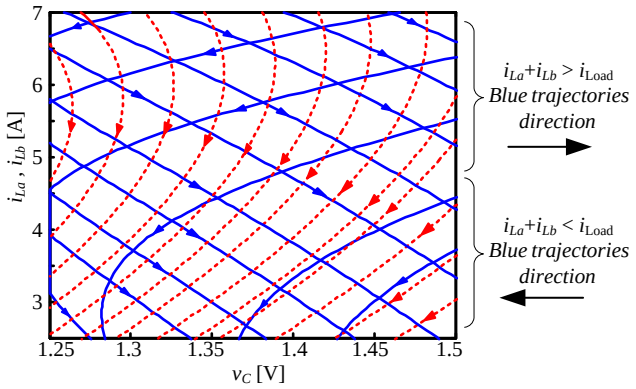

Fig. 11. State-space map for the SC-buck converter. On (states 1 and 3-solid-blue) and off (states 2 and 4 - doted red) trajectories.

Therefore, substituting (8) and (7) into (6) and assuming $v_{Ct}=V_{in}/2$ yields:

$$\frac{C_o}{3}v_C^{\,3}-L_b\frac{i_{L_b}}{R_L}v_C^{\,2}+\left(i_{L_b}^{\,2}L_b+i_{L_b}L_b i_{L_a}(0)-i_{L_b}L_b i_{L_b}(0)\right)v_C$$
$$+L_bV_{in}\left(\frac{i_{L_b}i_{L_b}(0)}{2}-\frac{i_{L_b}^{\,2}}{4}\right)+const_b=0 \qquad (9)$$

where $const_b$ is defined by the initial values of i_{Lb} and v_C at the beginning of state-1 The first solution of this function yields the state-1 trajectories of the converter in the form of $v_C=f(i_{Lb})$ with three initial conditions: $i_{La}(0)$, $i_{Lb}(0)$ and $v_C(0)$.

By symmetry in the operation of state-3 to state-1 and proper variable assignment, the state-trajectories for state-3 are derived from (9). The variables are assigned as: $v_{Ct}=V_{in}/2$, i_{La} swaps with i_{Lb}, and L_a swaps with L_b. This results in:

$$\frac{C_o}{3}v_C^{\,3}-L_a\frac{i_{L_a}}{R_L}v_C^{\,2}+\left(i_{L_a}^{\,2}L_a+i_{L_a}L_a i_{L_b}(0)-i_{L_a}L_a i_{L_a}(0)\right)v_C$$
$$+L_aV_{in}\left(\frac{i_{L_a}i_{L_a}(0)}{2}-\frac{i_{L_a}^{\,2}}{4}\right)+const_a=0 \qquad (10)$$

where $const_a$ is defined by the initial values of i_{La} and v_C at the beginning of state-3

States 2 and 4, which are the off states, are identical and the state equations can be expressed as:

$$\frac{dv_C}{dt}=\frac{1}{C_o}\left(i_{L_a}+i_{L_b}-\frac{v_C}{R_L}\right), \qquad (11)$$

$$\frac{di_{La}}{dt}=-\frac{v_C}{L_a}\ ,\ \frac{di_{Lb}}{dt}=-\frac{v_C}{L_b}, \qquad (12)$$

Using (11) and (12), the expression of i_{La} can be derived:

$$i_{L_a}=i_{L_a}(0)+\frac{L_a}{L_b}\left(i_{L_b}-i_{L_b}(0)\right), \qquad (13)$$

and the state trajectories for each state are obtained by the variable assignment as described earlier.

Substituting (13) and (12) into (11) yields

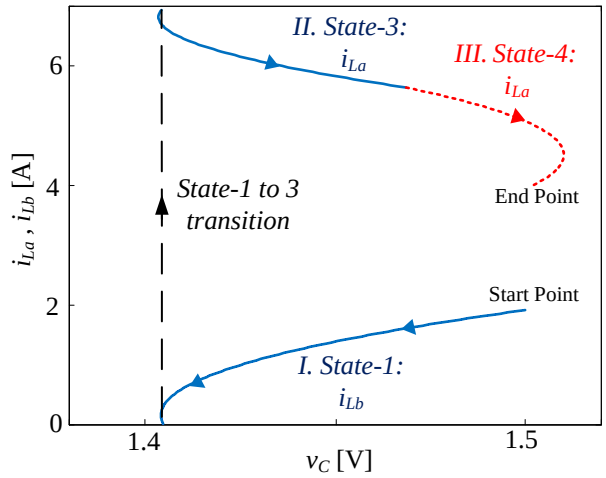

Fig. 12. Optimal trajectories for loading transient: I. On period of phase *a* (state-1). II. On period of phase *b* (state-3). III. Off period of both phases (state 2 or 4). Note the singular transition point – monitoring different currents using the same plot.

$$v_C^{\,2}\frac{C_o}{2}-v_C\frac{L_a}{R_L}+L_a\left(i_{L_a}^{\,2}+\left(i_{L_b}(0)-i_{L_a}(0)\right)i_{L_a}\right)+const=0 \qquad (14)$$

where *const* is defined by the initial values of the inductors' currents and output voltage at the beginning of the state-2 or state-4. Solving (14) yields the trajectories of the converter $v_C=f(i_{La})$ for states 2 and 4.

Following the above derivations, the state trajectories for the SC-buck converter are defined as a conventional buck converter with two expansions. First, the converter includes two on-states (state-1 and state-3) and two identical off states (state-2 and state-4). The second expansion is that there are three initials conditions instead of two. As a result, the procedure to obtain the graphical state-space map as presented in Fig. 11 is as follows:

- Horizontal axis variable for all states is the output capacitor voltage v_C.
- For states 1 and 2, the vertical axis variable is i_{Lb}; for states 3 and 4 i_{La} is used as the vertical axis. i.e., the state-variable is the inductor current that is currently in off state (with direction down toward the horizontal axis) is used as the vertical axis.
- The progress direction of all the trajectories is down along the vertical axis.
- Transition on the map between states 1 to 3 is not continuous, but depends on the actual value of the inductors currents. Because of this so-called singularity, it is possible to view the climb-up of the inductor current from a lower point to a higher one, as depicted in Fig. 12.

The procedure enables to draw a state-space map with two trajectories instead of four, where states 1 and 3 share one trajectory (on) and states 2 and 4 share the other (off), and as a consequence two-dimensional state-plane instead of three-dimensional state-space can be used. This is facilitated by duplication of the vertical axis such that it represents both i_{La} and i_{Lb} as shown in Fig. 11. The blue (solid) trajectories represent an on state; state-1 is monitored by i_{Lb} and state-3 is supervised by i_{La}. The red (dotted) trajectories represent an off state; state-2 is

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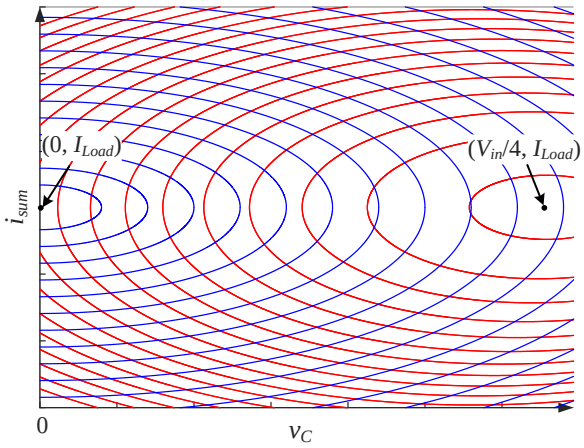

Fig. 13. State-plane of the SC-buck with v_C and i_{sum} as the state-variables.

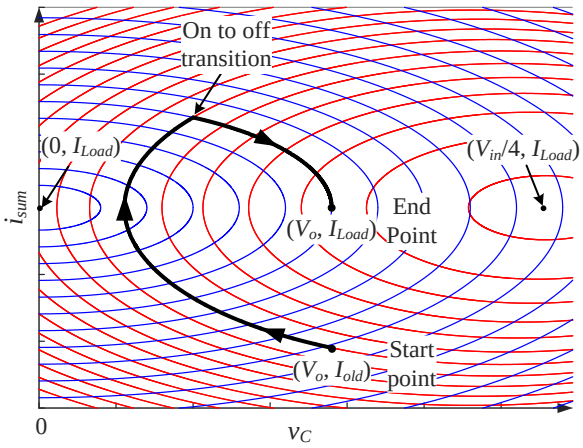

Fig. 14. Time-optimal movement on the state-plane for a loading transient.

monitored by i_{Lb} and state-4 is supervised by i_{La}. For an easier view, a single trajectory is depicted in Fig. 12 for a case of a loading transient (full movement along the trajectory is detailed in the next sub-section).

The state trajectories derived in (9), (10) and (14), and depicted in Fig. 11 are quite complex and it is hard to decipher the dynamic properties of the converter and to define a control law based on them. To overcome this challenge, a new state-variable is defined as the sum of inductors currents $i_{sum} = i_{La} + i_{Lb}$. The output capacitor voltage is maintained as the second state-variable that is used. Using this set of state-variables, the state-equations for state 1 are given by:

$$\frac{di_{sum}}{dt} = \frac{\left(V_{in} - v_{Ct}\right)\frac{L_b}{L_a + L_b} - v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}, \quad (15)$$

for state 3 given by:

$$\frac{di_{sum}}{dt} = \frac{v_{Ct}\frac{L_a}{L_a + L_b} - v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}, \quad (16)$$

and for states 2 and 4 given by:

$$\frac{di_{sum}}{dt} = -\frac{v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}. \quad (17)$$

Under the assumptions of identical on-times for states 1 and 3 and the same inductance used in both phases, i.e. $v_{Ct}=V_{in}/2$ and $L_a=L_b=L$, expressions (15) and (16) of the on states are identical and given by:

$$\frac{di_{sum}}{dt} = \frac{V_{in}/4 - v_C}{L/2}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}, \quad (18)$$

and (17) for the off states can now be re-written as:

$$\frac{di_{sum}}{dt} = -\frac{v_C}{L/2}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}. \quad (19)$$

The resultant set of state equations [(18) for the on states and (19) for the off states] exactly match the state equations of a conventional buck converter with an input voltage of $V_{in}/4$ and inductor of $L/2$. This also implies that the state trajectories of the SC-buck are the same as a conventional buck converter. The state trajectory for the on states is given by:

$$\begin{aligned} &C_o\left(v_C - \frac{V_{in}}{4}\right)^2 + \frac{L}{2}\left(i_{sum} - I_{Load}\right)^2 \\ &= C_o\left(v_C(0) - \frac{V_{in}}{4}\right)^2 + \frac{L}{2}\left(i_{sum}(0) - I_{Load}\right)^2 \end{aligned}, \quad (20)$$

And for the off states the state trajectories are

$$C_o v_C^2 + \frac{L}{2}\left(i_{sum} - I_{Load}\right)^2 = C_o v_C^2(0) + \frac{L}{2}\left(i_{sum}(0) - I_{Load}\right)^2, \quad (21)$$

where I_{Load} is the load current and equals V_o/R_L, $i_{sum}(0)$ is the initial value of the sum of inductor currents, i.e. $i_{La}(0)$ and $i_{Lb}(0)$, and $v_C(0)$ is the initial value of the output capacitor voltage. Plotting these trajectories on the state plane (v_C, i_{sum}) result in two ellipses with centers at ($V_{in}/4$, I_{Load}) for the on states and (0, I_{Load}) for the off states, as depicted in Fig. 13.

By observing the above trajectories and based on previous studies [36], a time-optimal control law can be derived by following the trajectory depicted in Fig. 14 for a loading transient. However, such movement might be deceptive since it is not guaranteed that all the four state-variables of the SC-buck (i_{La}, i_{Lb}, v_{Ct}, v_C) converter reach their new steady-state operating point. One reason is that there is a degree of freedom in i_{sum}, i.e. there is no guarantee the each of the inductors currents are in their new steady-state operating point if their sum reach its steady-state operating point. A simple example is that one inductor carries the load current by itself while the other inductor current is zero. A second reason is that the series-capacitor voltage is not described on this state-plane and therefore its voltage is not controlled. Therefore, a necessary (and not sufficient) condition for time-optimal response is a movement on the state-plane as depicted in Fig. 14. To overcome these issues, two controllers have been developed and are detailed in the following subsections.

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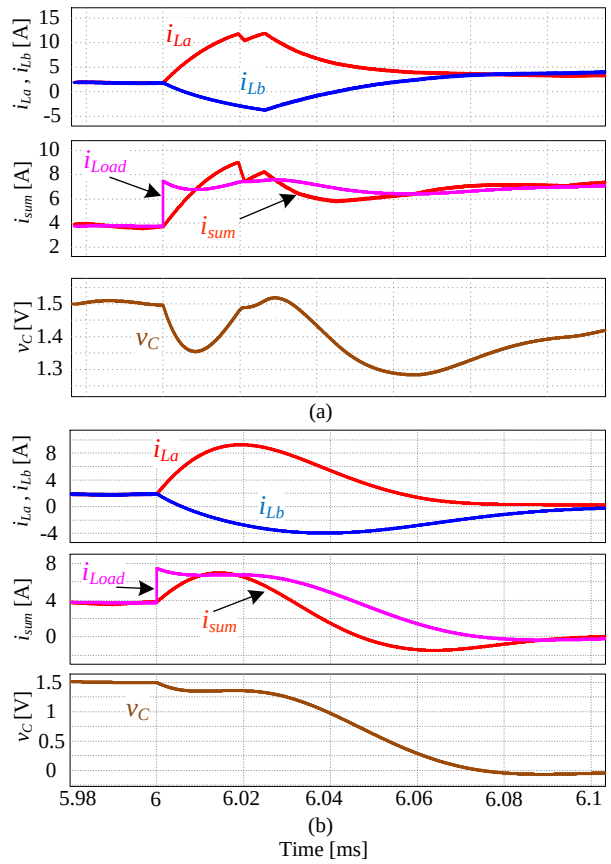

Fig. 15. Attempts of time-optimal recovery from loading transient with uneven distribution of the on phases: (a) large series-capacitor (1 mF) and (b) steady-state sized series-capacitor (50µF).

A. *Minimum-Deviation Transient-Mode Controller*

Observation of the resultant state-space map for the SC-buck converter reveals one of the main differences of this converter topology with respect to a multi-phase buck. As exemplified by Fig. 15(a), during an on state while one of the inductors currents ramps up and may satisfy the required charge balance to the output, the other phase's inductor current ramps down and may result in unstable convergence around the new steady-state point. In addition, since only one phase carries the load, the minimum possible deviation is not obtained. It should be noted that for demonstration purposes, the load transient convergence in Fig. 15(a) has been obtained using an extremely overly-sized series-capacitor (1 mF) to hold the charge during the exceedingly long on time. The situation worsens when C_t is sized to the steady-state requirements (50 µF in the simulated case) as depicted in Fig. 15(b), which results in divergence from the new steady-state operating point.

Based on the behavior of the converter and by observing the trajectories' map, better results are obtained by distribution of the on periods between the phases. As presented in Fig. 12, switching between one on sequence to another, and then applying the off phase, results in a smaller voltage drop, down to the minimum-deviation of v_C.

To facilitate fast transient detection and end-of-transient phase, the first is assisted by two auxiliary comparators with thresholds very close to the reference output voltage ($V_{th,H}$ and $V_{th,L}$, see Fig. 1). The comparators assist in the detection of both loading and unloading transients to initiate the operation of the transient-mode controllers.

A minimum-deviation switching sequence for the SC-buck converter is as follows (described for loading transient):

- At the detection of a load change by comparator *cmp2*, the controller switches to one of the on states (1 or 3).
- A second on period of the alternating phase is initiated when sum of the currents equals to the new load current. This point is detected by the event of the output voltage reaching its minimum point [27].
- Third, an off state (state 2 or 4) can be initiated based on the charge balance of the output capacitor, which can be achieved by transient time calculation. Q_{charge} and $Q_{\text{discharge}}$, which represents the value of the output capacitor charge and discharge, must be equal, as shown in Fig. 17. By assuming that the sum of the inductors current $i_{La}+i_{Lb}$ ramps up with a slope of $(V_{\text{in}}/2-2V_o)/L$, and ramps down with a slope of $-2V_o/L$, the second on state ends when $T_3=T_1D_o^{0.5}$ [31], where D_o is the duty-ratio seen by the output capacitor (due to summing of the two inductors currents), and is given by

$$D_o = 4\frac{V_o}{V_{in}}. \tag{22}$$

This assures the desired equilibrium, and can be implemented using counters.

The method of detecting the point where the sum of inductors current equal the new load current is by detection of the peak\valley of the output voltage. However, it should be noted that the voltage value of the peak\valley is not important. Only the event of reaching a peak\valley is important, and that is the reason for searching the point where the slope of the output voltage is zero. The method for detection of the voltage valley point (or the current cross-over point) in the presented SC-buck converter is the same as in any other time-optimal algorithm for buck converters that requires this kind of detection, and therefore it is not considered as a main contribution in the paper. These methods include sensing of the output voltage (either with ADC or analog sensing), sensing the output capacitor current or estimating the output capacitor current [27], [30]-[32], [43]. It should be noted that direct sensing of the inductor current for this purpose is possible only in single phase converters. In the SC-buck converter the currents of both phases need to be sensed in order to detect the instance when their sum equals the load current. For this reason, we have shown and used one method out of several that have been presented in previous studies. The detection method has been implemented by observing the derivative of the output voltage and detecting its zero-crossing, in a similar approach as detailed in [27].

Fig. 16 and Fig. 17 demonstrate the full sequence procedure for a loading transient, showing the individual inductors currents, sum of the currents, and the output capacitor voltage for both the time-domain and the state-plane. As can be seen, the resulting recovery trajectory of the sum of currents exactly matches a time-optimal behavior for a loading transient of single-phase buck converter. However, as will be discussed in the following subsection, although the response may seem like a time-optimal one, it is only a minimum-deviation response.

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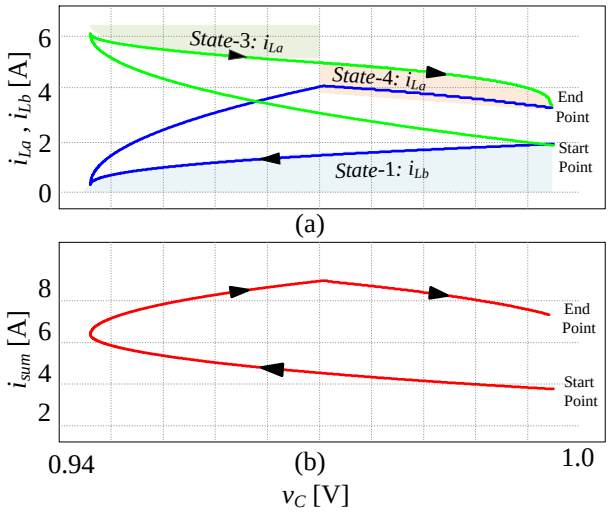

Fig. 16. Simulation results of a loading transient on the state-plane: vertical axis is (a) the inductor currents, (b) the sum of the inductors currents.

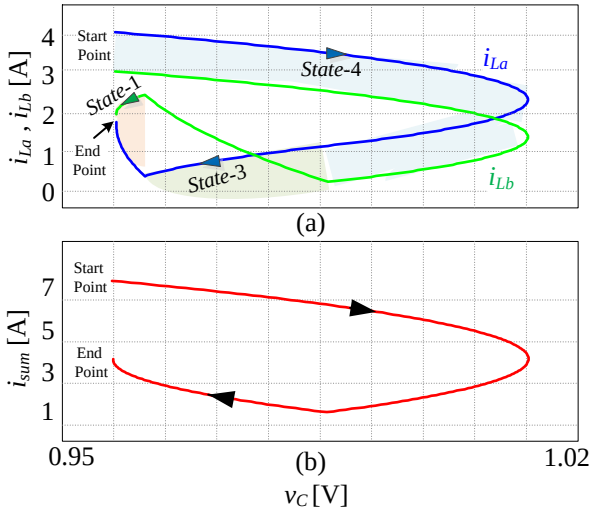

Fig. 18. Simulation results of unloading transient on the state-plane: vertical axis is (a) the inductor currents, (b) the sum of the inductors currents.

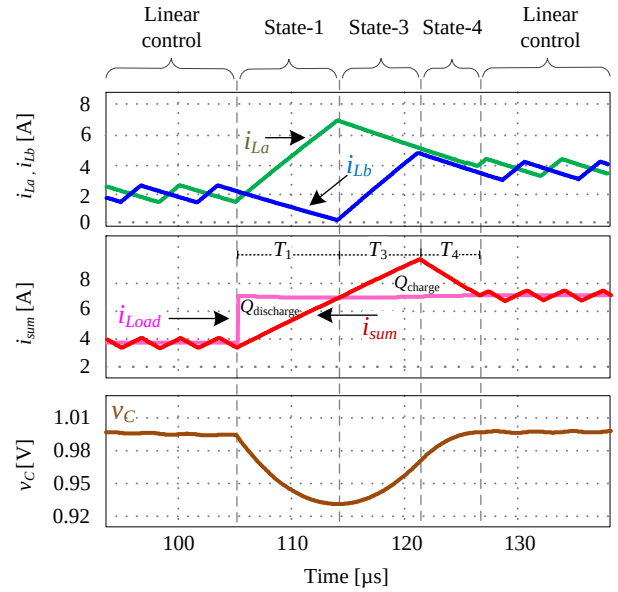

Fig. 17. Minimum-deviation recovery sequence for a loading transient.

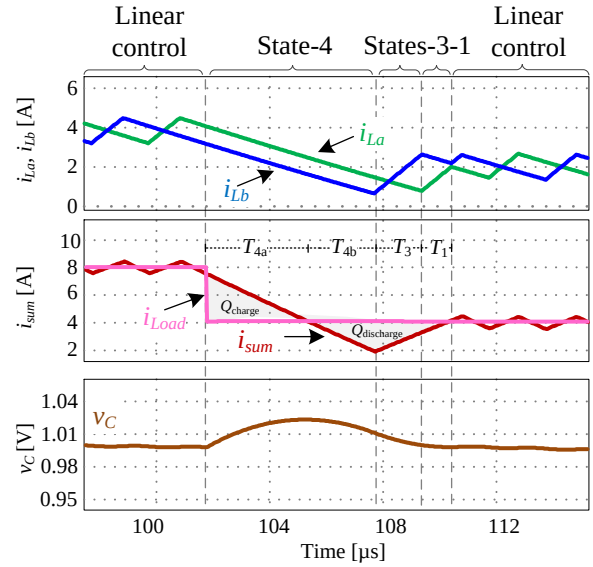

Fig. 19. Minimum-deviation recovery sequence for unloading transient event.

This is since the series-capacitor is being over-charged or discharged during the transient period, which results in oscillations after the end of transient. In fact, to obtain a true time-optimal response, all the four state-variables (v_C, v_{Ct}, i_{La}, i_{Lb}) must reach the new steady-state operation point at the minimum possible time. In the above case, three out of the four state-variables reach the new steady-state point, but the fourth one which is v_{Ct} is now at the correct point at the end of transient. Therefore, although the output voltage deviation is minimal, additional time is needed to move v_{Ct} to the new steady-state operation point and fully recover from the load transient, which implies that this is not a true time-optimal response.

In addition to loading transients, the transient-mode controller is also capable of handling unloading transients. For this case there is more similarity to a conventional buck converter since the off state (2 or 4) is quite similar and differs in the slew-rate of the output current ($-V_o/L$ for buck and $-2V_o/L$ for SC-buck). Fig. 18 and Fig. 19 demonstrate the full sequence procedure for an unloading transient, showing the individual inductors currents, sum of the currents, and the output capacitor voltage for both the time-domain and the state-plane.

For unloading transients, the switching procedure is as follows:

- At the detection of an unloading transient by comparator *cmp1*, the controller switches to one of the off states (2 or 4).
- Second, an on state (distributing between the two phases) is initiated based on the charge balance of the output capacitor, which achieved by transient time calculation. By assuming that the sum of the inductors currents $i_{La}+i_{Lb}$ ramps down with constant slope of $-2V_o/L$, and ramps up with a slope of $(V_{in}/2-2V_o)/L$, the off state ends when $T_{4b}=T_{4a}(1-D_o)^{0.5}$ [31] (see Fig. 19), where D_o is given by (22).

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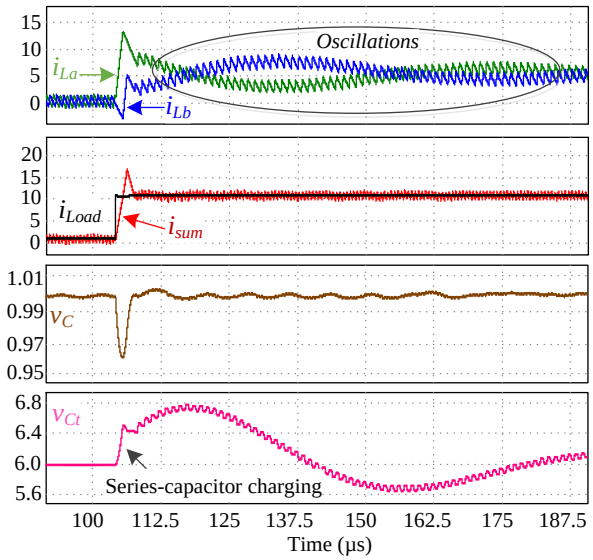

Fig. 20. Oscillations of i_{La} and i_{Lb} after the transient due to charging of the series-capacitor during the transient period when using the minimum-deviation controller.

B. *Synchronized Time-Optimal Controller by Duty-Ratio Saturation*

As can be observed in Fig. 20, the first on time during the transient is significantly prolonged compared to the on time in steady-state operation, which may result in over-charge (or discharge) of the series-capacitor. Since the distribution of the on time between the phases is not equal, i.e. $T_1 \neq T_3$, the series-capacitor voltage v_{Ct} can no longer be assumed as a constant that equals $V_{in}/2$. As a result, the inductors currents at the end of transient are not equal. At this point, although the output voltage is not affected by it, oscillations of the currents occur since $V_{Ct} \neq V_{in}/2$ and $T_a = T_b$. The reason for these oscillations is the fact that the design of the controller assumes that v_{Ct} is constant and the input voltages of the two phases are equal. To overcome this issue, an improved transient-mode controller that produces a time-optimal response, i.e. moving all the four state-variables to the new steady-state operation point in the minimum possible time, has been developed. One possibility to solve this issue is to increase the series-capacitor's size to reduce the magnitude of the oscillations; however, as seen in the previous section, this requires an overly sized capacitor, which is prohibitive in volume-sensitive applications. An alternative solution that has been adopted here is to distribute the task of the on state between the two phases. This is shown in Fig. 22 and facilitated by assignment of even on times between the two phases while limiting the switching frequency. An equivalent approach to the minimum-deviation method presented earlier is achieved by saturation of the duty-ratio to its maximum value for the SC-buck converter, i.e. to D=0.5, for ramping up the inductors currents. Using this approach, v_{Ct} remains virtually constant and equals $V_{in}/2$ throughout the duration of the load transient, and as a result the inductors currents are equal at the end of transient (within the current ripple) and oscillations of them after the transient are prevented. In fact, to completely avoid any change in v_{Ct}, the switching frequency during the transient must be infinite. Since voltage ripple of the series-capacitor is allowed and exists also in steady-state operation, there is no need to reduce it to zero for the transient period. In a properly designed

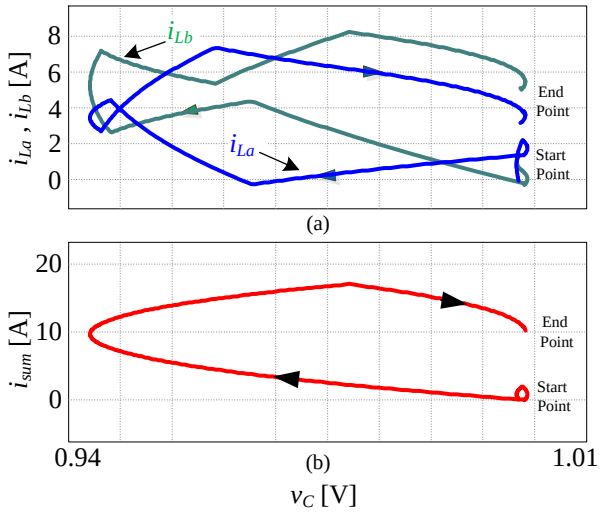

Fig. 21. Simulated loading transient response of the synchronized time-optimal controller using duty-ratio saturation on the state-plane. Vertical axis is (a) the inductors currents, (b) the sum of the inductors currents.

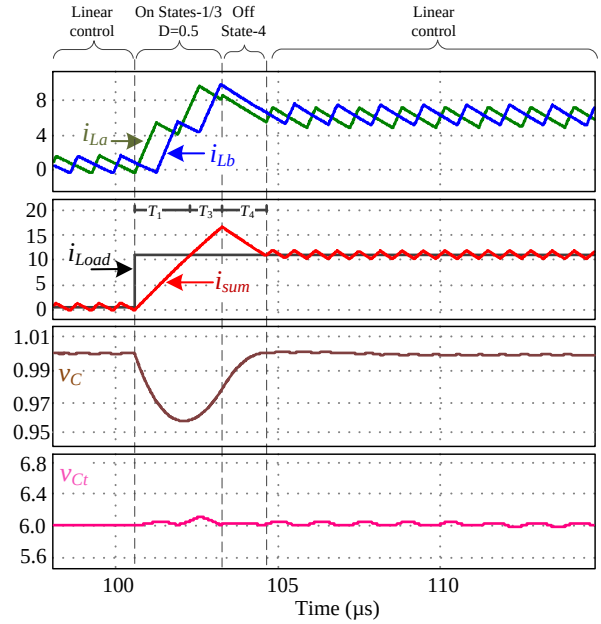

Fig. 22. Simulated time-domain response of a loading transient of the synchronized time-optimal controller using duty-ratio saturation.

converter, typical voltage ripple of the series-capacitor is 5-10% of the nominal voltage under every load conditions, and using the synchronized time-optimal controller the maximum voltage ripple can be estimated since the duty-ratio (and on-time) of the phases is known. Therefore, the switching frequency for the transient period remains the steady-state switching frequency, and although a small error of the series-capacitor voltage may appear at the end of transient, it is small and within the voltage ripple magnitude and can be handled by the steady-state controller without causing an addition transient. Although more switching actions are used during the transient and as a consequence the switching losses may increase, they are negligibly small as the switching frequency remains the same as in steady-state operation. It should be noted that switch commutation times may impact the transient time due to an effective duty ratio that is lower than 0.5, but since they are small compared to the on times of a switches and their effect is very small. In addition, switch commutation times do not impact the

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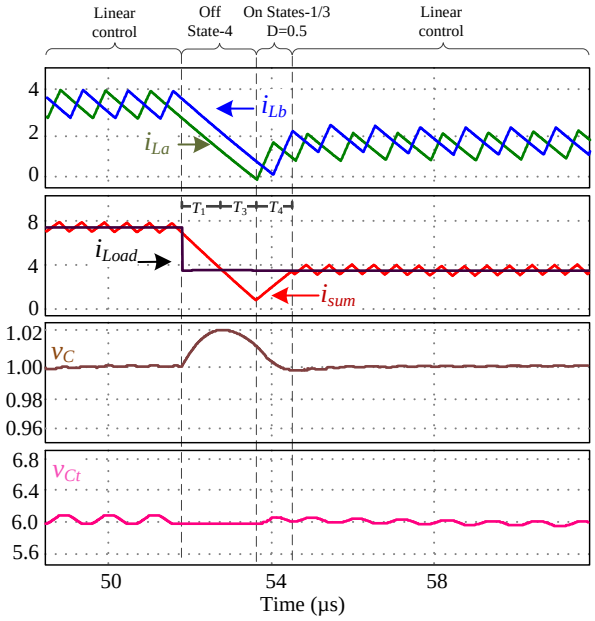

Fig. 23. Simulated time-domain response of an unloading transient of the synchronized time-optimal controller using duty-ratio saturation.

series-capacitor voltage since there is current flowing through the series-capacitor only during the two on states.

Fig. 22 and Fig. 21 demonstrate the full switching sequence of the duty-ratio saturation approach for a loading transient in both time-domain and in the state-planes. At the detection of a loading event, the controller saturate the duty-ratio to D=0.5 and the on time is equally shared between the phases. Next, an off state (state 2 or 4) is initiated based on the charge balance of the output capacitor as described for the minimum-deviation controller in the previous subsection. It can be seen in Fig. 22 that, although the switching frequency is finite and there are small errors in the inductors currents, the difference between the inductors currents remains within the current ripple during as well as after the transition period, the voltage of the series-capacitor is virtually constant and the oscillations are avoided. It should be noted that in order to avoid any mismatches in the inductors currents and series-capacitor voltage at the end of transient, the switching frequency during the transient period should be infinite. The infinite switching frequency is required in order to overcome any situation where one of the phases has more on states than the other and charge balance of C_t is not fully maintained. However, in a properly designed converter where C_t is designed to have small ripple, excellent charge balance can be obtained when operating at the steady-state switching frequency for the transient period. Another significant advantage of this approach is the fast that the DPWM is not bypassed for the transient period and synchronization in the system is maintained. This feature enables a smoother transition between the steady-state and transient-mode controllers.

To verify that time-optimal response is facilitated, the movement of the state-variables along the trajectories is examined for both approaches by observation of the output voltage and the sum of the inductors currents. Consequently, the resultant state-plane maps (see Figs. 15, 17 and 20) resembles one of a conventional buck converter. It can be observed from Figs. 15 through 21 that, the resultant optimal trajectory is the one where the minimum output voltage deviation is obtained, i.e. as in conventional time-optimal control [43].

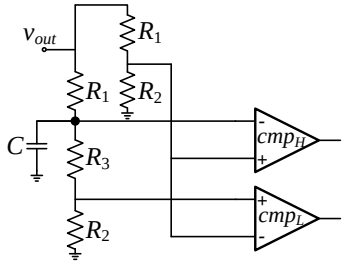

Fig. 24. Comparators references voltages generating circuit.

TABLE I. EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	*Value*
Inductors L_a, L_b	0.5 µH
Series-capacitor C_t	10 µF
Output capacitor C_o	200 µF
Output capacitor ESR R_c	1.5 mΩ
Switching frequency f_s	800 KHz
Comparator Voltage Reference $V_{ref,H}$	V_o + 20mV
Comparator Voltage Reference $V_{ref,L}$	V_o - 20mV

The unloading response when using the time-optimal controller is very similar to an unloading transient using the minimum-deviation controller, as shown in Fig. 23. The difference between the two is only in the distribution of the on times between the two phases. While the time-optimal controller distributes the on-time evenly between the phases by setting the duty-ratio to 0.5 in states 1 and 3, the minimum-deviation controller don't necessarily do so. Since the on-time in high conversion ratio is very short and the switching frequency in finite, there is a negligibly small difference between the responses of the controllers. The reason is that for this case the on-time just before the end of transient is very short since D_o is small. For this reason, the response shown in Fig. 23 is very similar to the one shown in Fig. 18. The state-space response is not presented here due to very high similarity to the one shown in Fig. 18. Nevertheless, in the following experimental section all the transient responses are shown.

IV. EXPERIMENTAL RESULTS

To validate the operation of the voltage-mode controller that is based on the average-behavioral small-signal model and the transient-mode controller, a 12-to-1V SC-buck converter prototype that operates at 800 KHz has been built and tested. The main components of the prototype are listed in Table I. The digital controller comprises the steady-state voltage-mode compensator and the transient-mode controller as shown in Fig. 1. The controller has been entirely realized on Altera Cyclone IV FPGA [44], including custom design of all related peripherals with an all-digital delay-line window-ADC and DPWM as described in [45], [46] and the total number of logic elements that were used is 1214 for the entire controller. Load transient signals were also generated by the FPGA, independently, without synchronization to the controller.

In this study Delay-line based window-ADC has been used for sampling the output voltage during steady-state operation. This architecture of ADC provides accurate measurement with modest hardware, and its full details and principle of operation are given in [46]. In the presented experimental setup, a 6-bit

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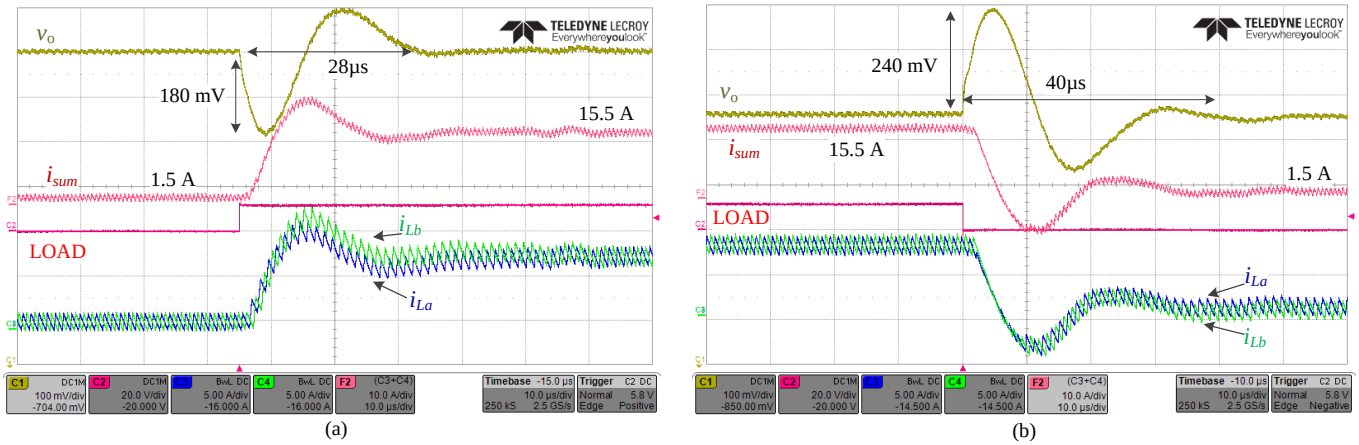
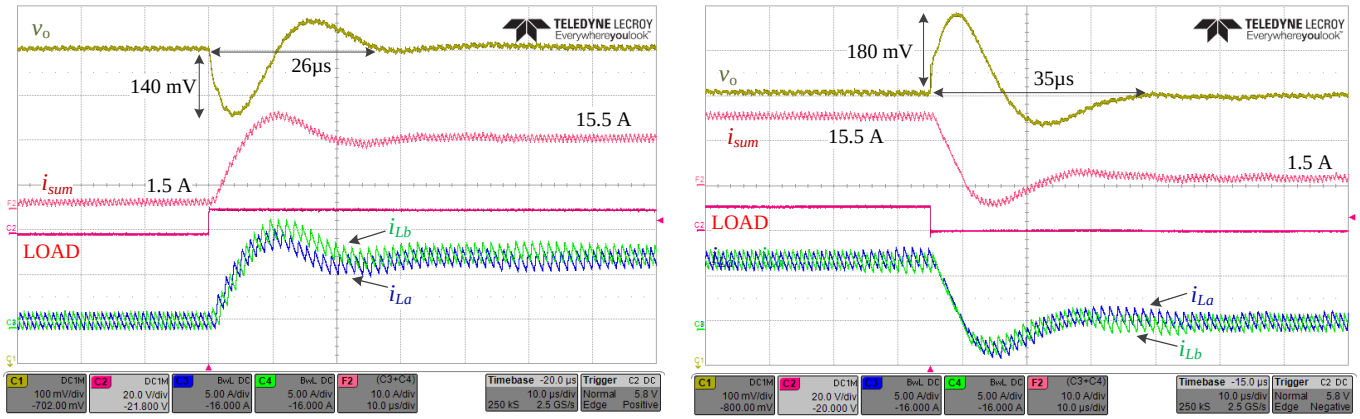


(a) (b)

Fig. 25. Voltage-mode controller response for sampling at f_s to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C2 – Load step signal, C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.



(a) (b)

Fig. 26. Voltage-mode controller response for sampling at $2f_s$ to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C2 – Load step signal, C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.

window-ADC is used. The ADC's sampling rate is set to be twice the switching frequency, i.e. $f_{sampling}$=1.6 MHz, with resolution of 5mV/bit.

The comparator's thresholds have been designed to be close enough to the nominal voltage for accurate transient detection and operation but also far enough from it to avoid false triggering of the transient-mode controller, as detailed in [27], [47], [48]. Therefore, for the presented experimental setup the thresholds were designed to be 1V±20mV. The comparators' voltages thresholds generating circuit is described in Fig. 24.

Fig. 25 and Fig. 26 show the operation of the digital voltage-mode controlled SC-buck converter with the transient-mode controller disabled, handling loading and unloading transients to compare the difference between a sampling frequency of f_s and $2f_s$, respectively. For a 14A loading transient, sampling at f_s - the output voltage undershoot and settling time are 180mV and 28µs, respectively. Sampling at $2f_s$ - the output voltage undershoot is reduced to 140mV and the settling time to 26µs. For an unloading transient of 14A the output voltage overshoot is 240mV and the settling time is 40µs with sampling at f_s, compared to 180mV overshoot and 35µs settling time with sampling at $2f_s$. It can be observed that there is a significant delay when sampling at f_s at the beginning of the transients due to the delay of $T_s/2$, as predicted by the evaluation in Section II.

Fig. 27 depicts the minimum-deviation transient-mode controller response to 14A loading and unloading transients. As can be seen, with this control law the output voltage deviations and settling times are significantly reduced compared to the voltage-mode controller. For a 14A loading transient, the output voltage undershoot is 80mV and transient time is 6µs, and for a 14A unloading transient the output voltage overshoot is 120mV and the transient time is only 8µs. However, as predicted by the analysis and simulations in Section III, it can be observed that oscillations of the inductors current occur due to over-charge of the series-capacitor, which implies that this is not a time-optimal response as one of the four state-variables is not at the correct operating point at the end of transient and result in increased settling times of 43µs for loading and 26µs for unloading.

Fig. 28 shows time-domain and state-plane representation for 14A load transient response of the synchronized time-optimal transient-mode controller. As can be seen, the output voltage deviations are the same as in the case of the minimum-deviation controller in Fig. 27, but the settling times are significantly reduced since the oscillations of the inductors currents are avoided. This is since v_{Ct} remains approximately constant (within ripple margins) for the transient period, despite of the fact that the two phases has unevenly distributed on-times, i.e. phase *a* has 4 on-times and phase *b* has only 3 on-times during the transient (See Fig. 28(a)). In addition, the state-plane

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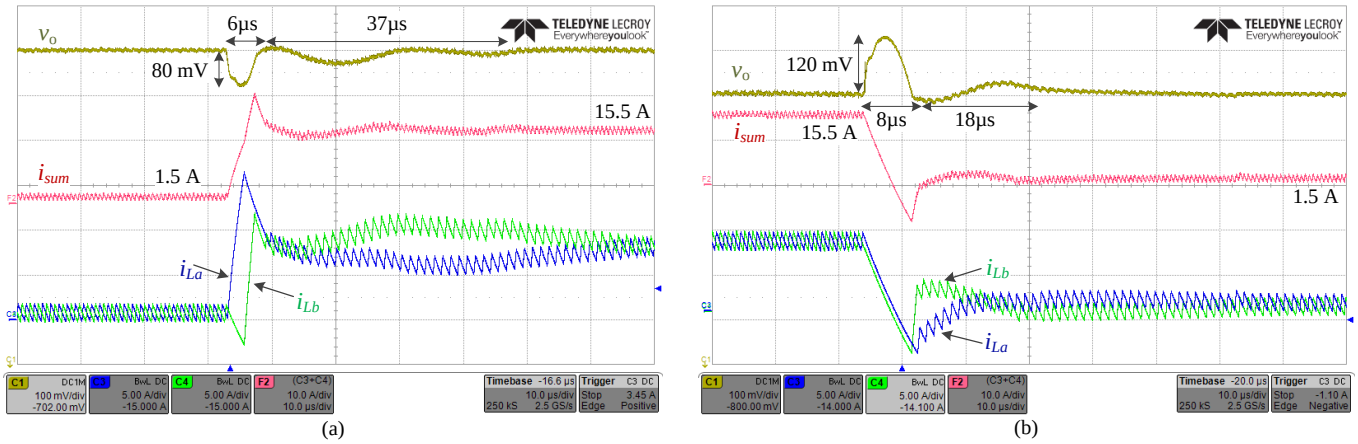

Fig. 27. Minimum-deviation controller response to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.

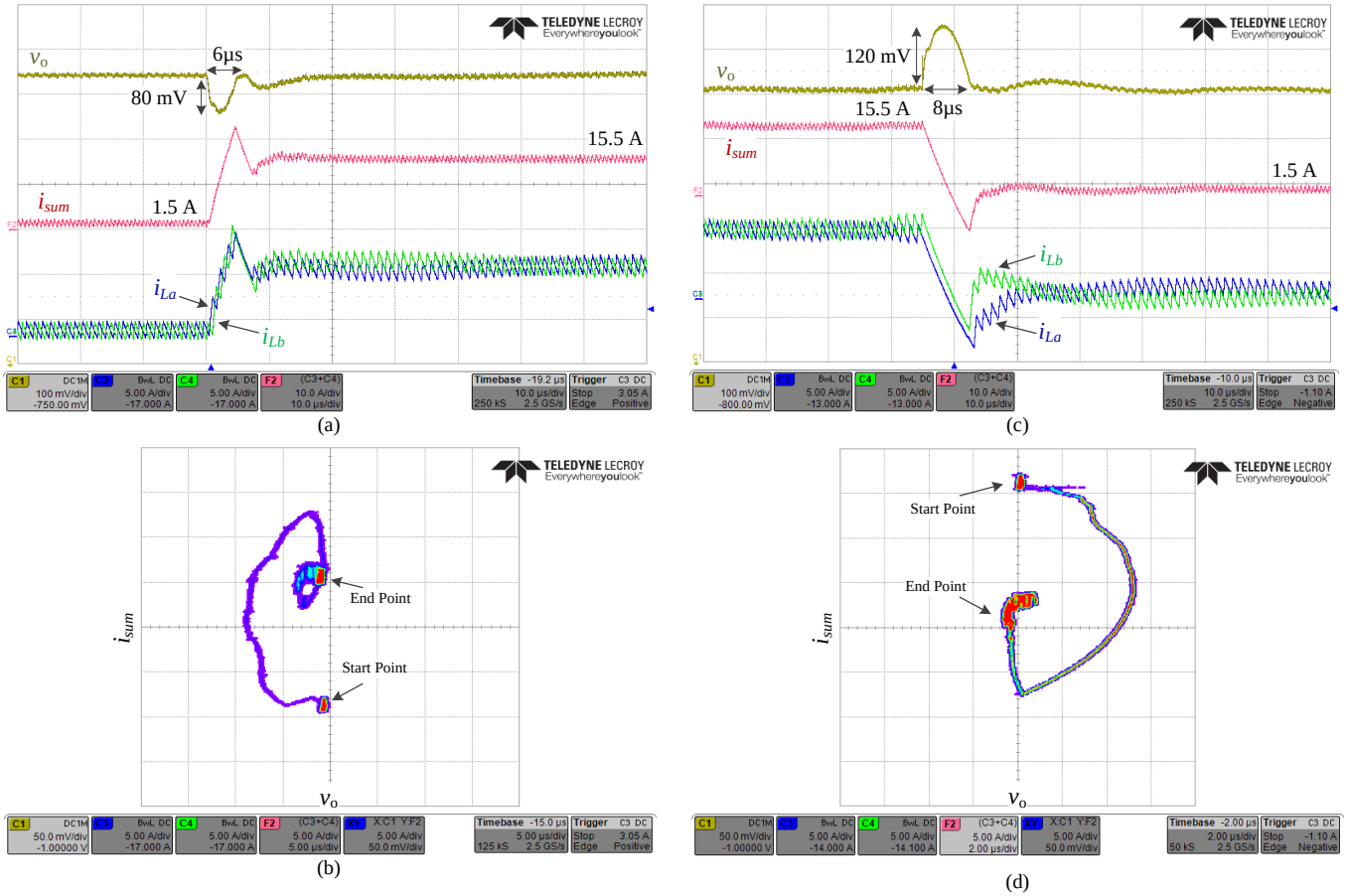

Fig. 28. Time-domain and state-plane representation response of the synchronized time-optimal controller to a 1.5A → 15.5A loading transient [(a), (b)] and 15.5A →1.5A unloading transient [(c), (d)]. For (a) and (c): C1 – v_o output voltage (100mV/div), C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div. for (b) and (d): horizontal axis is v_o (50mV/div), vertical axis is sum of inductors currents i_{sum} (5A/div).

representation validates the analysis of the time-optimal trajectories from Section III. It should be noted that there is noticeable regulation process after the end of transient, in a similar manner as allowed by VRM applications [49]. However, this regulation is required due to small errors in the inductors currents at the end of transient that happen due to finite switching frequency. Since these errors are small, the steady-state controller can handle them without any significant output voltage overshoot or undershoot.

V. Conclusion

In this study, an optimal closed-loop control scheme for a series-capacitor buck converter has been presented. The controller, which has been realized on a digital platform, merges a voltage-mode controller for steady-state operation and a transient-mode time-optimal controller for load transients. In the theoretical analysis, an average-behavioral model as well as state-space representation of the converter have been derived, then two transient-mode controllers have been developed. The

analysis revealed that a key factor for recovery of the converter from load transients is the capability of the controller to satisfy the charge-balance of the series-capacitor at all times (including during load transients). The transient-mode controllers that have been developed distribute the on-time period between the phases and by doing so, an expedited yet smooth, transient recovery is achieved. The experimental validation of the controller operations has been found to be in very good agreement with the theoretical predictions. Also shown are the differences between small-signal voltage-mode and time-optimal control alternatives, demonstrating the superiority of the state-variables based approach.

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