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Low Voltage Sub-Nanosecond Pulsed Current Driver IC for High-Speed LIDAR Applications

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***Abstract* — This paper introduces a new low voltage sub-nanosecond monolithic pulsed current driver for light detection and ranging (LIDAR) applications. A unique architecture based on a controlled current source and Vernier activation sequence, combined with a monolithic implementation, allow operation from low input voltage levels, high-resolution pico-seconds range pulse width, and rapid rise and fall times. An on-chip low voltage pulsed driver sub-nanosecond prototype has been implemented in a TS 0.18-μm 5-V-gated power management process. It incorporates an integrated wide range senseFET based current sensor and a rail-to-rail comparator for current regulation. A separate line of investigation has been carried out to characterize the avalanche capabilities of the integrated lateral MOSFET power devices required for the driver IC. Several lateral diffused MOS (LDMOS) power devices have been custom designed and experimentally evaluated for a life-cycle performance characterization. In addition, a delay-line (DL) based controller to govern the pulsed current driver IC is described and implemented on an FPGA. To validate the concepts of the high-resolution LIDAR current driver, both discrete and IC experimental setups have been constructed and evaluated, validating the method for currents up to 20 A peak in discrete and 5A in integrated solution. Post-layout analysis and the experimental evaluation of the driver IC have been found to be in very good agreement. The experimental results demonstrate overall improvement on several operation properties, such as rise time, fall time, and pulse width resolution, of over one-order of magnitude compared to the state-of-the-art silicon-based LIDAR drivers. For 5-V input, and a representative output pulse of 5-A, the results that have been obtained are: 900 ps rise time and fall time of 2.5 ns, all measured at the driver's light output. In addition, the pulse width resolution has been enhanced to hundreds of ps, which is significantly below the intrinsic delay of the power switches.**

***Index Terms* — controlled current source IC, current pulse, driver IC, LIDAR, laser diode, power MOSFET, pulse circuits on-chip.**

I. Introduction

Latest boost in development of autonomous vehicles, aerial drones and industrial robots creates a huge demand for a short-range environment-sensing interface [2]-[6]. LIDAR system (Fig. 1a), i.e. *Light Detection and Ranging*, employs an infrared laser for distance measurement, and it is one of the promising methods to be cost-effective, precise and reliable for portable applications [2]-[7]. Range accuracy and resolution of a LIDAR depend on the rise-time, fall time and pulse-width of emitted light pulse, which in turn is a direct function of the current supplied to the laser diode by the driver [2], [5]-[7]. Implementation of a driver with sub-nanosecond rise-time and pulse width poses an extreme challenge due to intrinsic parasitic capacitances and inductances of the components [2], [6]. An ideal setup to drive a laser diode is a current source that generates short pulses with controllable pulse amplitude, width, and rise and fall times (Fig. 1b). In practice however, device parasitics limit the parameters above to a certain boundary, and perhaps more challenging is the relatively slow dynamic performance of high-impedance sources. As a result, the practical implementations of driving low-impedance loads are forced to compromise on some of the parameters.

Some of the earlier methods to drive a laser diode are using a BJT avalanche phenomenon [8]-[10]. While this method potentially results in fast rise times and short pulse width, it requires a number of transistor stages to improve the rise time in every subsequent transistors stage [10]. It also requires extremely high voltages, on the order of hundreds and even a thousand volts to generate an avalanche [8], [10]. Pulse shaping is complex and the efficiency of these methods is rather low, resulting in bulky and excessive heat generating installations, with low pulse repetition frequency (PRF) located within kilohertz scale. An alternative, simpler approach to drive a laser diode is to charge a capacitor to a predefined voltage, and then activate a switch that discharges the capacitor to the laser diode to generate a light pulse [9], [11]. This approach still requires a relatively high voltage, since the current is developed according

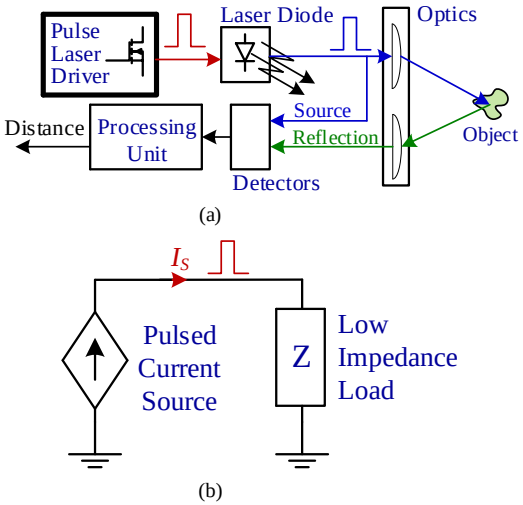

Fig. 1. LIDAR (a) Conceptual block diagram of the system; (b) Ideal pulsed laser diode driver.

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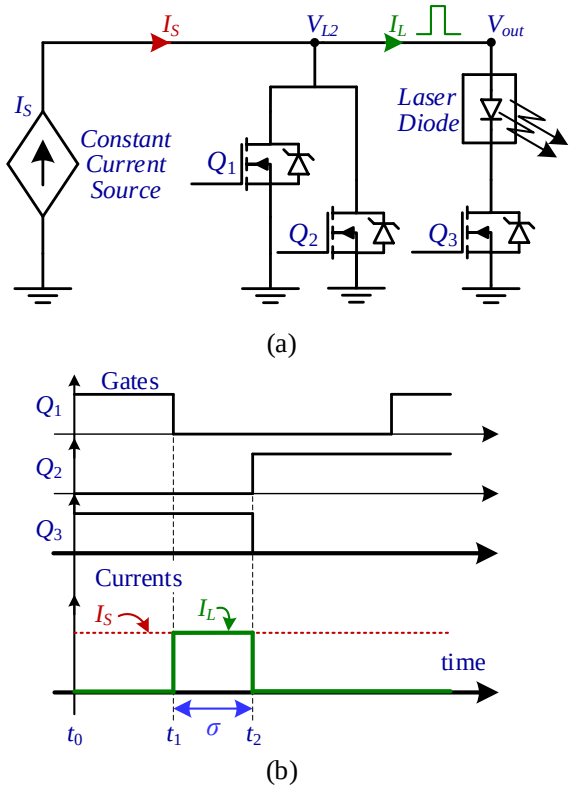

Fig. 2. Driver architecture: (a) Schematics; (b) Switching sequence.

to the impedance of the laser diode. The most significant drawback of this method is that switching devices with extremely short transition and delay times are required [9]. Both methods require a special technology for integrated circuit implementation such as an expensive avalanche BJT or a GaN device with proper drive. Another method is to use a high voltage source and an inductor to create a high impedance path, which then forces the current through the laser diode [12].

The alternative concept that has been pursued in this study is to build up a constant current that flows through an inductor and channel the current flow to and from the load using switch assembly. In this approach, the high-impedance characteristics of the inductor are utilized as well as the possibility of rapid transitions.

The objective of this study is to present a high and rapid current-sourcing power driver for LIDAR applications, as shown in Fig. 1. The power driver features controlled current source and programmable sub-nanosecond resolution for the pulse width with rapid transitions (rise and fall times). It is a further aim of this paper to detail the development process and present a fully monolithic IC implementation of the laser driver. The study also extends to include a wide dynamic range current sensor, delay-line (DL) based pulse shaping controller, a current sourcing stage, as well as development and evaluation of lateral power devices with the ability to sustain high-energy bursts under breakdown conditions.

The rest of the paper is organized as follows: Section II describes the architecture and principle of operation of the new low voltage sub-nanosecond monolithic pulsed current driver. Section III details practical implementation. A high-resolution DL-based controller architecture is described in Section IV. The IC implementation, monolithic design considerations including evaluation and characterization of several LDMOS power devices, as well as post-layout results are delineated in Section V. Experimental results of the pulsed current driver are reported in Section VI. Section VII concludes the paper.

II. Driver Architecture and Principle of Operation

An idealized current driving concept is depicted in Fig. 1b, it shows a controlled pulsed current source that drives a low-impedance load. Unfortunately, ideal current sourcing is not a feasible practice, in particular current source behavior is generated through a device or circuit that mimics high-output impedance within its bandwidth limitations. As a result, rapid transitions that exceed the system bandwidth cannot be obtained using this concept. An alternative approach that inspired by controlled pulsed current source and rapid gate drives configurations has been adopted in this study and is depicted in Fig. 2a. It utilizes a regulated constant current source, I_S, followed by a network of power switches, Q_1-Q_3 that act as a current routing network. The operation of the driver is described with the assistance of Fig. 2b that illustrates an idealized gating sequence and load current. The operation is divided into an idle state and two phases: turning on and turning off transitions. In the idle state t_0 (Fig. 2b), the switch Q_1 is on, providing a closed path for the current flow of the source, while the switches Q_2 and Q_3 are turned off. At this point, the system is ready for outputting a current pulse. In the turn on phase, at time t_1, Q_3 is already on and Q_1 turns off, the current from the source is routed towards the load, laser diode in this case. The turn off phase t_2 is commenced by simultaneously turning Q_2 on and Q_3 off, causing the inductor current to rapidly route back off the load through Q_2. The use of the additional parallel transistor Q_2, as opposed to operation with Q_1 alone, allows flexible setting of the pulse duration with precise and high time resolution, which cannot be obtained using a single device due to the relatively long intrinsic delays and response time that are involved with high current devices [13]-[15]. The series transistor Q_3, when turned off, increases the impedance of the load path so that the current flow is rapidly halted. As will be detailed in the next section, it also assists to overcome the effect of parasitic inductances that in the practical case, introduces significant turn off delays.

It should be noted that the gating sequence can be repeated periodically, on demand. For energy saving purposes, between sequence cycles, and depending on the PRF and desired duty cycle of the load, the constant current source may be switched to lower amplitude, or completely turned off.

III. Practical Implementation

A primary objective of this study is to develop a low-voltage pulse generator to drive LIDAR applications. The power driver required to be able to provide high-resolution pulse width adjustment, ultra-fast rise and fall times, controllable current amplitude, and be compatible for IC implementation. There are several challenges associated with the objectives above.

A. Time Delays of Practical Components

The current routing switches are power MOSFETs with unavoidable intrinsic delay between turn on command and the conduction of the MOSFET channel, $t_{d(on)}$. In particular, for power devices that are designed to handle significant current

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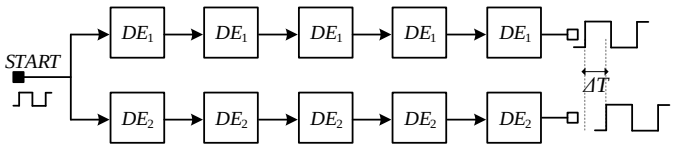

Fig. 3. Driver architecture: (a) Schematics; (b) Switching sequence.

ratings, these delays are on the order of several nanoseconds to some tens of nanoseconds. To achieve time resolution of some 100's picoseconds for the pulse width setting, a Vernier method [16]-[18] has been employed. In this technique, a digital 'START' control signal is fed into two (or more) delay chains with different delay characteristics (Fig. 3), such that a high-resolution time delay is being generated. The resulting time delay, ΔT, equals to the time difference between the delay elements (DE) within the delay chains (i.e., by the delay between their rising edges). In principle, any resolution can be achieved by this method, however, it should be emphasized that in practice, the time resolution is limited by mismatches of the transistors, length of the DL, and any potential noise. To overcome these limitations there are several modified approaches utilizing Vernier method [16]. Two MOSFETs, Q_1 and Q_2 (Fig. 2a), are placed in parallel to each other. One transistor Q_1 is designed and rated for high current whereas the second transistor Q_2 is designed for speed (can be of smaller size for die optimization). Prior to the turn on phase, MOSFET Q_2 is turned off, while MOSFET Q_1 is left on. At the point t_1 (Fig. 2b) two gate commands that are offset from one another by the width of the pulse σ are generated, turning Q_1 off, and with delay of σ at time t_2, turning Q_2 on. As a result, this Vernier time-skewed command of Q_1 and Q_2, reroutes the current from the source to the load for σ seconds, facilitating a pulse width that is significantly faster than the intrinsic delay of the device's $t_{d(on)}$.

B. Parasitic Capacitances

Switch Q_1 is the main path for high constant current generated by the current source. To attain high efficiency, the on state resistance of the switch, $R_{ds,on}$ needs to be as small as possible. Large MOSFET with low $R_{ds,on}$ is preferable, however, this comes at the cost of higher output capacitance of the device C_{OSS} (C_{ds} + C_{gd}). This capacitance imposes finite slew-rate of the voltage build up across the load, which in turn limits the rise time of the current due to parasitic inductances in series with the load. To achieve high voltage slew-rates, high currents are required from the source. In addition to limiting the slew-rate, the parasitic capacitance C_{OSS}, resonates with parasitic inductance of the load path, setting up the limit for rise time.

To address the challenges described in this section, integrated circuit design is considered in this work. Adjustable design of the power device, and miniaturization of the whole circuit, i.e. on-chip implementation, allows achieving several goals. Reduction of the parasitic components in the current path, i.e. lower C_{OSS} and lower parasitic inductances due to the on-chip interconnections. Achieving a better balance between on resistance and switch output capacitance according to the application, and integration of the gate driver with the power switches (Q_1-Q_3) to facilitate higher driving speeds.

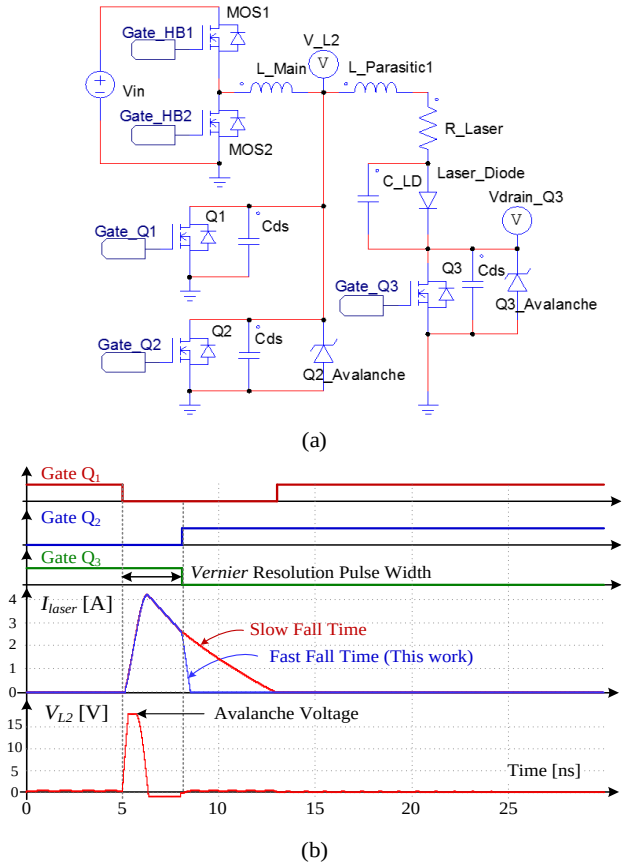

Fig. 4. Simulation (a) Schematics; (b) Waveforms.

C. Parasitic Inductances

Fall time of the current pulse through the laser diode depends on the parasitic inductances (including the stray inductance of the laser diode) and the voltage that is applied to the laser diode during its turn off. In conventional current driving method such as [12], a freewheeling diode is added in parallel to the load to avoid high voltage damage as a result of the residual energy in the parasitic inductance. However, since the forward voltage of laser diodes is relatively low, if freewheeling is allowed, the turn off time extends and cannot be regulated. It should also be noted that during the turn off period, the current 'tail' circulates energy through the load path heating up the laser diode, an extremely undesirable scenario for LIDAR applications. To overcome this challenge an additional switch Q_3 in the load path is employed (Fig. 4). Switch Q_3 turns off together with the turn on of Q_2 so that any residual current in load path charges the output capacitance of Q_3, which in turn boosts the voltage at the drain of Q_3. Increased voltage at the drain of Q_3 reverse biases the diode, preventing further conduction, resulting in rapid turn off time of the load.

High voltages at the drain of Q_3 could potentially damage the laser diode. To protect the laser diode from very high reverse voltages, switch Q_3 is selected/designed with reasonable avalanche voltage level, so that at very high currents, the voltage is clamped to some maximum value by the MOSFET, as symbolically represented in the simulation schematics of Fig. 4a with a device named Q_3*_Avalanche*.

Additional effect of parasitic inductances in the presence of current source are instantaneous voltage spikes at the switching

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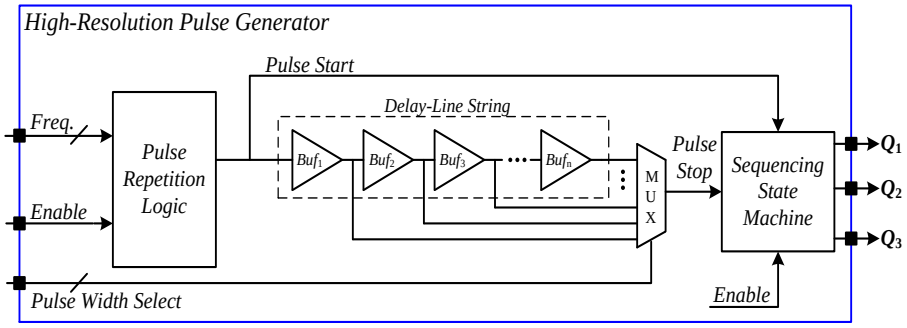

Fig. 5. Simplified block diagram of a DL-based high-resolution pulse generator.

nodes. In this circuit, the node prone to this problem is V_{L2} (Fig. 4a), where $L_{Parasitic1}$ avoids an immediate current redirection to the laser diode. The voltage at the node rises as a function of current amplitude and the total node capacitance, and can reach very high values compromising the power switches Q_1 and Q_2. One way to overcome this challenge is to add an auxiliary Zener diode. This solution however, adds an extra parasitic capacitance and in terms of monolithic implementation, requires large silicon area. The solution developed in this study is based on avalanche rated integrated MOSFETs [8], [10], [19], and discussed in detail in Section V, and represented with the device Q_2*_Avalanche* in Fig. 4a.

A cycle-by-cycle simulation test-bench has been constructed in PSIM (PowerSim, Inc.) (Fig. 4a) to evaluate the solutions for the discussed challenges. The Vernier method is employed in the simulation, to generate high-resolution pulse width of the laser current I_{laser} as shown in Fig. 4b. In addition, the voltage at node V_{L2} is clamped to the avalanche breakdown voltage, which is predefined in the simulation to 18 V, and simulated by a Q_2*_Avalanche* device. An example of a fall time improvement over the conventional case without the additional switch Q_3, is given in the middle plot of Fig. 4b. The fall time of the system shown in this study, (blue trace) is much shorter than the conventional freewheeling approach, (red trace). It should be noted that the trapezoidal shape of the pulse is within the application-imposed limits.

IV. High-Resolution LIDAR Driver Controller

Control challenges associated with the design of LIDAR driver IC based on the presented architecture include design and implementation of a controlled current source, and a precise high-resolution, low power, pulse generation logic sequencer.

One option to realize controlled current source, is by a half-bridge that feeds an inductance to create high output impedance (as shown in Fig. 4a). The series inductance satisfies the high impedance characteristics of the sourcing element. To assure virtually constant current delivery the inductance value is set sufficiently high so that the energy delivered to the laser diode, E_{dlivered}, is negligibly small comparing to the overall inductor energy ($LI^2/2$), i.e. ($LI^2/2$)>E_{dlivered}. The switching frequency of the half-bridge is selected to be sufficiently slower than the width of the load pulse, so that the current source is virtually constant to the pulse generation switches. The current control is implemented by hysteretic-type reference-based control scheme, similarly to [20]-[23]. The inductor current is compared to a reference level using comparator, triggering the operation of the half-bridge power-stage each time a reference

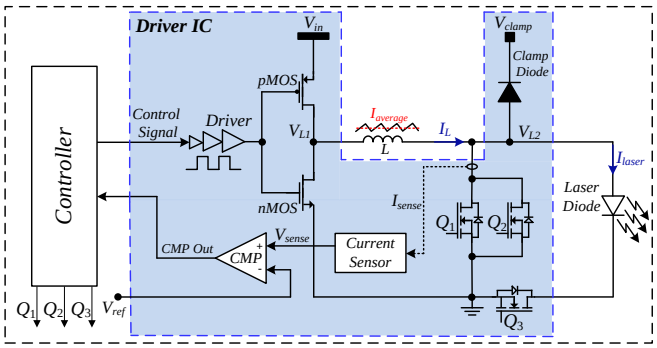

Fig. 6. Block diagram of the implemented IC.

level is crossed. Current thresholds are set to maintain the current ripple low, and close to the target current.

Start command arrives from the pulse repetition unit, which is passed to switch Q_1 to turn it off, in addition, the pulse start signal propagates throughout the buffers string (Buf_1 to Buf_n in Fig. 5). The delay of each element is associated with its transition response time, $t_{d(Buf)}$, predefined by the controller implementation process and technology [24], [25]. Rising edge signal advances along the DL string, accumulating the delays of each of the subsequent buffers response time. Pulse width selection multiplexer decides which of the buffers connects to the output signal, pulse stop, which eventually triggers switches Q_2 to turn on and Q_3 to turn off (Fig. 2b). This implies that longer pulse start signal propagates throughout the DL yields longer delay that accumulates between the pulse start and pulse stop edges, determining the laser current duration. The pulse start and stop signals are passed to the state machine, that generates the gate drive commands for Q_1-Q_3. It should be emphasized that a key feature of this DL-based configuration is that the response time/delay of a single buffer is generally much shorter than the period of the system's main clock. This contributes to increased resolution, pulse falling edge placement, down to a single gate response time, with no significant power losses associated with high frequency clocks and fast phase-locked-loop used in conventional methods. The DL-based architecture of the pulse generation unit, enables to entirely design the controller by HDL (hardware description language), i.e., by pure digital means through direct synthesis [24].

V. IC Implementation

The block diagram of a low voltage sub-nanosecond pulsed current driver IC prototype is shown in Fig. 6. The IC integrates power, analog and digital logic on a single die. Layout constraints such as adding guard rings and isolation wells

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between the devices have been employed to reduce coupling noise and undesired holes/electrons injection. An extra care is taken to layout the high current routes. On one hand, wide metal routes potentially result in electro migration problems and non-uniform distribution along the conductors, while on the other hand low width metal routes contribute to parasitic resistance. This has been resolved in this study by keeping the high current routes as short as possible to minimize redundant metallization resistance.

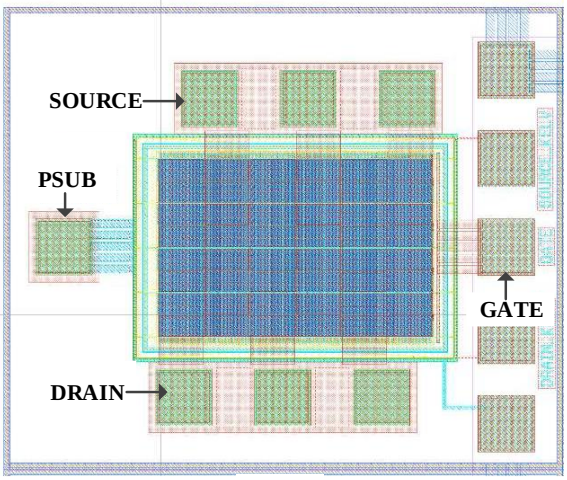
A. Half-Bridge Configuration

A unique feature of the driver IC developed in this study is the low voltage operation, V_{in}=5 V, while capable to provide high amplitude current pulses to the load at high PRF. Since the size factor of the design is a valuable merit as well, the half-bridge power-stage is realized by standard 5V CMOS devices. As shown in Fig. 6, the synchronous half-bridge includes a pMOS high-side switch and an nMOS low-side switch. The switches have been designed symmetrically with silicon on-resistance of 50mΩ (neglecting the parasitic resistances caused by the metallization and bond wires). The effective gate widths of the switches are $W_{g,pMOS}$ =152,000 µm and $W_{g,nMOS}$ =52,800 µm. Realizing the high-side switch by a standard pMOS device, enables a ground-referenced gating signal for the half-bridge (with gate voltage swing between 0-to-5 V), i.e. neither level shifter nor isolation are required. The latter also implies that the driving stage of the half-bridge can be simplified to a single cascaded buffers chain, conserving both the die-area and power consumption.

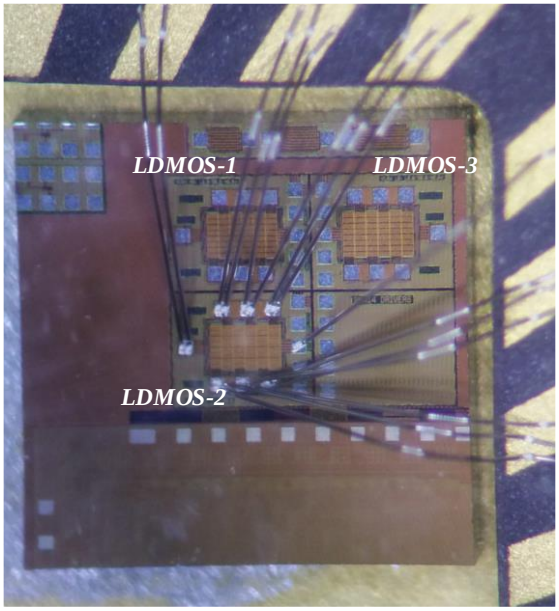
B. Power Switches Characterization

As mentioned in Section III-C, the drain voltage V_{L2} (Fig. 6) of the switches Q_1 and Q_2 can potentially rise over the rated breakdown voltage of the standard 5V CMOS devices. To guarantee the reliability in terms of overvoltage protection of a high-performance power system on-chip, high breakdown voltage LDMOS power devices are used in this study [26]. The transistors Q_1, Q_2 and Q_3 have been implemented symmetrically by a high-voltage 5V-gated nLDMOS.

Another issue associated with power switches is voltage clamping, which is achieved in this work using an avalanche breakdown effect of the LDMOS. Up to-date, practice with lateral device does not allow exceeding more than half of the rated voltage since it may result in permanent damage of the oxides [19], [27]-[29]. However, since in this study, the power driver configuration relies on the avalanche characteristics of the transistors for reliable execution, *repetitive* avalanche effect of the lateral devices has been investigated. A batch of three types of LDMOS transistors with different doping levels and oxide thickness have been fabricated and examined through a life-cycle test. The test forced avalanche conditions with various energy levels, at repetition rates of one MHz over four weeks per device. It has been found that in case that the energy levels applied per avalanche do not exceed the safe operating area of the transistor, the device operates under breakdown



(a)



(b)

Fig. 7. (a) Layout view of the fabricated basic LDMOS power device, (b) Die photo of one fabricated LDMOS power devices for avalanche characterization and evaluation.

conditions without any reliability issues such as drifts, or other oxide memory effects. The layout of a basic LDMOS device that have been fabricated for avalanche evaluation is shown in Fig. 7a, and micrograph of the packaged die is shown in Fig. 7b.

The fabricated LDMOS devices have been experimentally examined to characterize their avalanche ratings. An experimental life-cycle tests, which extended to four weeks per device, have been carried out by driving the devices with a constant current source of 1-A, while applying short turn off pulses repeated at 1 MHz. The clamped voltage of the devices is measured continuously to monitor any potential degradation in the performance. During this experiment different current

TABLE I – *LDMOS-2* SLEW RATE MEASUREMENTS

Current	130mA	225mA	400mA	600mA	800mA	1.5A
Turn ON slew rate [V/ns]	3.3	5.8	14	23	32	33

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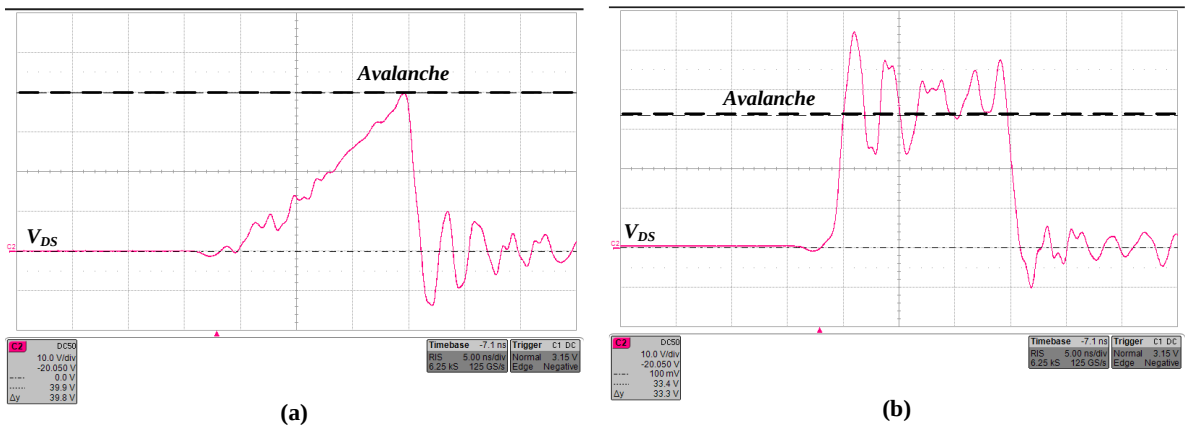

Fig. 8. Slew rate at: (a) 130 mA current; (b) 1.5 A current; Vertical scale: 10V/div, Horizontal scale: 5ns/div.

amplitudes are applied to validate the change of the drain-to-source voltage, V_{DS} rise time. In terms of slew-rate and stable avalanche voltage, the best performance including extreme current cases has been achieved for *LDMOS-2*. The measurements for *LDMOS-1* did not have sufficient and reliable avalanche rating, on the other hand, good avalanche characteristics have been achieved for *LDMOS-3*, however in terms of life-cycle tests it did not provide the target performance. Fig. 8. shows measured results for *LDMOS-2*, there an average avalanche rating of approximately 36V has been measured, for minimum current of 130mA (Fig. 8a) and maximum current of 1.5A (Fig. 8b). The results of the measured slew rates for *LDMOS-2* as a function of the different currents are summarized in Table I. It should be noted that further increase of the current did not improve the voltage slew rate, this is explained by the limitations of the gate driver and relatively large parasitic inductances in the gate-driving path, present in the experimental setup, built of discrete components.

According to the obtained results of the different LDMOS devices, to improve the area-efficiency factor of the driver IC while reliable avalanche characteristics are obtained, a new generation of custom designed LDMOS with avalanche voltage of 18 V has been constructed. To avoid any additional failure risks of the driver IC with the new LDMOS device due to overvoltage at node V_{L2}, and to promote IC compatibility for gate drive application, a monolithic clamping diode rated up to 40V has been integrated as shown in Fig. 6. The diode may be connected to an external clamping voltage rail providing an additional low impedance path, if needed.

C. Current Sensor

To successfully control the half-bridge based current source, accurate current sensing over a wide range is required. In this work, current sensor has been developed and implemented on-chip. The sensor is needed to provide an accurate current reading that are swinging from tens of milliamperes to several amperes, under the frequency range of several MHz. There are several approaches for implementing an on-chip current sensor [30]-[33]. The current-sensing in this study is based on a senseFET approach, (Fig. 9a) providing an accurate sensing, while maintaining reasonable power consumption [30], [34]-[36]. The current sensor is realized by a matched senseFET LDMOS switch M_{SFET}, with a significantly smaller size than that of the main switch Q_1. To achieve an accurate sensing,

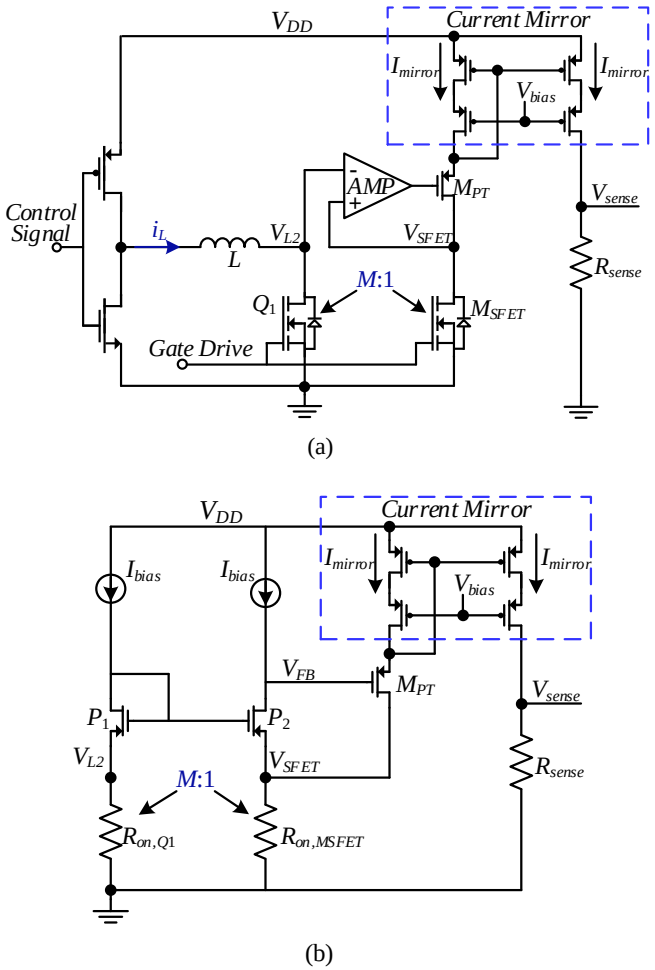

Fig. 9. Current-sensing scheme: (a) System level, (b) Simplified schematic of the sensing circuitry.

equal current densities between the switches are required and assured by equating the operating points of both Q_1 and M_{SFET}. This implies that the same gate drive signal is provided to both Q_1 and M_{SFET}. A trans-impedance amplifier structure [37]-[39] is used to force the same voltage drop at nodes V_{L2} and V_{SFET}. The amplification stage consists of equal bias currents to keep transistors P_1 and P_2 in saturation as shown in Fig. 9b. Transistor M_{PT} provides a feedback path which compensates for any change in V_{L2}, by allowing the required current (which is the mirroring current) to flow through M_{SFET}, forcing V_{SFET} to

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be equal to V_{L2}. The current mirror has been designed in cascode configuration to increase the output resistance reducing the systematic mismatches [40]-[43]. Additionally, the current mirror structure and transistor M_{PT} have been properly sized and matched to guarantee that a sufficient current can be pulled down, such that the amplifier will be able to force the voltages V_{L2} with V_{SFET} to be equal. These conditions result in mirroring of the inductor current I_L to the M_{SFET} with a ratio of M as follows:

$$I_{mirror} = I_L \frac{R_{on,Q_1}}{R_{on,M_{SFET}}} = \frac{I_L}{M}. \quad (1)$$

Given the ratio of M:1 between Q_1 and M_{SFET}, the current I_{mirror} is M times smaller than the actual inductor current $I_{L,}$ in this study the value of M has been set to be 500. To convert the current I_{mirror} to a voltage suitable for the controller operation, the current I_{mirror} is mirrored again to the output of the sensor, and flows through an on-chip poly-based resistor R_{sense}. As a result, the voltage V_{sense} across R_{sense} is proportional to inductor current I_L. Sensing signal V_{sense} is expressed as

$$V_{sense} = I_{mirror} R_{sense} = \frac{I_L R_{sense}}{M}. \quad (2)$$

Poly-based resistors tend to have variations, thus to avoid undesired offsets, rigorous simulation procedure including extreme corners cases and statistical simulations has been carried out, verifying the resistance of R_{sense}. It should be emphasized that although Q_1 and M_{SFET} are implemented by LDMOS power devices, the sensing circuitry is implemented by standard CMOS devices only, resulting in better overall size and power consumption.

D. Rail-to-Rail Comparator

As discussed in Section IV, the controller operation of the driver IC is based on comparison between the inductor's current and a reference/target one. Since the driver IC operates from the range of several milliamperes to several amperes, the comparator should be able to operate at full swing at the input as well as at the output. Thus, a rail-to-rail comparator has been realized as depicted in Fig. 10. A complementary p-channel and n-channel differential pairs are used at the input stage to accommodate a rail-to-rail operation. For low input voltages, the differential pMOS pair is biased, amplifying the voltage difference at the input nodes (*NIN* and *PIN*). In a complementary manner for high input voltages the differential nMOS pair is biased to amplify the input. Comparator's negative input *NIN* is connected to the sensed signal V_{sense} (from the current sensor), where the positive input *PIN* is connected to V_{ref} through a positive resistive feedback network. The feedback resistors R_2 and R_1 are for a hysteresis arrangement to improve the noise-immunity at the input of the comparator. The hysteresis band has been designed to be 60mV, where R_2 and R_1 have been designed to be 836Ω and 68kΩ, respectively. The output stage consists of three cascaded inverters to generate a rail-to-rail output.

To guarantee high matching of both differential pairs for process, voltage and temperature variations [42], the input pairs have been addressed in the layout stage by using common-centroid technique [42], [43]. The active load current mirror structures and bias currents have been implemented using inter

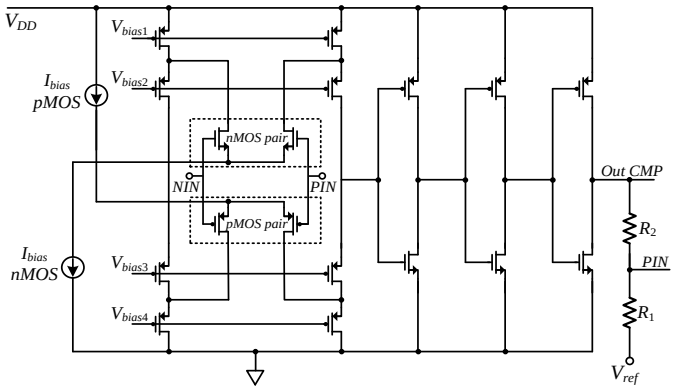
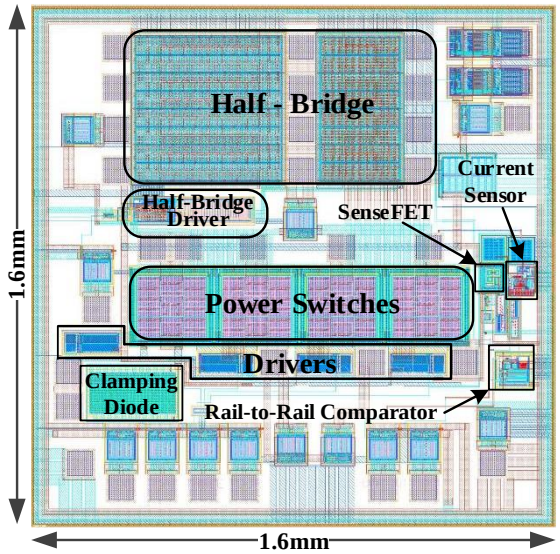
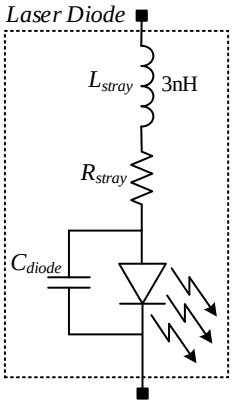


Fig. 10. Simplified schematic of the rail-to-rail comparator.



(a)



(b)

Fig. 11. (a) Chip layout of the driver IC; (b) Laser diode model used for post-layout analysis.

digitation technique to guarantee proper matching between the transistors [43]. Additionally, to further increase the noise-immunity of the diff-pairs, isolating guard rings have been added.

E. Driver IC Post-Layout Verification

A low voltage sub-nanosecond pulsed current driver IC has been designed and implemented in TS 0.18-μm 5V-gated power management process. The overall die area is 2.56mm^2 and the chip layout is shown in Fig. 11a. The driver IC has been

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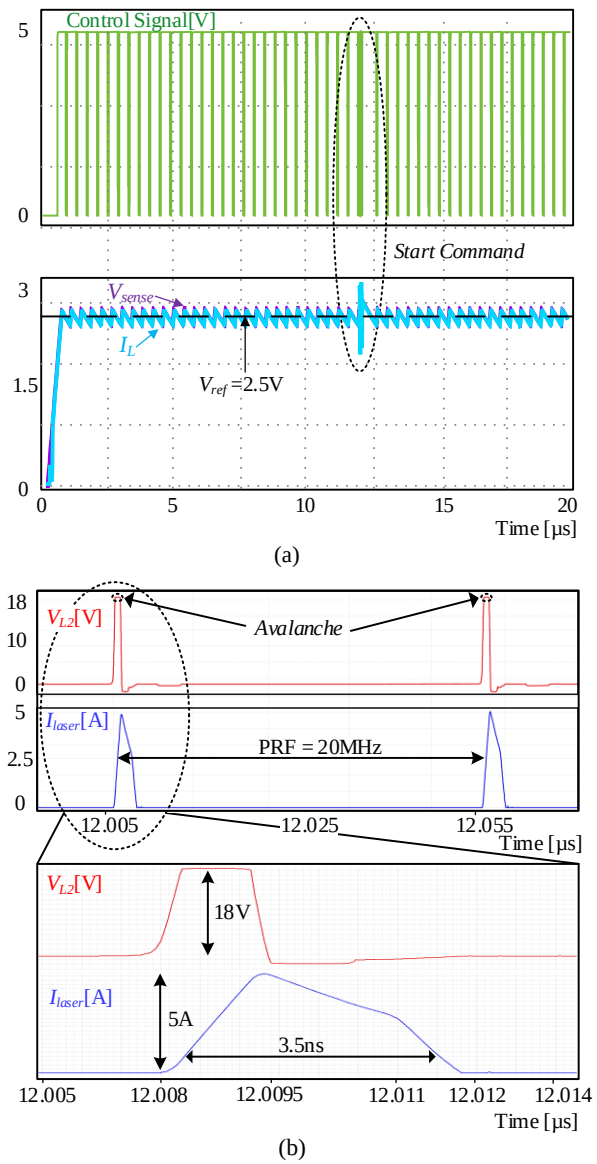

Fig. 12. Post-layout results of the driver IC for I_L=2.5A. (a) Control signal for the half-bridge and sensing signal from the current sensor; (b) Zoom-in on post-layout results of the voltage node V_{L2} and on the laser diode current I_{laser}.

verified with post-layout results using Cadence Spectre simulator, demonstrating a closed-loop operation of the driver architecture. The laser diode has been modeled with ideal elements as shown in Fig. 11b, such that a diode with forward biasing of 2 V combined with parasitic inductance and capacitance of 3 nH and 10 pF, respectively. The control signal for the half-bridge power-stage and gate signals for Q_1-Q_3 generating Vernier sub-resolution pulse width method are produced by a control logic block that has been described through Verilog-A.

Fig. 12 depicts post-layout results for a target inductor current I_L=2.5 A the peak pulse current developed in this case is 5 A from a 5-V input, whereas the IC connects to an external inductor L=1 μH. It can be observed that at steady-state the inductor current settles on the reference level V_{ref} =2.5 V at an operating frequency of 2.5 MHz (Fig. 12a) validating proper operation of the integrated current sensor and comparator. Fig. 12b top plot shows a zoom-in on node V_{L2} and on the laser diode current I_{laser}, with a PRF of 20 MHz, when a start command arrives from the controller. Fig. 12b bottom plot is a single pulse zoom-in of the top plot, which shows the current I_{laser} with a pulse width of 3.5 ns and rise and fall times are approximately 900 ps. Furthermore, it can be seen the target avalanche voltage of 18 V is achieved.

VI. Experimental Results

Experimental validation is divided into two complementary trials. One, presents experimental results achieved using a discrete prototype Fig. 13a and covers the validation of the theoretical concepts developed in this study, including the demonstration of fast rise and fall times, high resolution pulse width generation capability, spanning a wide range of pulse currents, peaking at a maximum of nearly 20 amperes. The other trial, presents a narrower validation of theoretical concepts, while concentrates on the fabricated driver IC operation combined with an FPGA-based controller validation Fig. 13b. IC system operation with its submodules is demonstrated and a proof of concept realization is provided.

In the first set of experiments, discrete prototype has been designed for validation of principle of operation of the driver architecture and the method to shorten the fall time of the laser diode current. The experimental system is built from a constant current source, implemented using a current controlled half bridge converter, followed by a network of power switches according to Fig. 2a. The laser diode that has been used for validating the driver architecture is PGAS1S03H by Excelitas. The light output has been obtained via a custom designed sensor, suitable for fast signals, tightly terminated, skewed and calibrated to obtain a signal. The sensor was based on a photodiode from Hamamatsu Photonics (S5973). Light measurement in these experiments represents the shape of the current flowing through the laser diode. The Oscilloscope, which has a bandwidth of 1GHz was not sufficient enough to capture a consistent singular signal. To this end, the RIS feature (Random Interleaved Sampling – an oversampling based on accumulation of repeated results) has been employed so that a consistent clear waveform can be presented for halted presentation (as opposed to live view on the oscilloscope).

Experimental measurements of anode voltage of the laser diode, and the photodiode output voltage, which is proportional to the laser light output, are shown in Fig. 14. The results without the clamping assistance of the series switch Q_3, are given in Fig. 14a, b and c, as can be seen, the fall time of the current is very long, approximately 20 ns. This is due to the residual current in the parasitic inductances leading to the laser diode, preventing shorter current pulses. Fig. 14d, e and f, show experimental measurements with the clamping aid of the series switch Q_3. It can be observed that a pulse width of 5ns is obtained, which is significantly shorter. The rise time that has been achieved using discrete setup is approximately 2-2.5 ns. The results are consistent over a wide range of currents. Fig. 14a and d present the results for 20 A current pulse, Fig. 14b and e present the results for 16 A current pulse, Fig. 14c and f present the results for 12 A current pulse. A small delay could be observed in the experimental results shown in Fig. 14, which is primarily due to the optical sensor response time.

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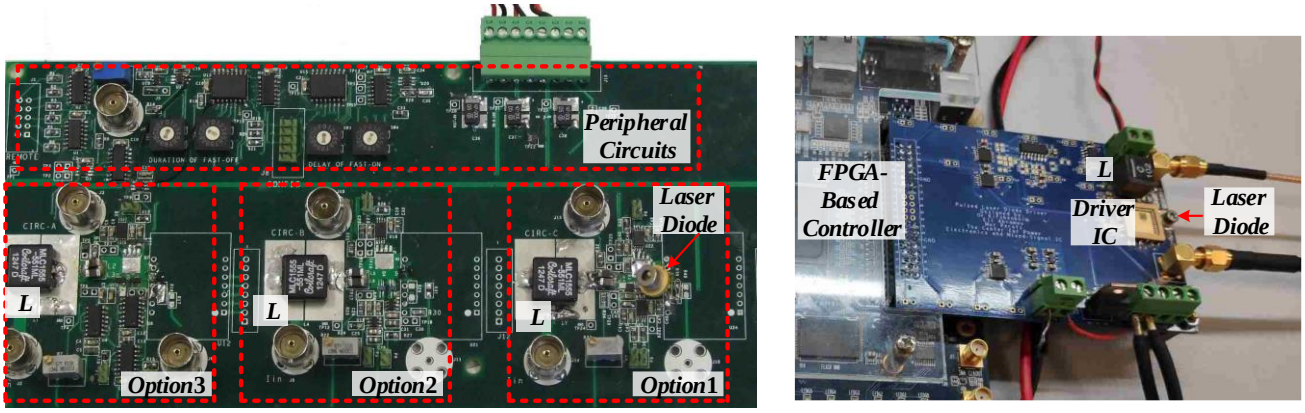
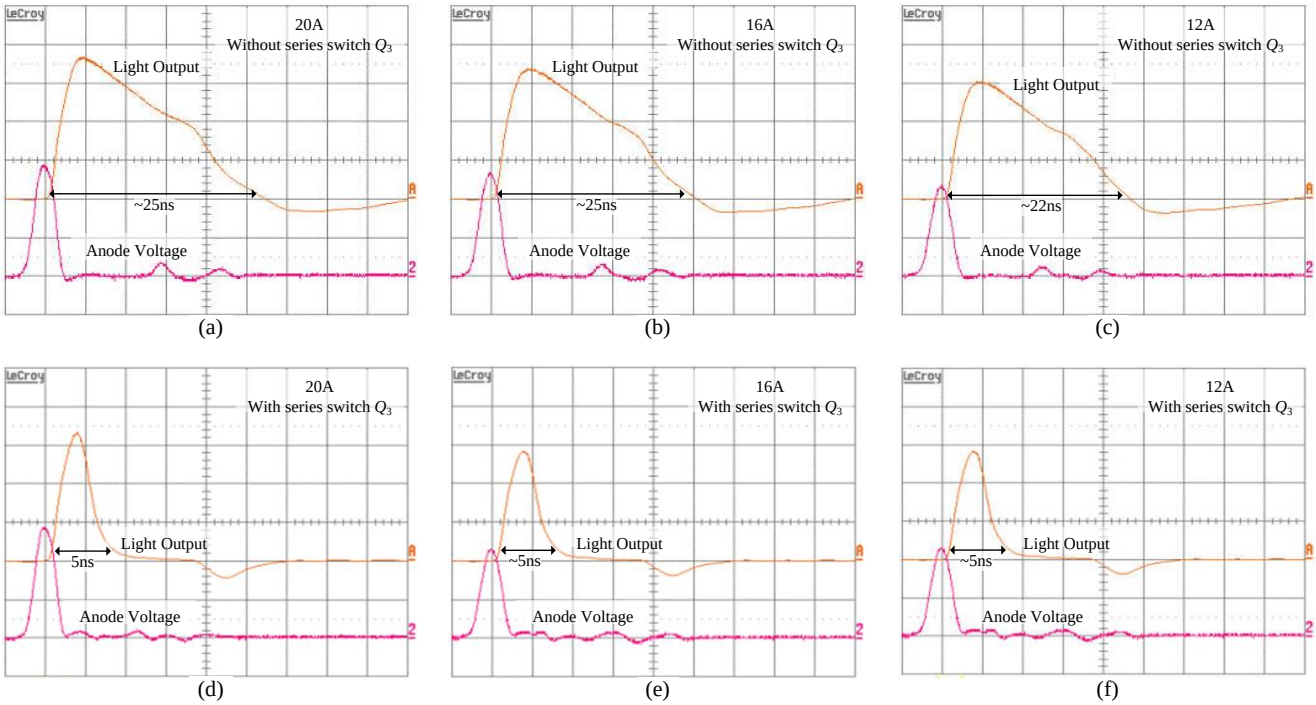


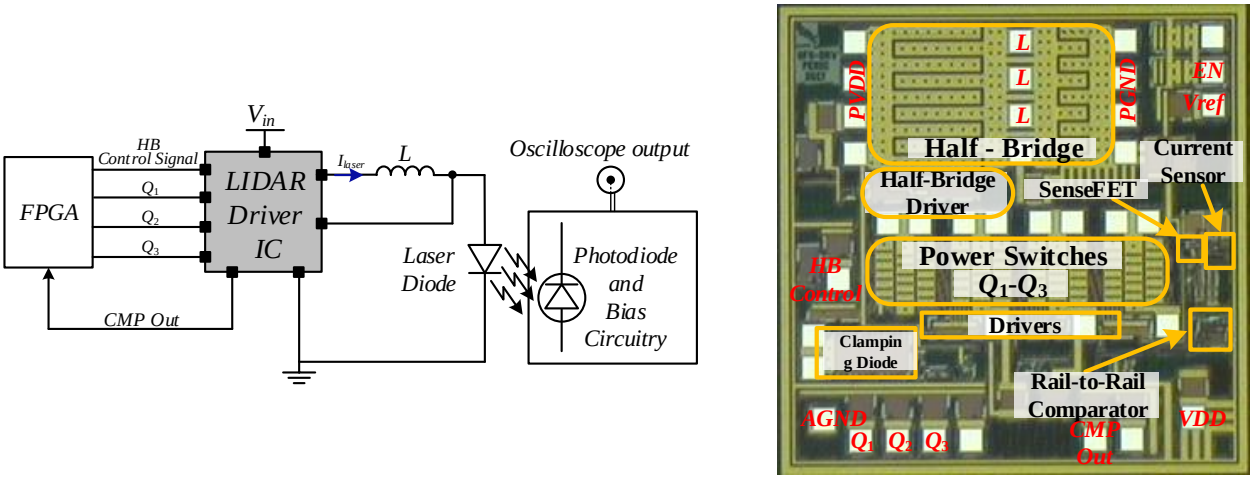
(a) (b)

Fig. 13. Experimental setups: (a) Discrete prototype includes several circuit options; (b) IC prototype (Driver IC is soldered on an evaluation PCB).



(a) (b) (c) (d) (e) (f)

Fig. 14. Discrete prototype experimental results: (a)-(c) without series switch Q_3, (d)-(f) with series switch Q_3. Light output (top trace), laser diode anode voltage (bottom trace); Voltage scale 20V/div, Horizontal scale 5ns/div.



(a) (b)

Fig. 15. (a) Test setup for the LIDAR driver IC, (b) Fabricated driver IC die microphotograph.

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For the second set of experiments, the fabricated current driver IC has been examined. The controller hardware has been fully coded in Verilog and implemented on a Altera Stratix IV FPGA using Quartus environment, whereas the delay of a single buffer element, $t_{d(Buf)}$, is approximately 200 ps. A diagram of the IC test setup is shown in Fig. 15a and die microphotograph is shown in Fig. 15b. The overall operating conditions and parameters of the driver IC prototype are summarized in Table II, in addition, comparison between post-layout and experimental results of the driver IC is given in Table III. Due to the current limitation of the on-chip devices, the validation has been carried out with currents of up to 5 amperes. The results without the clamping assistance of series switch Q_3 are given in Fig. 16a, non-clamped behavior has been achieved by forcing Q_3 to conduct continuously. The results with clamping assistance are shown in Fig. 16b. Current fall time without clamping assistance stands on 7 ns, while the clamping assistance of the switch Q_3 cuts the fall time almost three times to around 2.5 ns, and the pulse width of 5 ns is obtained. Another important demonstration is the current rise time that drops below 1 ns in an on-chip implementation. To achieve the highest possible rise time the quality factor of the resonant circuit formed by the parasitics was pushed as high as possible, resulting in the current shape shown in Fig. 15, and double the current peak relative to the current set by the source. As in the discrete prototype trial, small delay could be observed here as well, introduced by the optical sensor.

TABLE II – SUMMARY OF DRIVER IC PROTOTYPE EXPERIMENTAL MEASUREMENTS AND TEST CONDITIONS

Specifications	***Value/Type***
Input voltage V_{in}	5-V
Photodiode	Hamamatsu-S5972
Laser diode	Excelitas-PGAS1S03H
Laser diode peak current I_{laser}	5 A
Off chip inductor L	1 μH
Switching frequency f_s	2.5 MHz
Buffer delay $t_{d(Buf)}$	200 ps
Rise \ Fall times	~900 ps / 2.5 ns
Current pulse width	5 ns
Total chip Si Area	2.56 mm^2

TABLE III – COMPARISON BETWEEN POST-LAYOUT AND EXPERIMENTAL RESULTS OF THE DRIVER IC

Specifications	***Post-Layout***	***Experimental***
Avalanche voltage	18 V	18 V
Average current	2.5 A	2.5 A
Peak current	5 A	5 A
Rise time	~900 ps	~900 ps
Fall time	~900 ps	2.5 ns
Current pulse width	3.5 ns	5 ns
Total chip Si Area	2.56 mm^2	2.56 mm^2

VII. CONCLUSIONS

A new low voltage sub-nanosecond monolithic pulsed current driver for LIDAR applications has been presented. Unique combination of driver architecture, based on controlled current source, and Vernier high-resolution pulse-width activation sequence that are developed in this study, demonstrate robust performance and very short rise and fall times. An on-chip low voltage driver prototype has been designed and implemented in a TS 0.18-μm 5-V-gated power

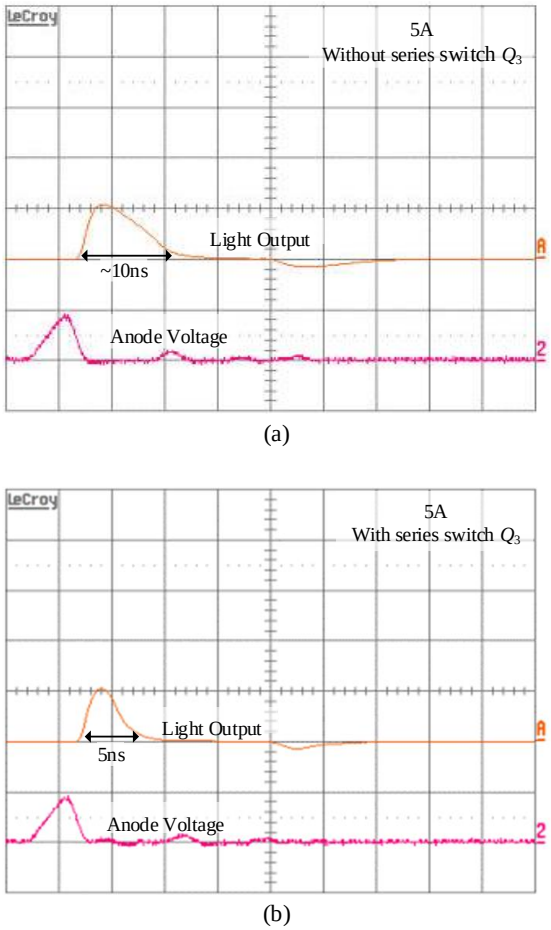

Fig. 16. Driver IC prototype experimental results: (a) without series switch Q_3, (b) with series switch Q_3. Light output (top trace), laser diode anode voltage (bottom trace); Voltage scale 20V/div, Horizontal scale 5ns/div.

management process. The IC includes power devices, wide range senseFET-based current sensor, and a rail-to-rail comparator for current feedback loop. A characterization of the avalanche capabilities of the integrated lateral MOSFET power devices required for the driver IC has been carried out. Three different LDMOS power devices have been custom designed and experimentally evaluated for a life-cycle performance characterization. In addition, a delay-line based controller to generate high-resolution pulses for the current driver IC is realized through hardware description language (HDL), i.e., by pure digital means without additional custom design.

Post-layout analysis of the power driver IC fed with 5-V input voltage, demonstrates laser pulse light output rise and fall times on the order of hundreds of picoseconds, and currents of up to 5-A, validating the theoretical predictions. Further validation of the theoretical concepts includes two Experimental setups, fabricated IC evaluation and a laboratory prototype based on discrete components. The concepts of high-resolution Vernier pulse width and short fall time has been experimentally tested on both the IC and discrete prototype setups demonstrating an excellent agreement with the theory. To the best of the authors' knowledge, this circuit presents the first integrated LIDAR driver that is based on a controlled current source architecture with a pulse width resolution on the order of hundreds of picoseconds.

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