

# Digital CPM Controller for Non-Inverting Buck-Boost Converter with Unified Hardware for Steady-State and Optimal Transient Conditions

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**Abstract** – This paper introduces a new current-programmed controller for non-inverting buck-boost converters. The controller facilitates tight voltage regulation and excellent transient convergence, all carried out through a simple CPM controller hardware. Steady-state operation for the full range of conversion ratios is supported with seamless transitions between modes and improved efficiency and ripple characteristics around unity conversion gain. In case of a load transient, an optimized boundary control scheme achieves near-optimal recovery, with programmable constrains for the voltage deviation and inductor current, covering the entire range of conversion ratios. The operation of the controller is experimentally verified on a 2-15V input to 3.3V output, non-inverting buck-boost converter, demonstrating significant improvement in steady-state around unity gain as well as fast convergence for load transients with programmable constraints for the output voltage deviation and inductor current.

**Keywords** – Digital control, state-space control, non-inverting buck-boost, efficient energy processing.

## I. INTRODUCTION

Following the rapid growth in computing power and in particular for portable electronics, the specifications and restrictions on efficient usage of battery-powered applications have been significantly tighten to assure compact and light devices with long operation cycles. In variety of such applications, in particular as those prone to wide range of ambient temperature swing [1], or for cells with wide voltage range [2]-[5], the source voltage can be higher or lower than the target regulated output. Another case that requires front-end conversion flexibility is for high-performance programmable-gate arrays (PGAs) that may be fed by multiple sources [6].

It is apparent that a flexible SMPS capable of stepping down, up, or operating around unity is essential. In addition, since direct conversion as point-of-load is preferred due to efficiency considerations, then the SMPS is also required to satisfy transient requirements and comply with the system dynamic characteristics [7]-[9]. Non-Inverting Buck-Boost (NIBB) converter configuration has a long track-record of carrying out the above-mentioned prerequisites. Although it comprises of four switches with two devices in the conduction path, its efficiency characteristics and ripple efforts have demonstrated superiority in comparison to a conventional buck-boost arrangement. One of the more attractive features of NIBB converters is the capability of operating as a buck

converter when step-down operation is needed and as a boost for step-up. Remaining is the region around unity in which, apparently, this converter lacks advantages than its precursor. Fortunately, several fundamental studies in the recent years [9]-[11], have been conducted around the unity region and demonstrated ripple and efficiency enhanced modes of operations. A key challenge would be to embed all required features as well as superior transient capabilities in a simple and unified controller.

Load transient recovery is a critical factor in the design of modern switch-mode power supplies. In particular, sizing of the passive components predominantly depends on the recovery pattern of the system, since largest deviations occur during transient events. To reduce the requirements of the converter's passives and as a result, the overall volume of the SMPS, high-performance voltage regulators typically employ transient-oriented controllers, which can be either boundary or hybrid. Boundary controllers [12],[13], among them hysteretic and sliding-mode controllers, are geometry-based methods that split the state-plane such that in one side of the boundary the operation is governed by the on state and by the off state at the other side of the boundary. Hybrid controllers [14],[15] switch between two or more control laws based on the system state variables in order to obtain the performance goals. Within the context of switch-mode applications, the hybrid control law typically incorporates a steady-state linear controller (i.e., PI or PID), to allow constant operating frequency, which simplifies

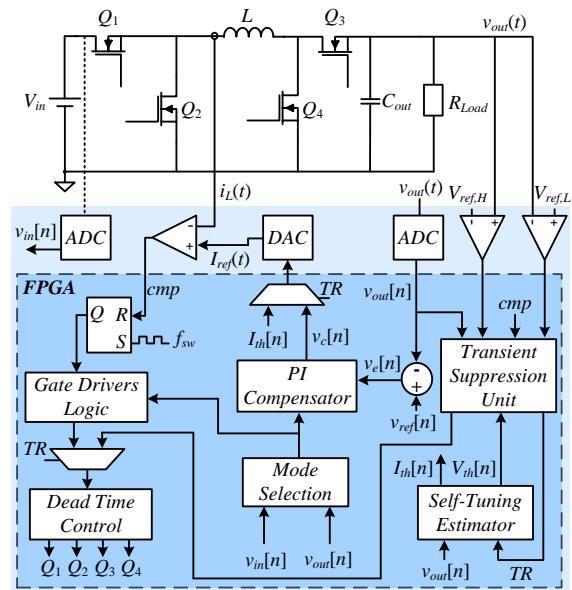


Fig. 1. Simplified schematic diagram of a non-inverting buck-boost converter with current-programmed controller.

the design of the power converter.

As opposed to buck-type conversion, which is classified as direct-energy transfer and characterized with closed-form optimal solution for the load transient recovery and deviation, in boost-type circuits general optimization of the recovery targets is significantly more complex. For example, time-optimal recovery of buck-boost converter results in extensive voltage drop, much larger than the minimum value that can be obtained [16]. However, ideal minimal voltage drop for boost-type conversion requires infinite convergence time. On the other hand, since in this study a NIBB converter configuration is used to support wide range of conversion ratios, it stands to reason that the recovery pattern may be further enhanced, beyond the conventional definition of time-optimality, benefiting from the topological flexibility of the converter. For instance, adding boosting phase to a loading step while in step-down conversion (buck mode in steady-state).

The objective of this study is to introduce a new controller architecture and implementation for NIBB converter as shown in Fig. 1. It employs a simple current-programmed configuration to realize a hybrid-type controller with tight voltage regulation and excellent transient convergence, all carried out through a classic two-loop controller hardware. A new steady-state operation mode for improved efficiency and ripple characteristics around unity conversion ratio is described and analyzed. The new controller supports operation in steady-state for the full range of conversion ratios with seamless transition between modes. It is a further objective of this study to introduce detailed transient mitigation algorithms for all operation modes, in particular for the unity conversion ratio but also for the entire operation range, enabling optimized transient recovery and untimely volume reduction of the overall solution. In addition, a load estimation procedure is delineated and demonstrated which considerably enhances the transient performance.

The rest of the paper is organized as follows: Section II describes the unified controller architecture and details its principle of operation. Section III covers the transient control scheme in the various regions of conversion modes. Practical implementation aspects are addressed in section IV. Experimental verification is provided in section V. Section VI concludes the paper.

## II. CONTROLLER ARCHITECTURE AND OPERATION

The NIBB converter, shown in Fig. 1 has four switches, which can be divided into two pairs:  $Q_1$  and  $Q_2$  make up the buck pair while  $Q_3$  and  $Q_4$  make up the boost pair. The operation for each pair of switches is complementary. The control objective in this study is to sustain a regulated output voltage for any setting of the input voltage (within the design specifications), which may be above, below or equal to the target output, and significantly vary during operation. To this end, the system governor adjusts the switching sequence so that the converter operates at the best performing configuration for the specific voltage gain. By assignment of two duty ratio notations,  $d_{buck}$  for the pair of  $Q_1$ - $Q_2$  and  $d_{boost}$  for  $Q_3$ - $Q_4$ , then the dc conversion ratio for NIBB converter can be uniformly expressed (i.e., regardless of information for the specific mode of operation) as [9]:

$$\frac{V_{out}}{V_{in}} = \frac{d_{buck}}{1-d_{boost}}. \quad (1)$$

In the following, the architecture and operation of the new controller are detailed. Emphasis is given to the challenges of the continuously varying input voltage and efficient regulation around unity conversion ratio.

### A. Controller Architecture and Operation

As can be seen in Fig. 1, the controller follows a two-loop current-programmed configuration with a digital outer voltage loop and inner comparator-based current loop. The voltage loop produces a digital reference,  $v_c[n]$  based on the error signal,  $v_e[n]$ , of the voltage loop for either the peak or valley current values, depending on the operation mode. The reference current values are converted to continuous-time representation by a digital-to-analog converter (DAC) which feeds the positive input of a comparator.

To ensure proper regulation of the output voltage for all conversion ratios, a state-machine algorithm described by the flowchart of Fig. 2, has been incorporated. The mode of operation (i.e., step-up, step-down or unity) is determined in this study by samples of the input voltage,  $v_{in}[n]$  and output voltage,  $v_{out}[n]$ , which are the inputs to the mode selection block (see Fig. 1). To prevent toggling and to ensure smooth transition between modes, the assignment of the operation mode is determined based on the steady-state value for the output voltage,  $v_{ref}[n]$ , and in addition, a hysteresis band is assigned around unity conversion ratio.

Efficient way that exploits the flexibility of this converter is to operate in the dedicated converter topology that is suitable for the conversion ratio based on the status of the input and output voltages. In this way, rather than operating in buck-boost mode for the entire range, a buck setup is preferred for step-down conversion, whereas step-up conversion is to be performed with a boost arrangement. It has been established in [17],[18] that this approach improves the power conversion efficiency and reduces the components ripple. Still remaining however, is the region around unity conversion ratio where buck-boost operation prevails since neither buck nor boost converters can achieve pure unity conversion while regulating the output voltage. To this end, several approaches to lower the ripple efforts have been pursued in recent years [9],[17]. This study too adopts the approach of operating in an enhanced mode around unity conversion ratio, with some unique adjustments of the enhanced modes selection and realization. To cover all conversion modes and move between them seamlessly, the operation of the steady-state controller has been segmented into four. There are two conventional cases of buck and boost, and two new modes of enhanced-buck and enhanced-boost, which are distinguished by the voltage status around the unity conversion ratio. The topology subcircuits for all operating modes are shown in Fig. 3 with typical current waveforms in Fig. 4.

For the case that  $V_{in} > V_{out}$ , the controller operates in a conventional buck mode. Here,  $Q_3$  is kept on,  $Q_4$  is off and the pair  $Q_1$  and  $Q_2$  toggles complementary. Voltage regulation is facilitated through valley current control, which determines the duty ratio of the toggling transistor pair. Equivalent subcircuits

for this operation mode are shown in Fig. 3b-c with inductor current shown in Fig. 4a.

For the case that  $V_{in} < V_{out}$ , the controller operates in a conventional boost mode. The passive pair here is  $Q_1-Q_2$  while  $Q_3-Q_4$  switching complementary (Fig. 3a-b). To utilize the same control hardware without modification, peak current control now determines the duty ratio for output voltage regulation (see Fig. 4b).

The enhanced-buck mode is engaged where the input voltage is slightly higher than the output voltage. In this case, the conventional valley current control, employed for the pure buck mode, is modified to a three-phase sequence for a switching period, resulting in inductor current waveform as shown in Fig. 4c. In the first interval  $t_{e1}$ ,  $Q_2$  and  $Q_3$  are on (subcircuit Fig. 3b) and the inductor current ramps down with a slope of  $(-V_{out})/L$  to the valley value assigned by the current reference. The second interval  $t_{e2}$  is a short boosting phase (subcircuit Fig. 3a) where the inductor current ramps up with a slope of  $V_{in}/L$ . The duration of the second time interval,  $t_{e2}$ , is chosen according the minimum conduction time of the power stage transistors and drivers,  $t_{min}$ , so that the following holds:  $t_{e2} > t_{min}$ . In the third interval  $t_{e3}$  (subcircuit Fig. 3c) the inductor current continues to ramp up, but with a moderate slope of  $(V_{in} - V_{out})/L$ , until the end of the cycle. The boosting phase timing can be realized by either assignment of a fixed duty ratio  $d_{boost}$  as employed in [9],[10], or as carried out in this study by changing the reference value to the comparator. Using the latter, cycle-by-cycle protection merit is maintained continuously along the entire range of conversion ratios.

Enhanced-boost mode is used for the case that the input voltage is slightly lower than the output voltage. In a similar way as the previous mode, a three-phase sequence is utilized, now with the difference that peak current value is initially obtained. A typical inductor current waveform for this case is depicted in Fig. 4d. Here, in the first interval  $t_{e1}$ , the current ramps up with a slope of  $V_{in}/L$  (subcircuit Fig. 3a). Then, in  $t_{e2}$ , the inductor discharges onto the load with a slope of  $(-V_{out})/L$ . Finally, in  $t_{e3}$ , the inductor current ramps down in buck-mode with a moderate slope of  $V_{out}/L$ . To facilitate the second phase,

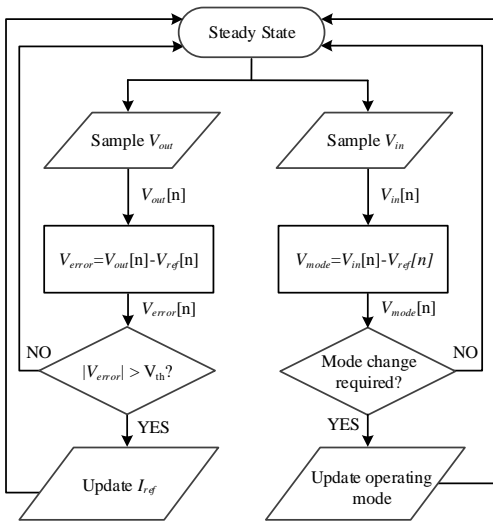


Fig. 2. Flowchart of the controller's operation in steady-state.

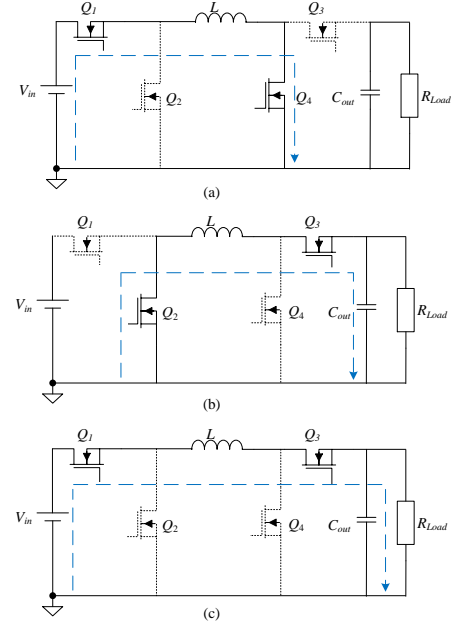


Fig. 3. Equivalent circuit of the non-inverting buck-boost converter in various stages of operation.

here too there are two options; One with a fixed duty ratio [9],[10], now  $d_{buck}$ . The second alternative, which has been carried out in this study, is by the current comparator.

From the above description, it implies that a single-comparator current-mode architecture is sufficient to all four modes, covering the full range of conversion ratios with enhanced conversion efficiency and lower ripple effort around unity ratio. These are achieved while retaining cycle-by-cycle current protection and simplifying the voltage-loop compensator by reducing the system order, because of the tight current-programmed control [19],[20]. A simple slope compensation configuration is also employed which supports all operating modes [21]. In addition, since information on both state variables is available to the controller, it enables to facilitate optimal load transient recovery by employing boundary or sliding-mode control law without hardware modification - this is addressed in the next section.

### B. Impact of the Operation Mode on the Inductor's Current rms Value

Conduction losses are a primary contributor to the efficiency of buck-boost converters, in particular around unity conversion ratio. Since this study presents a modified operating sequence, it is essential to explore the effect of the new current waveform on the rms value. The analysis in this subsection is carried out in the context of the presented control method, i.e. it is generalized for wider range of conversion ratio, considering the operating mode per the status of input and output voltages.

The inductor's current in enhanced-boost and enhanced-buck modes can be divided into three sections, as can be seen in Fig. 5a and Fig. 5b. The rms value of the inductor current can be derived using the sum of the squares as follows [23]:

$$I_{Lrms} = \sqrt{I_{Lrms(1)}^2 + I_{Lrms(2)}^2 + I_{Lrms(3)}^2}, \quad (2)$$

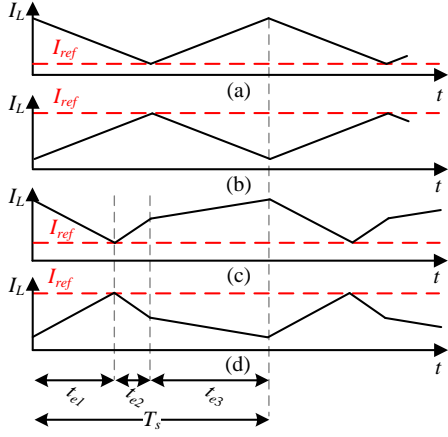


Fig. 4. Inductor current waveforms in various modes (a) conventional-buck (b) conventional-boost (c) enhanced-buck (d) enhanced-boost .

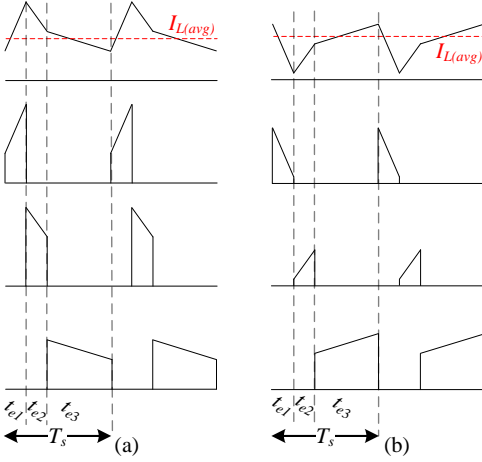


Fig. 5. Current waveforms around unity conversion ratio. (a) enhanced-boost mode, (b) enhanced-buck mode. Division to three intervals with known shapes.

where  $I_{Lrms(1)}$ ,  $I_{Lrms(2)}$ ,  $I_{Lrms(3)}$  are the rms values of the three parts of the inductor current waveform. The rms value of the inductor's current when operating in conventional buck, conventional boost and conventional buck-boost modes can be expressed as [10]:

$$I_{Lrms\_buck} = \sqrt{I_{out}^2 + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2}. \quad (3)$$

$$I_{Lrms\_boost} = \sqrt{\left(\frac{I_{out}}{1 - \frac{V_{out} - V_{in}}{V_{out}}}\right)^2 + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2}. \quad (4)$$

$$I_{Lrms\_buck-boost} = \sqrt{\left(\frac{V_{out} + V_{in}}{V_{in}} I_{out}\right)^2 + \frac{1}{12} \left(\frac{V_{out} V_{in} T_s}{(V_{out} + V_{in}) L}\right)^2}. \quad (5)$$

To facilitate comparison benchmark, the inductor's current rms value has been normalized with respect to the highest rms value of a conventional buck-boost mode, as can be seen in Fig. 6. Also added are independent simulation results, that validate the correctness of the expression in (2), as shown in Fig. 6. The result implies that when feasible, operation in either pure buck or boost is preferred. However, around unity

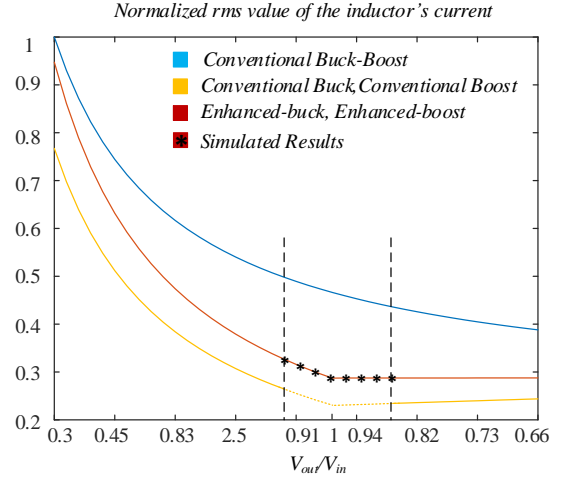


Fig. 6. Normalized rms values of the inductor current under various operating modes.

conversion, the new shape for the current as obtained by the enhanced modes, results in lower conduction losses in steady-state compared to conventional approaches.

### C. Variable Frequency Operation

To further improve the conversion efficiency, frequency scaling is employed. Operation at high conversion ratio calls for higher frequency operation to lower the ripple efforts and by doing so, reduce the size of the passive components. When operating around unity conversion ratio however, it is possible to lower the operating frequency and by that reduce the switching losses, and more importantly, drive losses. In the enhanced modes, the second time-interval ( $t_{e2}$ ) with respect to the cycle duration, determines the average value of the inductor current, which is expressed as:

$$I_{L(avg)\_enhanced-buck} = I_{out} \frac{1}{1 - \frac{t_{e2}}{T_s}}. \quad (6)$$

$$I_{L(avg)\_enhanced-boost} = I_{out} \frac{1}{\frac{t_{e2} + \frac{V_{out} - V_{in}}{V_{out}}(T_s - t_{e2})}{1 - \frac{V_{out}}{V_{in}}}}. \quad (7)$$

As can be seen from these expressions, keeping the correct ratio between the second interval to the switching period assures that the average current, and hence the load current, are satisfied. This implies that lowering the switching frequency is allowed without jeopardizing the performance, and even improving it. It should be noted however, that a secondary constraint of the maximum allowed ripple sets a lower limit on the frequency. The controller in this study has been designed so that the constraints are met while the switching frequency is adjusted according to the difference (or ratio) between  $V_{out}$  and  $V_{in}$ .

## III. TRANSIENT CONTROL

### A. Programmable-Deviation Controller

In this section, two recovery patterns are presented within the context of indirect energy transfer conversion (as NIBB) that, compared to the time-optimal solutions, constrain the output voltage deviation or peak inductor current (or both)

while maintaining fast convergence in response to load transients. A primary objective in the controller design is to maintain the same hardware for all cases in the steady-state as well as for transients. Therefore, the hybrid controller incorporates the steady-state peak current programmed mode (CPM) arrangement and adds a transient-mode controller. For the transient-mode, two additional logic blocks have been developed, namely the *transient suppression block* and *self-tuning estimator* (see Fig. 1). Upon a load transient detection, these blocks take over the task of estimating the load current and creating the gating signals to the power switches.

The first recovery profile that is described is current-constrained recovery as illustrated in Fig. 7. Upon detection of a loading transient, from  $I_{old}$  to  $I_{ref}$ , the controller recovers from the loading event in a two-step process. First, the CPM controller is bypassed and  $Q_1$  and  $Q_4$  are turned ON while  $Q_2$  and  $Q_3$  remain OFF, while the new load state is estimated. During this time and based on the new load estimation, the controller sets a threshold for the inductor current,  $I_{th}=I_{ref}$ . Once the inductor current reaches the assigned threshold, the controller moves along the boundary  $I_L=I_{th}$  in a sliding mode operation, causing the output voltage to rise up without changing the inductor current. The definition of the controller and its realization is quite simple and features simple current comparison with some hysteresis band. As a sliding controller, it can be defined as follows:

$$\begin{aligned} \sigma_i(v_C, i_L) &= i_L - I_{ref}, \text{ for } v_C < V_{ref} \\ \text{on: } \sigma_i < 0 \quad \text{off: } \sigma_i > 0 \end{aligned} \quad (8)$$

The second recovery profile applies constraints on both the output voltage to a desired level and on the inductor current, here the new steady-state value has been assigned. The recovery is described through a three-step process and is illustrated in Fig. 8. First, in a similar way as in the previous mode, the inductor current is ramped up, while the controller

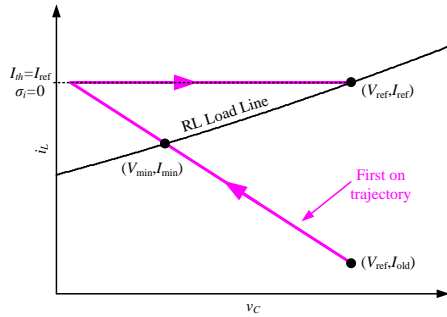


Fig. 7. Illustrative movement of the state plane for the current-constrained mode handling a loading transient.

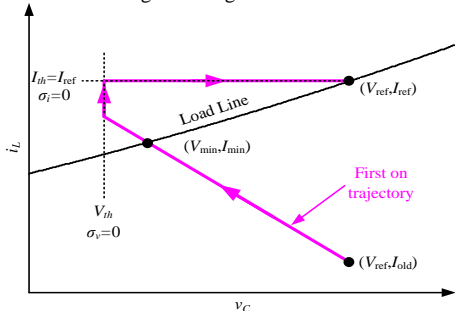


Fig. 8. Illustrative movement of the state plane for the voltage-deviation and current-constrained mode handling a loading transient.

sets two thresholds: one for the output voltage and one for the inductor current based on the load estimation. In the second step, the controller is assisted by the voltage threshold to operate as a sliding-mode controller that is defined by

$$\begin{aligned} \sigma_v(v_C, i_L) &= v_C - V_{th}, \text{ for } i_L < I_{th} \\ \text{on: } \sigma_v > 0 \quad \text{off: } \sigma_v < 0 \end{aligned} \quad (9)$$

During this step, the inductor current rises without changing the output voltage until it reaches the current threshold and the controller moves to the third step. During the third and final step, the controller moves along the boundary  $i_L=I_{th}$  in a sliding mode operation, this can expressed as:

$$\begin{aligned} \sigma_i(v_C, i_L) &= i_L - I_{th}, \text{ for } v_C < V_{ref} \\ \text{on: } \sigma_i < 0 \quad \text{off: } \sigma_i > 0 \end{aligned} \quad (10)$$

Optimized boundary control scheme covering the entire range of conversion ratios has been designed based on the above-mentioned recovery profiles for loading events and conventional time-optimal solutions for unloading events. The design approach is aided by the analytical derivation of the converter's state trajectories and load-line combined with graphical illustrations of the state-plane for various voltage gains.

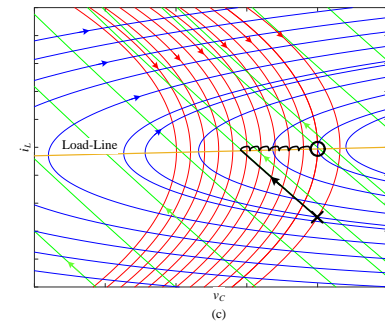
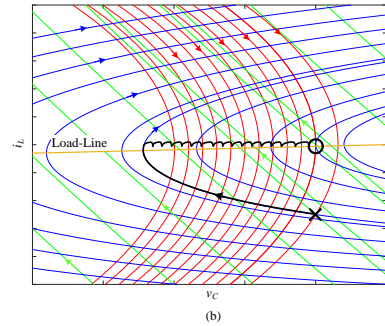
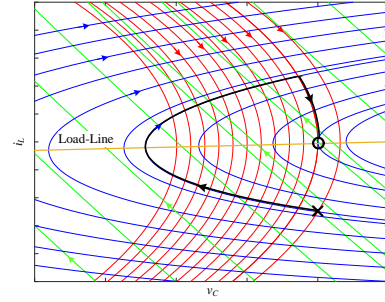


Fig. 9. State plane representation of NIBB operating in enhanced-buck mode for a loading transient. (a) Recovery pattern of conventional Time-Optimal Control (TOC). (b) Recovery pattern of current-constrained mode in conventional buck mode. (c) Recovery pattern of current-constrained mode in enhanced-buck mode with a boost-phase.

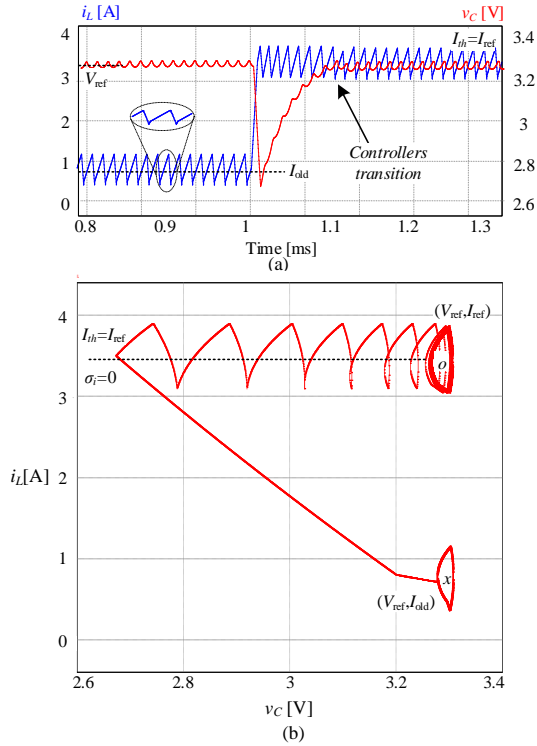


Fig. 10. Simulated response of the current-constrained controller to a 0.8-3.5 A loading transient of a NIBB converter in enhanced-buck mode. (a) Inductor current (blue) and output voltage (red) (b). State-plane representation of the output voltage and inductor current.

In both recovery profiles, the switching frequency of the power devices during sliding-mode operation is determined by a hysteresis band around the reference value. It is set according to the maximum allowed ripple and takes into account the frequency limitations of the power-devices and drivers used in the design.

The selection of the specific recovery pattern relates to the sensitivity of the design to specific components. For example, should the inductor current in the design must not exceed a certain limit then the current-constrained controller is to be employed. This controller realization provides flexibility in the selection of the hardware by choosing the recovery pattern based on the available sensors per specific design.

The controller recovery pattern for loading events in enhanced-buck mode is an example of exploiting the topological flexibility of the NIBB converter to further improve the transient response while reducing output voltage deviation as well as lowering the peak inductor current that is required for recovering to the new steady-state. Illustrations of the state-plane as well as the specific recovery trajectories for loading transient, in enhanced-buck mode are depicted in Fig. 9. The two constrained recovery profiles (Fig. 9b-c) presented earlier in this section are compared with time-optimal pattern (Fig. 9a) as a benchmark case. It can be seen that while a conventional buck time-optimal recovery ramps the inductor current up by with a slope of  $(v_{in}-v_{out})/L \approx 0$ , here the addition of a boosting phase ramps up the inductor current with a slope of  $v_{in}/L$ . This improvement alone significantly enhances the recovery performance on both deviation and time properties since it increases the applied voltage on the inductor. In a similar manner, recovery of enhanced-boost mode for the

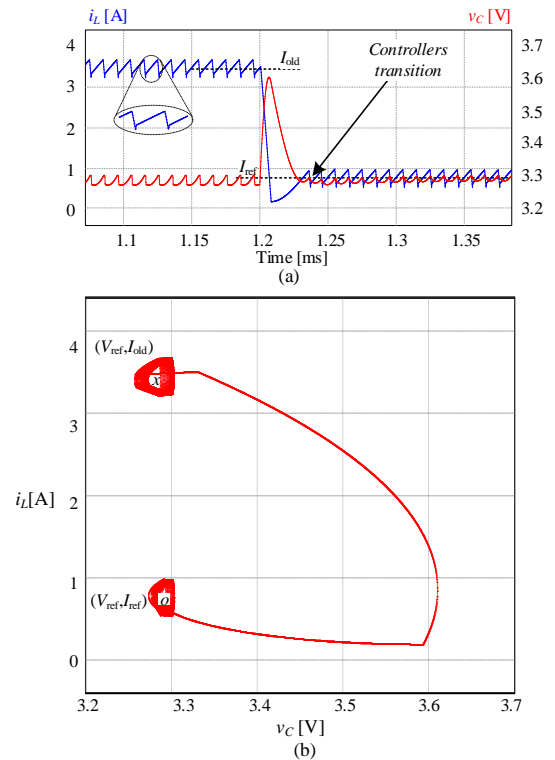


Fig. 11. Simulated result of time-optimal controller to a 3.5A to 0.8A unloading event of a NIBB converter operating in enhanced-buck mode. (a) Inductor current (blue) and output voltage (red). (b) State-plane representation of the output voltage and inductor current.

NIBB converter is found to superior over the one of a conventional boost. This has been widely detailed in [15].

To demonstrate the operation of the transient recovery pattern, simulation testbench (in PSIM) has been constructed. Fig. 10 shows the resultant recovery pattern for 0.8A to 3.5A loading transient, while the converter operated in enhanced-buck mode (3.8V to 3.3V). Fig. 10 depicts the time waveforms for the output voltage and inductor's current as well as the state-plane for better visualization of the trajectories along the recovery phase. It can be seen that the current is well confined within the hysteresis margins during the convergence. It can also be seen that resumption to steady-state is obtained smoothly without additional oscillations due to the correct estimation of the load status (location marked on the timing diagram).

Fig. 11 shows the resultant recovery pattern for a 3.5A to 0.8A unloading transient, while the converter operates in enhanced-buck mode (3.8V to 3.3V). Here, fast convergence is assured by employing conventional time-optimal recovery pattern. Fig. 11 depicts the time waveforms for the output voltage and inductor's current as well as the state-plane representation.

The case of consecutive loading events of different magnitudes for a step-down mode of operation is shown in Fig. 12. The consecutive transients result in different output voltage deviations but converge to steady-state based on the load estimation process (described in IV). The reference inductor current is updated after the estimation procedure is complete which results in a recovery pattern without any current overshoot and seamless transition between the transient and the steady-state controller.

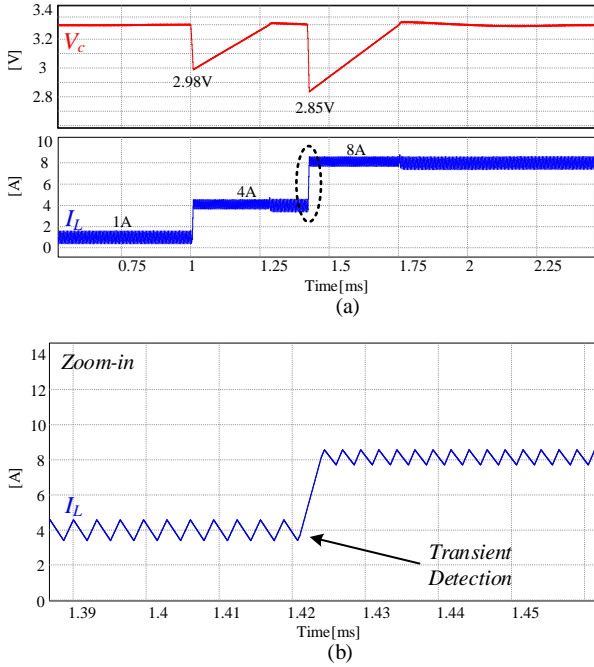


Fig. 12. Current-constrained controller response to a 1-4-8 A consecutive loading transients (a) Output voltage (top) and inductor current (bottom). (b) Zoom-in on the inductor current.

Comparison between linear and non-linear control schemes for load transients has been presented in preliminary studies. For example, in [15] where the response of multiple non-linear controller types was compared with a CPM controller with in-depth comparison of the transient recovery characteristic (i.e. output voltage deviation, transient duration, etc.)

### B. Stability Analysis

The hybrid controller in this work combines large-signal and small-signal controllers. The condition for stability in such a hybrid controller is that the large-signal controller will move the converter's state to the desired steady-state operating point, regardless of its initial conditions. Derivation of the large-signal region of convergence (ROC) is carried out in this section for the sliding-mode controller used in case of a loading event in step-down mode.

The template of the sliding-mode controller is chosen according to the converter's load-line. The load line of a NIBB converter operating in step-down configuration loaded by a resistive load (RL) can be expressed as:

$$LL_{RL}(v_C, i_L) = \left\{ v_L, i_L : i_L = \frac{v_C}{R} \right\}. \quad (11)$$

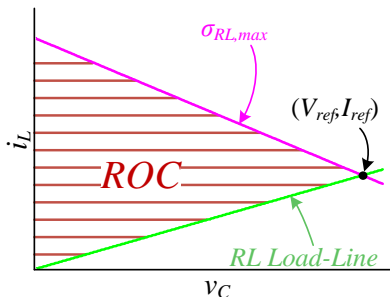


Fig. 13. Illustrative ROC for NIBB in step-down configuration loaded by a resistive load

The load-line is linear and thus a linear switching surface,  $\sigma_{RL}$ , is selected:

$$\sigma_{RL} = i_L - I_{ref} - \lambda_{RL}(v_C - V_{ref}). \quad (12)$$

The converter's average model can be expressed as:

$$\begin{cases} \frac{dv_C}{dt} = \frac{1}{RC}v_C + \frac{1}{C}i_L \\ \frac{di_L}{dt} = \frac{1}{L}V_{in}u - \frac{1}{L}v_C \end{cases}. \quad (13)$$

where  $u$  is the control input. To examine whether the trajectories along the switching surface lead to a unique steady-state operating point, current and voltage errors,  $\tilde{i}_L$  and  $\tilde{v}_C$ , are defined as follows:

$$\begin{cases} \tilde{v}_C = v_C - V_{ref} \\ \tilde{i}_L = i_L - I_{ref} \end{cases}. \quad (14)$$

Substituting (13) into (14) yields:

$$\tilde{i}_L + I_{ref} = C \frac{d(v_C + V_{ref})}{dt} + \frac{1}{R}(v_C + V_{ref}). \quad (15)$$

The expression in (15) can be separated into two parts which represent the dc component and the time-dependent component:

$$\begin{cases} i_{DC} = \frac{V_{ref}}{R} \\ i_{AC} = \tilde{i}_L = C \frac{d(\tilde{v}_C + V_{ref})}{dt} + \frac{1}{R}\tilde{v}_C \end{cases}. \quad (16)$$

If  $i_{AC} \rightarrow 0$  along the switching surface, the system is asymptotically stable and converges to the dc steady-state point. By substituting (14) and (16) into the switching surface, the following differential equation is obtained:

$$C \frac{d\tilde{v}_C}{dt} + \frac{1}{R}\tilde{v}_C - \lambda_{RL}v_C = 0. \quad (17)$$

Using (17), the stability condition of the switching surface can be obtained as:

$$\lambda_{RL} < \frac{1}{R} = \lambda_{RL,max}. \quad (18)$$

Choosing  $\lambda_{RL}$  that satisfies (18) results in assured convergence of the state variables to  $(V_{ref}, I_{ref})$ . In addition, the ROC is bounded by the load-line to guarantee that the switching surface does not pass in a rejective region [22]. The ROC can be depicted on the state-plane as shown in Fig. 13, bounded by the load-line and the curve  $\sigma_{RL,max}$ . The switching surfaces where chosen to comply with the above constraints and thus large-signal stability is assured.

Analysis for voltage step-up configurations has been studied in detail in previous studies [22]. Here, to assure convergence of the state variables  $\lambda_{RL}$  should be chosen to satisfy the following:

$$\lambda_{RL} < \frac{1}{RV_{in}} = \lambda_{RL,max}. \quad (19)$$

#### IV. PRACTICAL IMPLEMENTATION

##### A. Load Current Estimation

The implementation of the self-tuning estimator is described in Fig. 12. It is based on a look-up-table (LUT) and on estimation of the load current through a comparison with a measurement of the known current value, named unity current. The LUT of the estimator is populated during the converter start-up. Over that period, the LUT's entries are stored, i.e. current and voltage threshold values are created, from measurement of the output voltage. After the writing of the values in the tables is completed, the output voltage deviation is used as an address (input of Fig. 14) to determine the LUT's outputs, i.e.,  $V_{th}$  and  $I_{th}$  values. Upon the converter power up a generic LUT is assigned. The known current of the protective resistor  $R_{bld}$  (also known as bleeding resistor), named unit current  $I_{unit}$ , is used for the system calibration. Such bleed resistance is often utilized in many practical cases as a protection from over-voltage at the output, in particular at light-load and DCM operation. During this time, the load is disconnected from the output of the converter, i.e., switch  $M_{out}$  is turned off, and in addition, switches  $Q_1, Q_3$  are off while  $Q_2, Q_4$  are on. This assures that the current path to  $R_{bld}$  is via the output capacitor alone. The value  $\Delta V_1$  is a function of  $I_{unit}$  and is measured as:

$$\Delta V_1 = v_{ADC}[n] - v_{ADC}[n-1] = \frac{V_{ref}}{R_{bld}} \frac{\Delta t}{C} = I_{unit} \frac{\Delta t}{C}, \quad (20)$$

where  $\Delta t$  is short sampling interval,  $v_{ADC}[n]$  is the current value of the ADC output and  $v_{ADC}[n-1]$  is the ADC value from the previous sampling cycle.  $\Delta t$  is chosen according to the specifications of the ADC as well as the transistors and drivers used in the power-stage. The maximum sampling frequency that ensures proper mitigation of the power switches is used to achieve short sampling period in order to sample the output voltage while the capacitor voltage decreases linearly. The value  $\Delta V_1$  is used to populate the LUT with  $I_{th}$  and  $V_{th}$  values for the full range of allowable output voltage deviations.

Upon power up of the converter and population of the LUT is completed, the switch  $M_{out}$ , usually existing in the applications of interest is turned on. During the remaining portion of the converter operation, the LUT is used to produce  $I_{th}$  and  $V_{th}$  during transient events. The input to the LUT is now the voltage deviation  $\Delta V_2$  measured during the on time of  $Q_1$  and  $Q_4$ . During a transient event, the load current  $I_{out\_new}$  is estimated as:

$$I_{out\_new} = \frac{\Delta V_2}{\Delta V_1} I_{unit}. \quad (21)$$

The inductor current reference assigned by the DAC is a function of the load estimation result and the operating mode

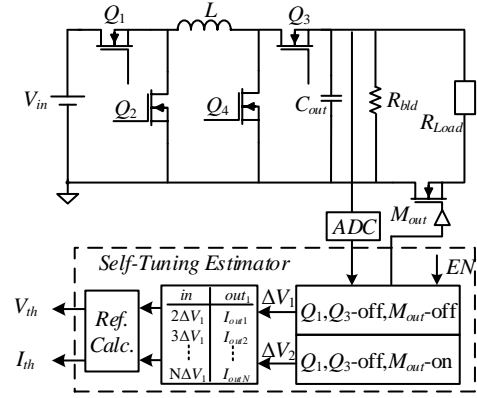


Fig. 14. Block diagram of the self-tuning estimator.

of the NIBB, i.e. step-up or step-down. In direct energy transfer configuration, the average output current is equal to the average inductor current. Therefore, the new steady-state average current can be expressed as follows:

$$I_{th} = I_{out\_new} \quad (22)$$

However, for indirect energy transfer the average inductor current is higher than the load current by factor of the duty ratio. For example, in a boost configuration, the new inductor current setting will be:

$$I_{th} = I_{out\_new} \frac{1}{1-D_{boost}}, D_{boost} = \frac{V_{out} - V_{in}}{V_{out}}. \quad (23)$$

It should be noted that in case the load estimation procedure produces a result that differs from the actual current drawn by the load, the hybrid-controller will still converge to the new steady-state with zero DC error while keeping most of its dynamic capabilities. The estimated load current is used to bring the system variables around the new operating point where the linear controller takes control and achieves zero steady-state error based on samples of the output voltage, as illustrated in Fig. 1. The load estimation procedure in this study may be somewhat complex for some applications, therefore a different realization described in [24] can be utilized.

#### V. EXPERIMENTAL VERIFICATION

In order to validate the operation of the unified current-programmed digital controller, a 2-15V to 3.3V non-inverting buck-boost prototype has been built and tested, using an 8.2 $\mu$ H inductor, 30 $\mu$ F output capacitance and operating frequency of 100-200 KHz. The experimental setup is shown in Fig. 15. The CPM controller dictates the resolution of the ADC and DAC which also satisfy the requirements of the non-linear controller. The resolution of the ADC is 32mv with maximum conversion rate of 20MHz. The resolution of the DAC is 2.5mV with maximum conversion rate of 20.4MHz. The converter is digitally controlled by a steady-state voltage-mode compensator and a transient-mode controller as shown in Fig 1. The digital controller has been entirely realized on Altera Cyclone IV FPGA, and the total number of logic elements used is 980 for the entire controller.

Steady-state operation has been verified through multiple experiments under various input voltages, as shown in Fig. 16- Fig. 18. Fig. 16a and Fig. 16b show the inductor's current in enhanced-boost mode for  $V_{in}=2.8V$  and  $V_{in}=3.2V$ , respectively.

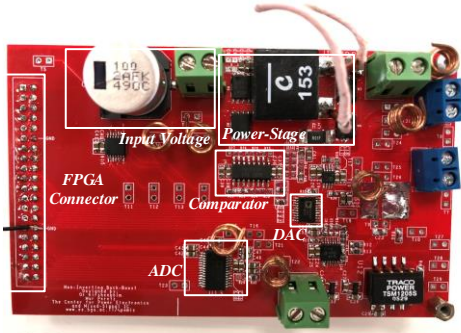


Fig. 15. Experimental prototype of the NIBB converter.

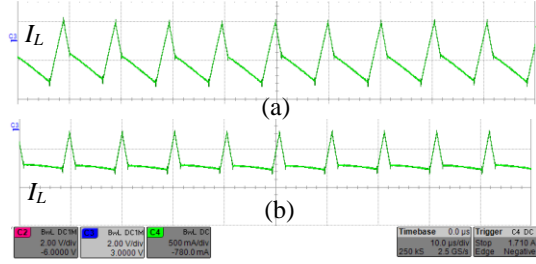


Fig. 16. Enhanced-boost mode,  $V_{out}=3.3V$  (a)  $V_{in}=2.8V$  (b)  $V_{in}=3.2V$ .

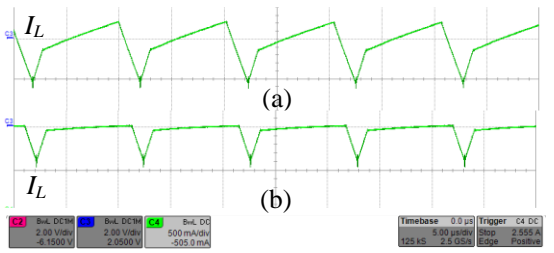


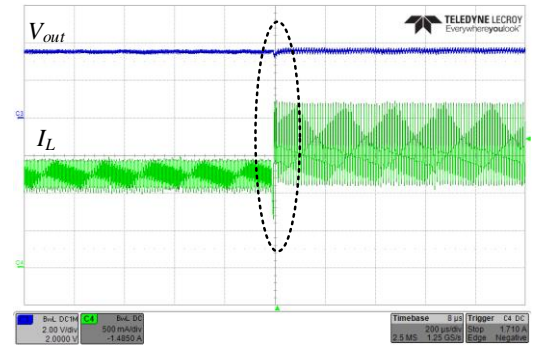
Fig. 17. Enhanced-buck mode,  $V_{out}=3.3V$ . (a)  $V_{in}=3.8V$ (b)  $V_{in}=3.4$ .

Regulated output voltage is achieved for a wide range of input voltages while significantly reducing average inductor current and rms values. Fig. 17a and Fig. 17b depict the operation in enhanced-buck mode for  $V_{in}=3.8V$  and  $V_{in}=3.4V$ , respectively.

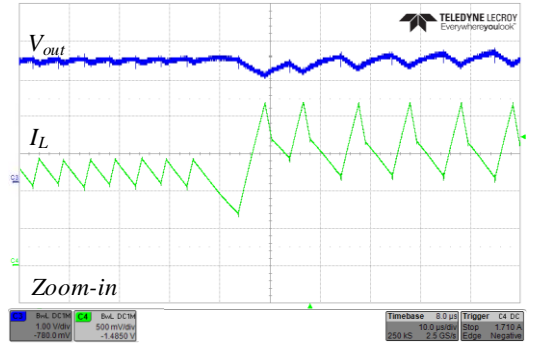
Fig. 18 shows a transition mode between conventional boost to enhanced-boost. It can be seen that, seamless transition between the two operating modes is achieved as in all other mode transition cases. A zoomed-in view of the inductor current and output voltage is shown in Fig. 18b demonstrating frequency scaling operation.

The transient controller performance for loading transient of 0.8-3.5A is depicted in Fig. 19-20. Fig. 19 shows the loading transient recovery of the current-constrained controller while in enhanced-buck mode.  $I_{th}$  is chosen to be equal to the new steady-state peak inductor current which results in an output voltage deviation of 1V and total transient time of  $60\mu s$  with no current overshoot. Fig. 20 shows loading transient recovery of the voltage-deviation-and-current-constrained controller while operating in pure-boost mode. The resultant recovery parameters are output voltage deviation of 1V, no current overshoot, recovery time to steady-state is  $50\mu s$ .

Load transient recovery of conventional buck or boost setups, where the input voltage is relatively far for the target output voltage, has been studied in-depth in previous studies. For example, in [25] where detailed comparison between linear



(a)



(b)

Fig. 18. Transition event from conventional boost to enhanced-boost operating mode,  $V_{in}=3V$ ,  $V_{out}=3.3V$ . (a) Transition event. Output voltage (top-blue) 2V/div, inductor current (bottom-green) 500mA/div, time scale  $200\mu s$ /div. (b) Zoom-in on the transition, Output voltage (top-blue) 1V/div, inductor current (bottom-green) 500mA/div, time scale  $10\mu s$ /div.

and non-linear controllers for a step-down configuration was presented. For the case of a boost configuration, a state-plane-based transient-mode control scheme has been presented in [15].

## VI. CONCLUSION

A unified current programmed digital controller for NIBB converter have been presented in this study. The controller incorporate a steady-state CPM controller for steady-state operation and a nonlinear transient-mode controller for load transients. Detailed analysis of the enhanced-modes has been carried out, followed by steady-state control scheme design to allow seamless transition between modes and improved ripple characteristics. Load transients are supported by the same hardware of the CPM controller, with programmable constraints of the output voltage deviation and inductor current. An optimized boundary control scheme for efficient load transient convergence has been perused with assured large-signal stability.

Experimental results of a 2-15V to 3.3V NIBB converter prototype are provided. For steady-state operation around unity conversation, well regulated output voltage is achieved with significantly reduced average inductor current and rms values. The controller exploits the versatile structure of the NIBB to maintain short transient time without the penalty of increased current or voltage overshoots.

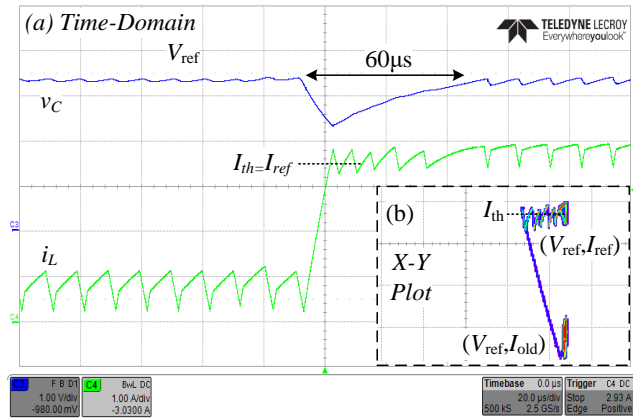


Fig. 19. NIBB converter's response and state-plane representation to a 0.8-3.5 A loading transient using the current-constrained controller. (a) Output voltage (top-blue) 1V/div, inductor current (bottom-green) 1A/div, time scale 20µs/div. (b) State-plane representation of inductor current (vertical axis - 1 A/div) and output voltage (horizontal axis - 1 V/div).

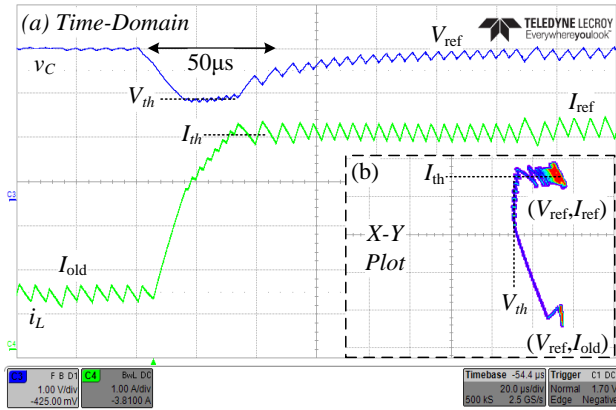


Fig. 20. NIBB converter's response and state plane representation to a 0.8-3.5 A loading transient using the voltage-deviation and current-constrained controller. (a) Output voltage (top-blue) 1V/div, inductor current (bottom-green) 1A/div, time scale 20µs/div. (b) State-plane representation of the inductor current (vertical axis - 1A/div) and output voltage (horizontal axis - 1A/div).

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