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Multi-Loop Control for Power Transfer Regulation in Capacitive Wireless Systems by Means of Variable Matching Networks

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***Abstract* — This paper introduces an adaptive multi-loop controller for capacitive wireless power transfer (WPT) systems. The new control approach combines continuous frequency tracking and matching networks tuning on both the primary and secondary to regulate a target current/power to the receiving side at the optimal power transfer conditions. This enables to effectively disengage the power delivery capabilities from the cross-coupling interactions between the transmitting and receiving sides, and to compensate for variations of the electrical circuits and capacitive medium. This paper highlights the complex functional relationships of the multi mixed-signal controller, and provides theoretical as well as practical insights on the dynamics and implementation of a closed-loop capacitive power transfer (CPT) system. The core of the multi-loop controller has been implemented through a digital orientation on an HDL platform. The effectiveness of the new controller is demonstrated on an experimental prototype of a resonant double-sided *LC* capacitive WPT that has been designed and implemented to operate in the MHz range. Experimental closed-loop operation is well demonstrated under various loads and medium conditions up to 200 mm air-gap, validating self-tuned CPT system. Furthermore, the capacitive interface has been methodically examined through Maxwell's Finite Elements Analysis (FEA) tools for different structures, distances and alignments. The results of the FEA have been utilized to enhance the accuracy of the experiments, accounting for the variable coupling capacitance under variations.**

***Index Terms* — capacitive power transfer, capacitive coupling, multi-loop controller, multi-mixed-signal control, closed-loop capacitive wireless system, impedance matching, variable inductance, adaptive matching networks, self-tuned system, wireless power transfer.**

I. Introduction

With the growing demand for increased computing power to support technology ramp-up, mobile power is essential to keep high-performance devices available for extended periods, ideally continuously [1]-[6]. Wireless power transfer (WPT) technology is a well growing approach to provide energy at all times, and to reduce dependency of weight and volume-sensitive mobile and portable applications in bulky batteries as a reliable main source of energy [7]-[9]. Capacitive power transfer (CPT) approach has been investigated in recent years, as an alternative near-field power transfer method to well know magnetic field-based approaches. One of the more attractive advantages of capacitive-based WPT is the avoidance of undesired Eddy currents and electromagnetic interfaces (EMI) that comes with magnetic based WPT methods [1], [9], [10]. In addition to efficiency improvements, CPT systems are potentially with lower volume and construction complexity [10]-[15].

A main challenge of general near-field WPT systems, and in capacitive approach in particular is that the power transfer capability and efficiency depend on the distance and alignment between the transmitting and receiving sides [14]-[16]. In addition, the coupling coefficient of the transfer medium and load conditions are sensitive to changes in the environment, component aging and temperature drifts, which dramatically decrease the power transfer capabilities of the system. Reducing the sensitivity of the WPT system to variations can be alleviated by designing matching networks that provide loose coupling between the transmitting and receiving sides [11]-[13], [15]. In this solution however, the system characteristics still strongly depend of the component values and the precision of the operating frequency. To fully disengage the system's characteristics from any drifts, changes and variations, a closed-loop active compensation is essential.

Several methods to reduce the effects of components and medium variations of WPT systems have been proposed for general power transfer, which can also be adapted to CPT [16]-[22] such as: frequency tuning, compensation networks impedance matching, and post regulation DC-DC conversion. In frequency tuning approach, the operating frequency is adjusted to track the resonant frequency. This results in optimal operating conditions [21], [23], [24], however, since the allowed frequency range for energy transfer is quite narrow, for example at 6.78 MHz operation the frequency band is ±15 kHz [25]. Thus, for distance, misalignment and load variations this solution alone does not accommodate for power transfer regulation. In [24], utilization of frequency adjustment in capacitive WPT to account for changes of the capacitive medium capacitance has been discussed. There, the resulting range compensation is quite narrow and requires relatively wide frequency range. This poses a limitation on the design of the system hardware in terms of the magnetics and other components which translates into rather bulky system overall. In impedance matching methods, the resonant inductor and

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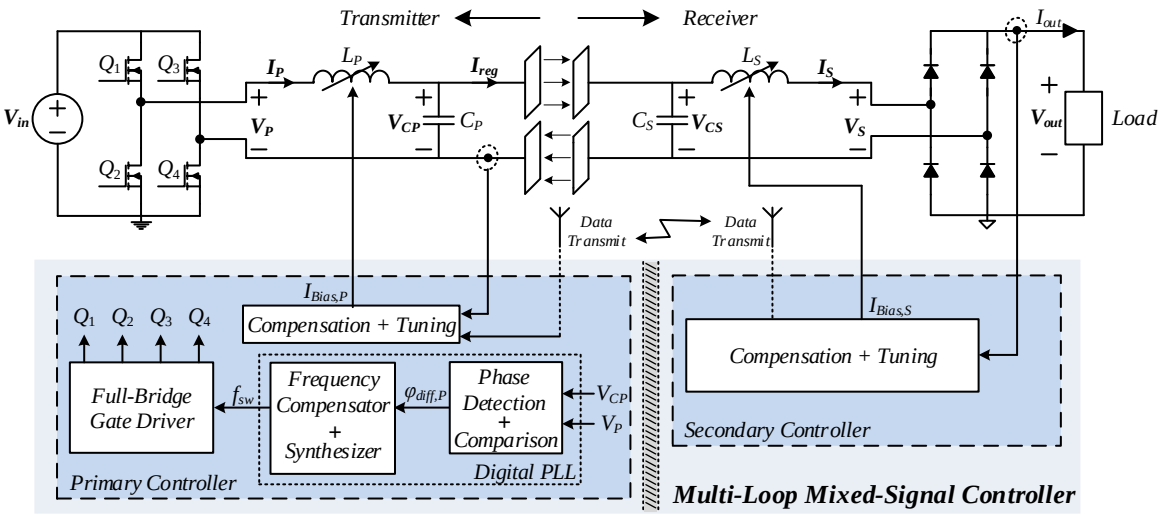

Fig. 1. Simplified schematic diagram of a double-sided *LC* capacitive WPT system with an adaptive multi-loop controller.

capacitor can be adjusted at a fixed frequency [26], [27]. Thus, the output voltage/current can be regulated by actively adjusting the matching network impedance [19], [28], [29]. The latter provides flexibility for regulation the transferred power to the load, but comes at the cost of potential additional control circuitry and potential degradation of the overall efficiency [29], [30]. It should be noted that although existing closed-loop methods enable to overcome some system variations and to extend the power delivery range (power levels and distance), a single control method is not sufficient to guarantee reliable operation of WPT systems. On the topic of magnetic field based WPT and in particular magnetic resonance, combined control methods have been investigated [1], [17], [31], however, a closed-form control mechanism for CPT has not been addressed hitherto. It would be extremely beneficial if a *multi-loop controller for capacitive-based WPT systems that compensates for the variations of multiple cross-coupling interactions between the transmitting and receiving sides, electrical circuits and medium characteristics* is utilized – this has been pursued in this study.

The objective of this study is therefore to introduce an adaptive multi-loop controller for CPT technology, which compensates on-the-fly for variations of source and the load circuits, coupling interface (distance and/or alignment) and matching networks as detailed in Fig. 1. The new control approach effectively disengages the power delivery capabilities from drifts or variations, which enables spatial freedom of the transferred energy to the receiving side. It relies on continuous tuning of the operating frequency to the resonant one, and adjusts both the transmitter's and receiver's matching networks such that the best power transfer conditions are obtained for any given combination of distance, displacement misalignment or component values. It is a further objective of this study to present a tuned network realization that is based on a variable inductor, i.e. it is not based on relays or semiconductor switches, and therefore enables continuous self-tuned impedance matching.

The rest of the paper is organized as follows: Following a brief survey of *LC*-based capacitive WPT system, Section II describes the principle of operation of the multi-loop controller and details its algorithm. The control architecture and functional analytical relationships are delineated in Section III, and detailed dynamic analysis for the primary building blocks of the multi-mixed-signal system is delineated. Section IV provides details regarding the practical implementation of the self-tuning system with emphasis on the challenges of sensors realization. Experimental verification of a CPT prototype with the adaptive multi-loop controller is provided in Section V. Section VI concludes the paper.

II. Closed-Loop Tuning of a Capacitive WPT System

The principle of operation of the adaptive multi-loop controller is described here through a resonant double-sided *LC* matching network [13], [15], as delineated in Fig. 1. It should be emphasized, however, that the core of the control algorithm is applicable for any CPT system, and with minor modifications to any resonant-based WPT method. To establish definitions that are used throughout the paper and to simplify some of the topology intricate features (e.g. dynamic behavior), the following subsection briefly reviews the double-sided *LC* resonant converter configuration.

A. Double-Sided LC Matching Network

The equivalent electrical representation of the capacitive-based medium is shown in Fig. 2. There, C_M is the equivalent mutual coupling capacitance, C_{M1} and C_{M2} are the self-capacitances of the coupling plates [12], [15], [32], [33]. The system is driven by a full-bridge inverter on the primary side, and the load is fed via a diode rectifier that is connected to the secondary's network. Provided that the self-capacitances and the mutual coupling capacitance C_M are lower than the total parallel matching capacitances C_P and C_S [12], [15], and that the drive frequency, f_{sw}, is near the matching networks' resonant frequency (i.e., $f_0 = 1/(2\pi) = 1/(2\pi)$, then the currents as well as voltages of the reactive elements are virtually sinusoidal [34]-[36]. This is since high-Q operation is naturally facilitated as the output impedance of the network in the primary side is relatively high. In [15], [37], [38], it has been established that when resonant operation is satisfied, the primary current, I_P, depends on the output voltage, and the secondary current, I_S, depends on the input voltage, and thus with the aid of system parameters the currents can be expressed as

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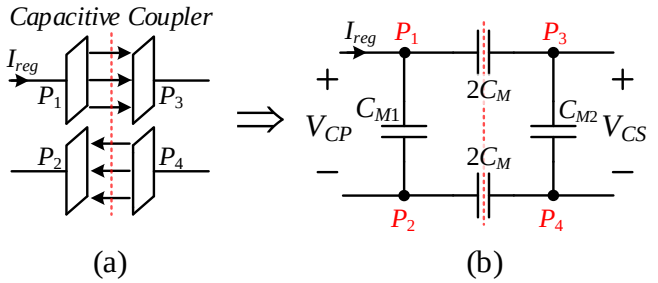

Fig. 2. Capacitive medium: (a) Simplified mechanical illustration, (b) Equivalent capacitance lumped model.

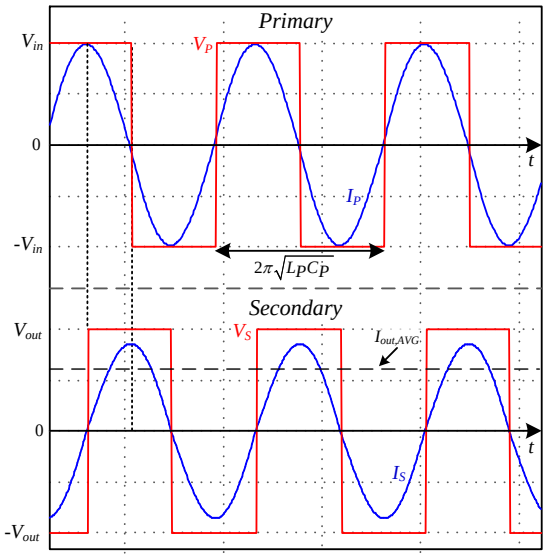

Fig. 3. Typical currents and voltages waveforms of a *LC* capacitive WPT configuration: upper signals - primary, bottom signals - secondary.

$$I_P = \underbrace{\frac{\omega_0 C_P C_S}{C_M}}_{G} V_S \quad ; \quad I_S = \underbrace{\frac{\omega_0 C_P C_S}{C_M}}_{G} V_P , \tag{1}$$

where ω_0 is the angular resonant frequency, V_P and V_S are the voltages of the primary and secondary, respectively. Typical waveforms of this CPT system are shown in Fig. 3. As described, while the primary and secondary voltages V_P and V_S are square waves, the currents are sinusoidal due to high-Q operation of the circuit. Since a full-bridge inverter is used at the front-end, the primary voltage V_P toggles between V_{in} to -V_{in}. It can be also seen, that for both the primary and secondary sides the current is in phase with the voltage, whereas the secondary voltage V_S lags the primary voltage V_P by 90º.

From (1), it can be seen that the double-sided *LC* CPT system can be described by a two-port network with gyrator characteristics [39], with a trans-conductance gain *G*. This implies that the dynamic behavior for the output side of the system can be characterized as a voltage-dependent current source, I_{out}, which represents the rectified current of I_S as illustrated as illustrated in Fig. 4. It should be noted that a detailed derivation of the network relationship of the circuit as well as the existence criteria of gyrator conversion have been thoroughly described and can be found in [37], [38]. Therefore, only the essential in-context details have been brought up here in order to establish the foundations for power regulation control.

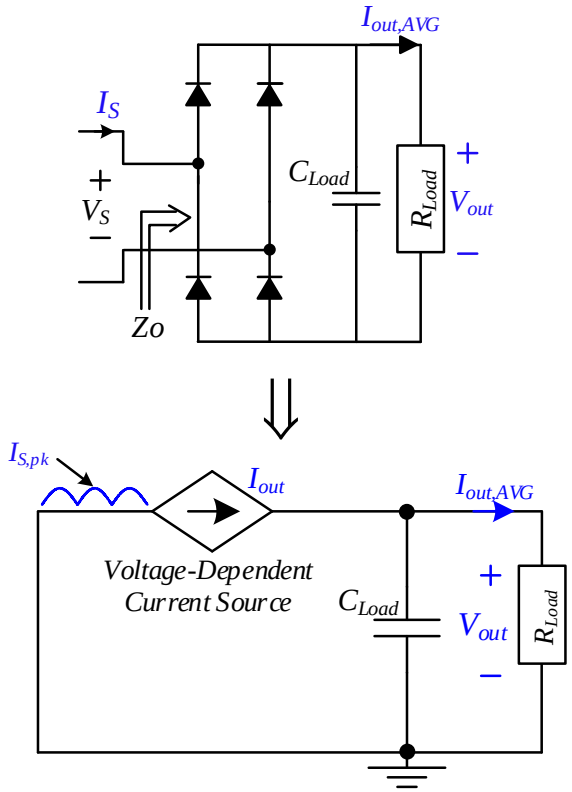

Fig. 4. Simplified behavioral model for the output side of the CPT system.

Employing fundamental harmonics approximation method [36] on (1), the average value of the output current I_{out} is expressed as a function of the input voltage V_{in} as follows

$$I_{out,AVG} = \frac{8}{\pi^2} \frac{\omega_0 C_P C_S}{C_M} V_{in} , \tag{2}$$

thus, the average output power P_{out} can be expressed as

$$P_{out} = \left(\frac{8}{\pi^2} \frac{\omega_0 C_P C_S}{C_M} V_{in} \right)^2 R_{Load} . \tag{3}$$

B. Controller Operation

Following the analysis and observations made in the previous subsection, an adaptive controller that monitors, tunes, and enables to continuously deliver constant current to the receiving side is addressed. Power regulation is facilitated by three major control loops as shown in Fig. 1, with two control loops at the primary side, while a third loop is located at the secondary circuit. The control loops are distinguished by their control objectives and bandwidth requirements, such that the operating characteristics of the WPT system are satisfied. The first loop resembles in structure to a digital phase-locked loop (DPLL) that synthesizes a switching frequency, f_{sw}, which continuously follows the resonant frequency, f_0, even under variations of the system parameters. This self-driving concept ensures in this *LC* configuration, that the power conversion characteristics of the matching networks are optimized. Compensating for changes in the coupling medium requires variation of the drive frequency off the specific optimized point and correcting the network parameters accordingly. This can be achieved by adjusting network's inductor, capacitor or both. In this study an approach based on variable inductor is employed. The second control

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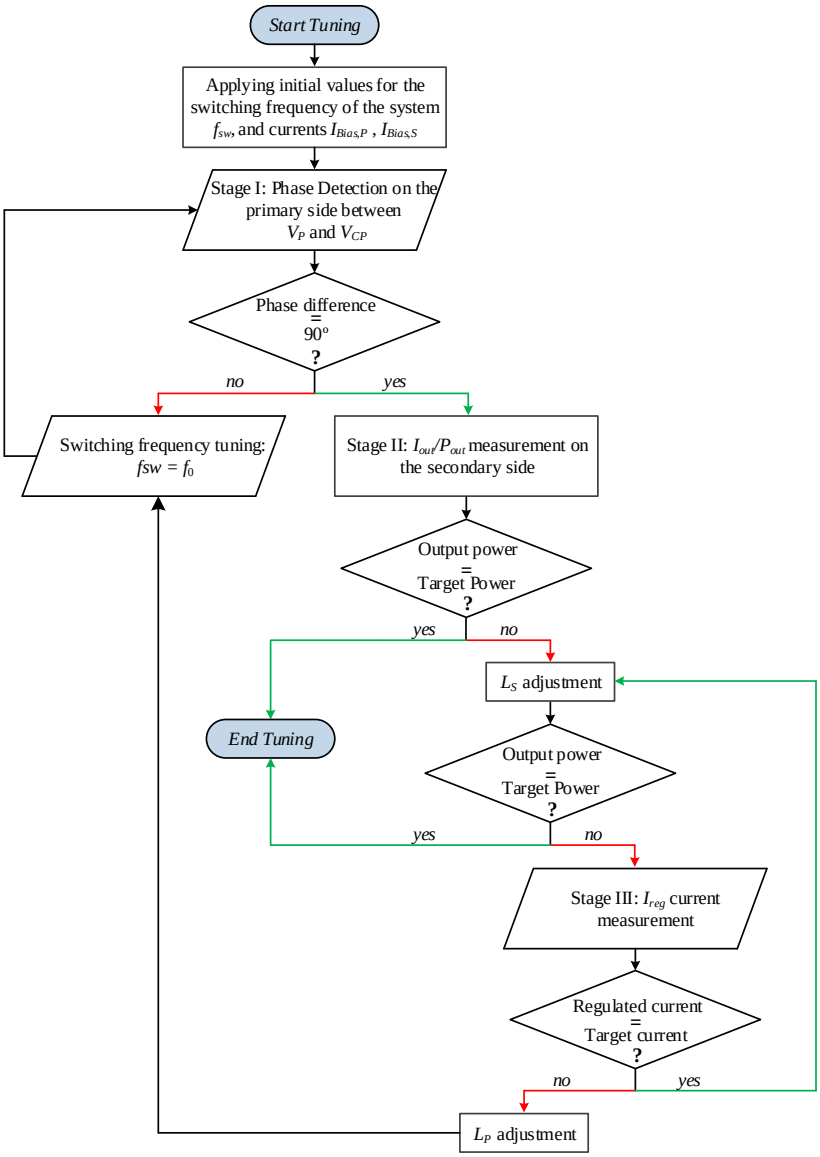

Fig. 5. Flowchart of the controller's tuning procedure.

loop comprises a current compensator and a tuning unit (current driver, as will be detailed later), that adjusts the inductance value of L_P such that a constant current is regulated to the capacitive plates. This transforms the primary circuit into a self-tuned architecture, in which the drive frequency tracks the resonant frequency on-the-fly, and the transmitted power is regulated by the resonant network's characteristics. A third compensation loop, located in the receiver side, comprises a tuning unit that adjusts the inductance value of the secondary side inductance, L_S, according to the desired output current (as well as power). It should be emphasized that, in general, controlling only one parameter may suffice for constant power delivery for static operation, however, to achieve more spatial freedom on-the-fly even for extreme medium and load variations, all three loops are required.

A high-level view of the tuning procedure utilizes the control loops is illustrated by the flowchart in Fig. 5. Upon initiation of the tuning procedure, a default set of pre-loaded values are used to determine the switching frequency f_{sw}, and the variable inductors L_P and L_S. These values are determined by the target operating conditions of the system. The adaptive tuning operation is performed independently per feedback loop, with its respected objective and rate. The inner feedback loop applies frequency tuning. There, the switching frequency to drive the full-bridge, f_{sw}, is being varied by the DPLL unit to match the resonant frequency of the circuit f_0. This is facilitated by measuring the voltages V_P and V_{CP} (Fig. 1), extracting the phase difference between them, and adjusting f_{sw} until the phase difference between the signals reaches 90°. In the case that the detected phase difference between the signals is not 90°, an error signal is generated to the DPLL frequency synthesizer, which in turn generates new switching frequency until $f_{sw}=f_0$.

The next stage of the tuning operation is facilitated by another feedback loop located at the secondary (receiver) side. In this loop, the inductance value L_S of the secondary's matching network is adjusted according to the operating resonant frequency of the primary side to maximize the energy transfer to the load. This is done by sensing the output current and adjusting L_S according to the current relationships in (1) and (2). This variation of the inductor value is realized by a current driver that applies dc bias to non-gapped side windings of the inductor as previously described in [40], [41].

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In the third stage of the tuning operation, the plates current I_{reg} (Fig. 1) from the primary circuit is sensed and compared to a target/reference one, which is defined by the information from the receiving side. The correction signal that is generated is used to vary the inductance L_P through a bias winding until the required current is achieved. Due to the variation of the inductance value, the resonant characteristics of the system change, and potentially move the system out of its optimized transfer conditions. As a result, the frequency tracking loop needs to search again and lock the switching frequency into the resonant frequency. Therefore, to satisfy proper operation of the multiple feedbacks, and to allow each feedback loop to converge with reasonable dynamics while being virtually decoupled one from another, the compensators are designed with descending bandwidth order. Utilizing this approach, employed in many multiple loop compensation schemes, assures that the faster loop is virtually transparent to its following and by doing so, significantly simplifies the system dynamics and complexity of the compensators. As a result, the interaction, or interference, between feedbacks is alleviated. The frequency tracking loop (of the primary side), is designed to be with highest bandwidth within the controller, i.e., responds the fastest among the multiple control loops. The second responding loop is the adjustment of the secondary's matching network as it receives its signal with defined frequency of the primary. The current/power regulation loop is designed with the slowest bandwidth among the three to assure that once the energy level is set, it is with the optimized transfer conditions given the network parameters and medium settings. The analysis, derivations, and in-detail description of the multi-feedback loops are provided next.

III. Controller Architecture

Following the high-level description of the control algorithm given in the previous section, a simplified *functional diagrams* that describe the signal flow and behavior of this self-adjusted, self-tuned, system are depicted in Fig. 6. The diagrams comprise both linear and non-linear transfer functions to reflect the specific operation of each 'transformation unit' (i.e. 'block') [40]. It should be emphasized that throughout the functional derivations, small-signal transfer functions are denoted by small letters. The diagram of the control scheme of the primary circuit includes two major loops to satisfy current sourcing behavior to the transfer plates (Fig. 6a). A third, independent loop is located at the secondary side to adjust the receiving network to regulate the output current. In addition, for both the primary and secondary circuits, the bias driver of the variable inductors is designed as a closed feedback loop configuration to maintain a forced current control. This enables to reduce the order of the outer feedback loop, and therefore simpler to stabilize the overall system. By employing self-calibrating frequency loop and adjusting the system parameters, regulation of the primary's output current, I_{reg}, can be achieved at the same time that the system is kept at resonance (while soft-switching conditions are met).

A. Primary Side Control Loops

Starting from the left side of Fig. 6a, the output current is translated to a reference current level, $I_{ref,P}$, which is a proportional representation of the required regulated current from the primary to the secondary. $I_{c,P}$ represents the correction signal generated by the current compensator, and $I_{e\_Bias,P}$ is the error signal of the inner bias current loop. K_{mod} stands for the modulator's gain, i.e., bias current correction signal, $I_{c\_Bias,P}$ to duty-cycle of the bias current driver. The bias driver in this study has been realized by a buck converter, and its transfer function is represented in the block diagrams by B_P. The bias current for the inductor L_P can be expressed as

$$I_{Bias,P} = D_P B_P(s) = \frac{D_P V_{Buck}}{sL_{Bias} + R_{DCR}}, \quad (4)$$

where L_{Bias} is the inductance value of the bias winding, R_{DCR} is the dc resistance of the inductor, D_P and V_{Buck} are the duty-cycle and the input voltage of the buck converter, respectively. After linearization, the small-signal transfer function between the duty-cycle and the inductor current $b_P(s)$ is expressed as

$$b_P(s) = \frac{i_{Bias,P}(s)}{d_P} = \frac{V_{Buck}}{sL_{Bias} + R_{DCR}}, \quad (5)$$

where $i_{Bias,P}$ is the small-signal bias current and d_P is the duty-cycle perturbation. Thus, the closed-loop transfer function of the buck converter is

$$A_{CL\_Buck,P}(s) = \frac{i_{Bias,P}(s)}{i_{c,P}(s)} = \frac{G_{comp2}(s)K_{mod}b_P(s)}{1 + K_{I,Bias}G_{comp2}(s)K_{mod}b_P(s)}, \quad (6)$$

where $G_{comp2}(s)$ is the transfer function of the inner compensator and $K_{I,Bias}$ is the gain due to the bias current sensing [40], [42]. By neglecting R_{DCR} and by assuming that the compensator has been designed properly to meet both phase margin and loop gain bandwidth, (6) can be further rearranged and simplified to a first order system [40]

$$A_{CL\_Buck,P}(s) = \frac{1/K_{I,Bias}}{1 + s/\omega_{Buck,P}}; \ \omega_{Buck,P} = \frac{K_{I,Bias}K_{p2}K_{mod}}{L_{Bias}}. \quad (7)$$

where K_{p2} is the gain due to the compensator. (7) implies that for the frequency range $\omega < \omega_{Buck,P}$ the inner current feedback has transformed the bias buck converter (from error signal to bias current) from a first order system to a zero order system.

H_{LP} represents the bias winding such that the relationship between the bias current and the primary side inductance is

$$L_P = H_{LP}(I_{Bias,P}). \quad (8)$$

The relationship of $H_{LP}(I_{Bias,P})$ can be obtained by experimental measurements, advanced simulation tools such as Maxwell-Ansys, or by analytical analysis which discussed in detail in Section IV-A. Local linearization around the operating point determines the non-linear small-signal response of H_{LP} as follows

$$h_{LP} = \frac{dL_P(I_{Bias,P})}{dI_{Bias,P}} = \frac{H_{LP}(I_{Bias,P0}) - H_{LP}(I_{Bias,P0} + \Delta I_{Bias,P})}{\Delta I_{Bias,P}}, \quad (9)$$

where $I_{Bias,P0}$ is the nearest measure value of the bias current for a given operating point, and $\Delta I_{bias,P}$ is the increment between the two nearest measured values of the bias current around the operating point. Finally, K_f is the response of the matching network combined with power-stage to the variable inductor generated by H_{LP} (the ratio of the regulated current I_{reg} to a change of the resonant characteristics).

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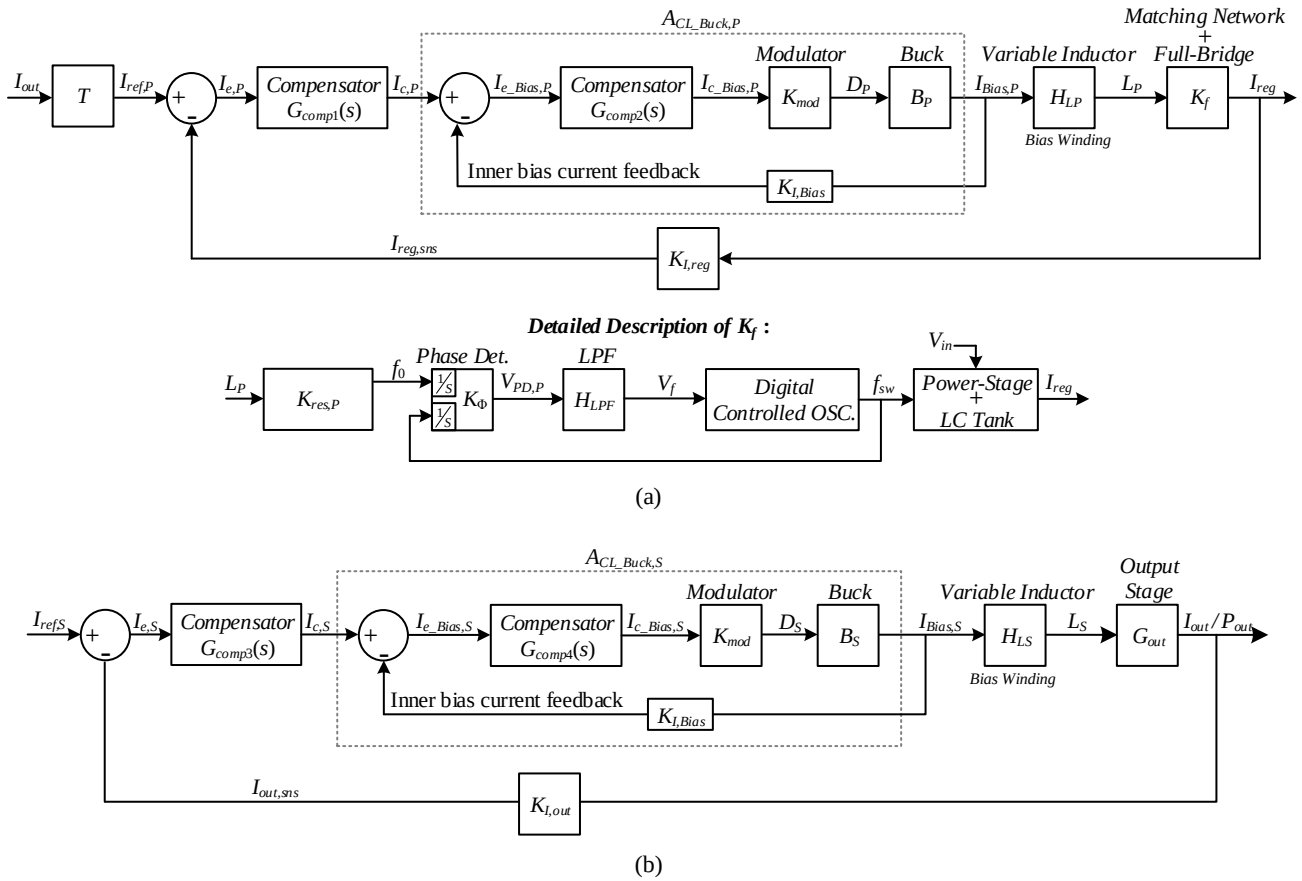

Fig. 6. Simplified functional signal flow diagrams of the multi-feedback controller: (a) Primary side control loops, (b) Secondary side control loops.

The bottom block diagram in Fig. 6a details the transfer characteristics of K_f. The output of H_{LP} dictates the resonant frequency f_0 of the CPT system such that

$$K_{res,P}(L_P) = f_0 = \frac{1}{2\pi\sqrt{\underbrace{H_{LP}(I_{Bias,P})}_{L_P} C_P}}. \quad (10)$$

Considering $H_{LP}(I_{Bias})$ as constant, due to relatively slow correction speed of the inductance value, the derivative of the large-signal $K_{res,P}(L_P)$ around the operating point yields the small-signal transfer function of the resonant tank [40]:

$$k_{res,P} = \left.\frac{df_0}{dL_P}\right|_{L_P(I_{Bias,P0})} = -\frac{1}{2L_{P0}} f_0, \quad (11)$$

where L_{P0} is the primary's resonant inductor value around the operating point.

Assuming that the frequency tuning is the fastest control loop within the system (as prescribed by the loop settings earlier), then f_0 is continuously compared to the switching frequency f_{sw} of the full-bridge to guarantee that $f_{sw}=f_0$. K_Φ represents the gain of the phase detector, consequently, the phase detector can be described as a module that includes two integrators at the input that translates frequencies into phases and a gain block. The outcome of the phase detection operation, $V_{PD,P}$, can be expressed as

$$V_{PD,P} = K_\Phi \varphi_{diff,P} = \frac{V_{DD}}{\pi}\varphi_{diff,P}, \quad (12)$$

where V_{DD} is the supply voltage of the phase detector, and $\varphi_{diff,P}$ is the phase difference between the target resonant frequency and the drive switching frequency signals (which is obtained by the signals V_P and V_{CP} as discussed in Section II-B). $V_{PD,P}$ which represents a proportional phase mismatch between the inputs of the phase detector for every switching cycle of the system is filtered by a lag-lead low-pass filter (LPF) network that is represented in the continuous domain as

$$H_{LPF}(s) = \frac{1+sCR_2}{1+sC(R_1+R_2)}, \quad (13)$$

which simplifies the stability of DPLL [43].

The voltage V_f is translated by a digitally controlled oscillator (DCO) unit to a drive frequency for the power-stage combined with the LC tank, which in turn generates the required I_{reg}. Taking into account the gyrator transfer characteristics of the system as discussed in Section II-A, and after some manipulations the regulated current to the capacitive coupler can be expressed as follows

$$I_{reg} = 2\pi f_0 C_P V_P. \quad (14)$$

Finally, the transfer function of the outer regulated current loop can be expressed as

$$A_{CL\_P}(s) = \frac{i_{reg}(s)}{i_{ref,P}(s)} = \frac{G_{comp1}(s)A_{CL\_Buck,P}(s)h_{LP}K_f}{1+K_{I,reg}G_{comp1}(s)A_{CL\_Buck,P}(s)h_{LP}K_f}, \quad (15)$$

where $G_{comp1}(s)$ is the transfer function of the outer compensator and $K_{I,reg}$ is the gain due to the regulated current sensing [42]. Under the bandwidth settings of the feedback loops as

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prescribed earlier, where the inner frequency-tuning loop has sufficiently faster response compared to the outer current regulation loop, i.e., L_P is continuously adjusted under resonant conditions of the network, then the closed-loop transfer function of (15) can be simplified to a first-order system and can be expressed as

$$A_{CL\_P}(s) = \frac{\frac{1}{s}K_{P1}A_{CL\_Buck,P}(s)h_{LP}K_f}{1+\frac{1}{s}K_{I,reg}K_{P1}A_{CL\_Buck,P(s)}h_{LP}K_f} = \frac{\frac{1}{K_{I,reg}}}{1+\frac{s}{\omega_{CL\_P}}}, \quad (16)$$
$$\omega_{CL\_P} = K_{I,reg}K_{P1}A_{CL\_Buck,P}(s)h_{LP}K_f$$

where K_{P1} is the gain due to the outer compensator and ω_{CL_P} determines the bandwidth of the outer current loop.

B. Primary Side Control Loops

Fig. 6b depicts the functional block diagram of the secondary's control loops. There, similar to the relationships carried out earlier for the primary side, the closed-loop transfer function of the secondary's bias driver, $A_{CL\_S}(s)$, is expressed as

$$A_{CL\_Buck,S}(s) = \frac{i_{Bias,S}(s)}{i_{c,S}(s)} = \frac{\frac{1}{K_{I,Bias}}}{1+\frac{s}{\omega_{Buck,S}}}, \quad (17)$$
$$\omega_{Buck,S} = \frac{K_{I,Bias}K_{p4}K_{mod}}{L_{Bias}}$$

where K_{p4} is the gain due to the secondary's inner bias current loop compensator. As mentioned earlier, utilizing current-mode control for the bias driver, within the specified current regulator bandwidth $\omega<\omega_{Buck,S}$ the bias current loop dynamics are considered as pure gain. Thus, the overall transfer function of the output current can be expressed as

$$A_{CL\_S}(s) = \frac{i_{out}(s)}{i_{ref,S}(s)} = \frac{G_{comp3}(s)A_{CL\_Buck,S}(s)h_{LS}G_{out}}{1+K_{I,out}G_{comp3}(s)A_{CL\_Buck,S}(s)h_{LS}G_{out}}, \quad (18)$$

where $G_{comp3}(s)$ is the transfer function of the outer compensator, $K_{I,out}$ is the gain due to the current sensing and G_{out} is the gain of the output stage. Assuming L_S is continuously adjusted to satisfy the required loading conditions of the output, the closed-loop transfer function of (18) can be simplified to a first-order system and can be expressed as

$$A_{CL\_S}(s) = \frac{\frac{1}{s}K_{P3}A_{CL\_Buck,S}(s)h_{LS}G_{out}}{1+\frac{1}{s}K_{I,out}K_{P3}A_{CL\_Buck,S(s)}h_{LS}G_{out}} = \frac{\frac{1}{K_{I,out}}}{1+\frac{s}{\omega_{CL\_S}}}, \quad (19)$$
$$\omega_{CL\_S} = K_{I,out}K_{P3}A_{CL\_Buck,S(s)}h_{LS}G_{out}$$

where K_{P3} is the gain due to the outer compensator and ω_{CL_S} determines the bandwidth of the output current loop. From the analyses for the secondary controller, it can be seen that the control architecture for the primary and secondary is practically the same with different control objectives. Once satisfied, this implies that the transmitting and receiving sides are tuned to satisfy the required loading conditions, and the system operates under optimal power transfer conditions since resonant power transfer is inherently imposed through the self-tuning procedure.

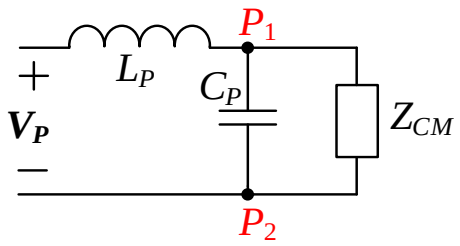

Fig. 7. Simplified equivalent circuit for the primary side.

C. System Bandwidth Selection

To assure reasonable dynamics of the multiple feedback loops, and to assure sufficient decoupling of the multiple feedback loops as well as steady-state convergence per medium settings, the system's bandwidths are assigned with respect to the transmitter's quality factor, Q, (receiver assumed of similar order), and the target operating frequency, f_{sw}, of the system. It should be noted that in systems, as double-sided LC with capacitive coupling, the response rate to changes in the control (drive frequency) signal might be rather slow, in the order of tens or hundreds switching cycles. This is since the quality factors are typically very high because of the somewhat open-circuit parallel loading of the networks (the plates terminals), as depicted in Fig. 7. The quality factor of the LC-based transmitter is a factor of the operating frequency as well as the resonant components and can be estimated as

$$Q = \frac{Z_{CM}(f_{sw})}{Z_R(f_{sw})}, \quad (20)$$

where Z_{CM} represents the reflected equivalent impedance to the primary side, which primarily determined by the coupler, and Z_R is the impedance of the resonator.

The natural slow response of the network should be taken into consideration in the selection of the system bandwidth and overall response rate. Fortunately, the objective of the control is to maintain a regulated current/power under variations of the capacitive coupling or other components drifts, which are the result of either mechanical movements or changes in environmental conditions that typically vary slowly.

The selection reasoning is as follows; the loop of the fastest bandwidth of the three loops is the DPLL, denoted by BW_1. There, for a given quality factor Q of the resonant networks, and assuming that f_{sw} is locked on f_0. Then $BW_1$is determined as follows

$$BW_1 = \frac{f_{sw}}{2Q}. \quad (21)$$

This is set so that the loop has relatively wide bandwidth, but is with the capability of the resonant network response rate. The secondary's control loop is also a relatively wide bandwidth loop and is set as a fraction of BW_1, typically a good practice is one-third (1/3) to one-tenth (1/10). This is done to assure that the secondary current regulation is carried out on a stable signal, arriving from the primary side. The third, plates current loop, is set to be with slower response, typically one-ninth (1/9) to one-fiftieth (1/50) of the switching frequency of the system. By doing so, the loops are virtually decoupled and the tuning process does not depend on preceding information or data of the system to facilitate closed-loop operation.

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IV. Practical Implementation

A. Variable Inductor

The implementation of variable inductor as employed in this study is shown in Fig. 8a. It is inspired by the prior art of [40], [44], [41]. The structure comprises an *E*-core type magnetic element with the primary inductor constructed on the middle, gapped leg, whereas the bias/control windings are formed on the outer, non-gaped legs, and connected in series but with opposite polarity. By doing so, the ac coupling between the center leg to the bias winding is cancelled while dc current through the auxiliary winding partially saturates this portion of the core, resulting in variable inductance, as illustrated by Fig. 8b.

The inductance value L can be estimated with the aid several design parameters such as: number of turns n, air-gap length l_g, and the effective magnetic path length l_e. Hence, the inductance L as a function of the bias current-dependent permeability can be expressed as [45]

$$L = \frac{n^2 \mu_0 A_e}{l_e} \frac{\mu_r(I_{Bias})}{1 + 2\frac{l_g}{l_e}\mu_r(I_{Bias})}, \tag{22}$$

where μ_0 is the air permeability, μ_r is the magnetic core permeability, and A_e is the core area. μ_r depends on the bias current I_{Bias} and can be obtained from either the manufacturer data or by experiment [45], [46]. A simplified expression of μ_r is given by

$$\mu_r(I_{Bias}) = \frac{\mu_{mi}}{1 + \left(H(I_{Bias}) / H_{\text{pole}}\right)^j}, \tag{23}$$

where μ_{mi} is the permeability initial value, i.e., $\mu_{mi} = \mu_r(H = 0)$, H_{pole} is the magnitude of the saturation field and j sets the permeability slope. The variable H represents magnetic field strength, which is linearly proportional to the bias current. The relationship between H and I_{Bias} is as follows

$$H(I_{Bias}) = nI_{Bias} / l_e. \tag{24}$$

B. Limit-Cycle Oscillations in Digitally Controlled Resonant Converters

A major practical issue that should be considered when designing closed-loop resonant based WPT systems, and particularly digitally controlled resonant WPT are limit-cycle oscillations (LCO). As originally presented in [47], the primary cause for steady-state oscillations is resolution mismatch of the quantizing units in the controller, i.e., analog-to-digital converter (ADC) and the DCO (assuming the compensators does not add quantization error) [47]. In addition to the operating-point-dependent gain that exist in resonant converters, the highest sensitivity to gain variations is located around the resonant frequency, a condition that becomes even further emphasized in capacitive WPT systems that operate with very high-quality factors. Since the controller targets optimal transfer conditions which are obtained at resonance (aside from slight deviation from the exact target frequency to facilitate ZVS), this calls for extremely sensitive calibration, i.e., fine frequency resolution generator at MHz range to facilitate LCO-free operation. Therefore, to ensure smooth high-frequency drive throughout the operation range (taking into account the worst-case conditions of the highest quality factor), the ADC and DCO units in this study have been designed to achieve the required effective acquisition as well as control resolution such that limit-cycle oscillations are remedied. Fortunately, the slow-response feature of the resonant network due to high-Q aids in this aspect. Since the network takes several cycles to react to changes in the drive frequency, it is utilized as an averaging action. Frequency dithering is embedded to enhance the drive frequency, and to provide effective frequency (over few cycles) with finer resolution than the base value.

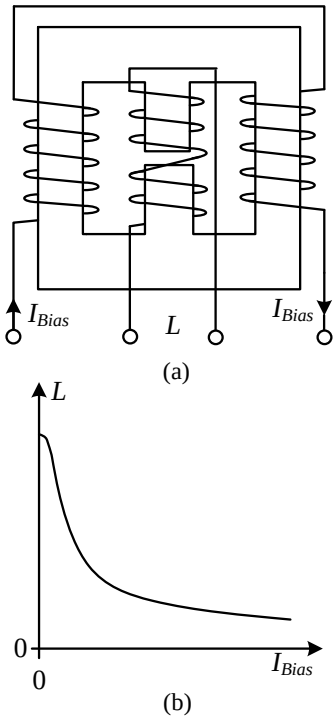

Fig. 8. (a) Variable inductor practical implementation, (b) Relationship between the inductance value and the bias current.

To determine existence of LCO in resonant converters, a comparison is carried out between the LSB values (i.e., resolution) of the digitally acquired value by the ADC and the output signal variation due to one-LSB change of the control [47]-[49]. A necessary condition for no limit-cycles is that the variation of the output ΔS_{out}, due to an LSB change of control is smaller than the ADC resolution Δ_{ADC} [47]

$$\Delta S_{out} < \Delta_{\text{ADC}} = \frac{V_{\text{ADC}}}{2^{N_{\text{ADC}}}}, \tag{25}$$

where V_{ADC} and N_{ADC} are the ADC's reference voltage and number of bits, respectively.

Digitally synthesized frequency is normally carried out by timers that are programmed to reset at a desired value, while maintaining a fixed 50% duty ratio [47]. The generated frequency can be expressed as follows

$$f_{\text{DCO}} = \frac{1}{N_{per} TB}, \tag{26}$$

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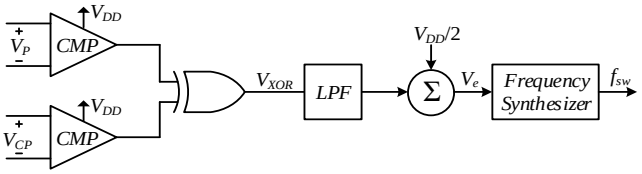

Fig. 9. Simplified schematic of the phase-locked-loop: phase detection, filter (and compensation), and frequency synthesizer.

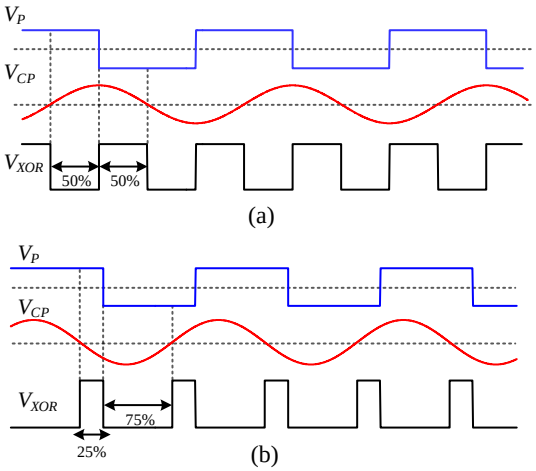

Fig. 10. Signals of the phase detector: (a) Tuned CPT system operating in resonance, (b) Example of a non-tuned CPT system reading.

where N_{per} is an integer and TB is the time-base of the unit clock. The frequency resolution can be calculated as the LSB change in N_{per}

$$\Delta f_{\mathrm{DCO}} = \frac{1}{N_{per}TB} - \frac{1}{\left(N_{per}-1\right)TB} \approx \frac{1}{N_{per}^2 TB} = TBf_{\mathrm{DCO}}^2 \,. \qquad (27)$$

From (27), it can be well observed that the frequency steps of the DCO are limited by the system clock frequency, and increase as the square of the operating frequency, i.e., at lower running frequency, the frequency resolution would be finer than what can be achieved at a higher frequency. Since finer resolution than the one obtained by the system DCO is required, an effective fast dynamics and low distortion frequency dithering procedure has been employed as detailed in [50].

C. Phase Detector

The phase detection in this study has been realized as illustrated by Fig. 9. Since the voltages of the resonators are significantly higher than the operation voltage levels of the controller and other electronics periphery, the voltages V_P and V_{CP} are scaled down using high-impedance attenuation circuit to voltage levels suitable for logic gates input such as the phase detector unit. Form practical implementation perspective, if a simple resistive divider is used, the input capacitance of the logic gate introduces phase delay between the actual zero-crossing point and the digital signal transition. In the case that the phase shifts of the two measured signals are different (due to different resistive path), a systematical offset exist, and should be calibrated out. Thus, to minimize phase offset errors, similar voltage scaling should be employed for both signals as much as possible, which might be impractical in high voltage gain systems. At such cases, active attenuation circuits as well as adaptive calibration are required.

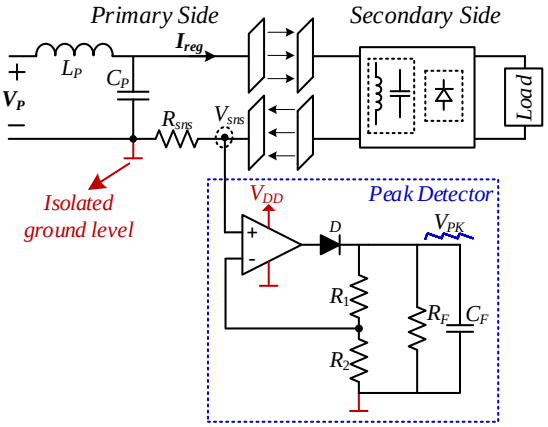

Fig. 11. Circuit diagram of the current-sensing setup.

The phase detector in this study is realized by type-I detection circuit, i.e., comparators as digitizers and an exclusive-or operator (XOR) phase comparator. Typical waveforms of the operation are depicted in Fig. 10, which shows two cases. Fig. 10a exhibits at-resonance operation, with phase difference of 90° and the resulting detector in 50% duty-cycle and averaged output is $V_{DD}/2$ (assuming the voltage supply of logic is V_{DD}). In this case the frequency generated by the synthesizer is stable and fixed. Fig. 10b demonstrates a case where the system is not tuned with a duty-ratio of V_{XOR} is 25%. In this case, the output of the filter is lower than $V_{DD}/2$, and the synthesizer varies its frequency until the desired phase difference is obtained and the filter's output is at $V_{DD}/2$.

D. Current-Sensing Circuitry

The multi mixed-signal controller requires various measurements of the operating conditions in the WPT system. A key measurement of the system is the plates current, I_{reg}, however, this high-frequency current is not trivial to measure and sensing techniques such as current transformer [51] and filter-sense [52] may result in complex sensing circuitry. The current-sensing employed in this study is based on a peak detector mechanism which consists of a simple half wave rectifier configuration as shown in Fig. 11. The sensed current converted to a proportional voltage suitable signal, V_{sns}, by flowing through the resistor R_{sns} [52], [53]. The peak detector is implemented around an operational amplifier to compensate for the voltage drop on the rectifying diode D. An active peak detector is employed so that relatively low gain measurement can be obtained (low resistance shunt resistor), and by doing so lowering the gain-bandwidth requirements of the sensor. The time constant of the peak detector is selected approximately ten times the period of the sensed sinusoidal signal to both filter out the ripple, and smoothly follow the peak value of the signal. The peak detector configuration enables reduced sampling rate requirements of the ADC, and therefore reduces the overall power consumption. Another benefit of this sensing circuitry is that it also provides an information for over-current protection (OCP) and can be used for fault protection of the system.

It should be noted that a key feature of the sensors of the implemented CPT system, in particular of the current sensing circuitry is an isolated ground reference level to the sense resistor as well as the peak detector circuit (Fig. 11). By doing

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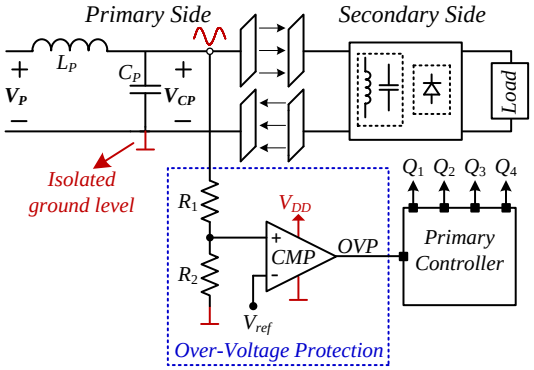

Fig. 12. Circuit diagram of the over-voltage protection setup.

so, the limitations due to sensing relative to a floating voltage node are eliminated, in addition, this configuration also improves the signal to noise ratio.

E. Over-Voltage Protection

As mentioned in the phase detection procedure, the voltage across the resonating capacitors is very high particularly in such high-Q operation. Thus, to avoid any potential failure risks of the CPT system due to over-voltage in the vicinity of the coupler, an over-voltage protection (OVP) mechanism has been implemented as illustrated by Fig. 12. Similar to phase detection process, the voltage V_{CP} is sensed and scaled down by a high-resistance divider network to voltage levels suitable for the comparator operation. The scaling of V_{CP} and the value of the reference voltage, V_{ref}, are determined according to the highest voltage allowed across the capacitor C_P, i.e., across the coupling plates. For a case that V_{CP} is higher than the reference voltage, the comparator output is fed to the primary's controller disabling the gate drive signals (Q_1-Q_4), and as a result the system is turned off, until it is being reset. This also allows to avoid undesired safety concerns due to arcing and high electric fields around the coupling plates [54].

F. Capacitive Coupler Design

To facilitate reliable estimation of the capacitive coupler for the experimental measurements, estimation of the plates capacitances has been carried out by Maxwell (Ansys) finite element analysis (FEA) tool (Fig. 13a). Typically, FEA are generated by defining the geometry of the element and by setting the boundary conditions. In the context of the capacitive coupler in this study, these are four symmetrical copper plates and voltage excitations to the plates. Rigorous simulation procedure over various air-gaps have been carried out to determine the coupling capacitances for symmetrical copper-based capacitive coupler, whereas each plate is 300x300 mm. Additionally, the thickness of the plates has been set to be 2-mm, to assure that it does not affect the coupling. The coupling capacitances of the plates have been calculated based on the equations in [12], [13] and the coupling coefficient, k_C, has been calculated by C_M /. The results for the equivalent mutual coupling capacitance, C_M, and for the self-capacitances (C_{M1} and C_{M2}) as a function of the air-gap are shown in Figs 13b and 13c, respectively. It can be observed that C_M decreases by approximately ten times at an air-gap of 200 mm, while the self-capacitances (C_{M1} and C_{M2}) are in the range of 10 pF and virtually constant when the air-gap is larger than 100 mm. This

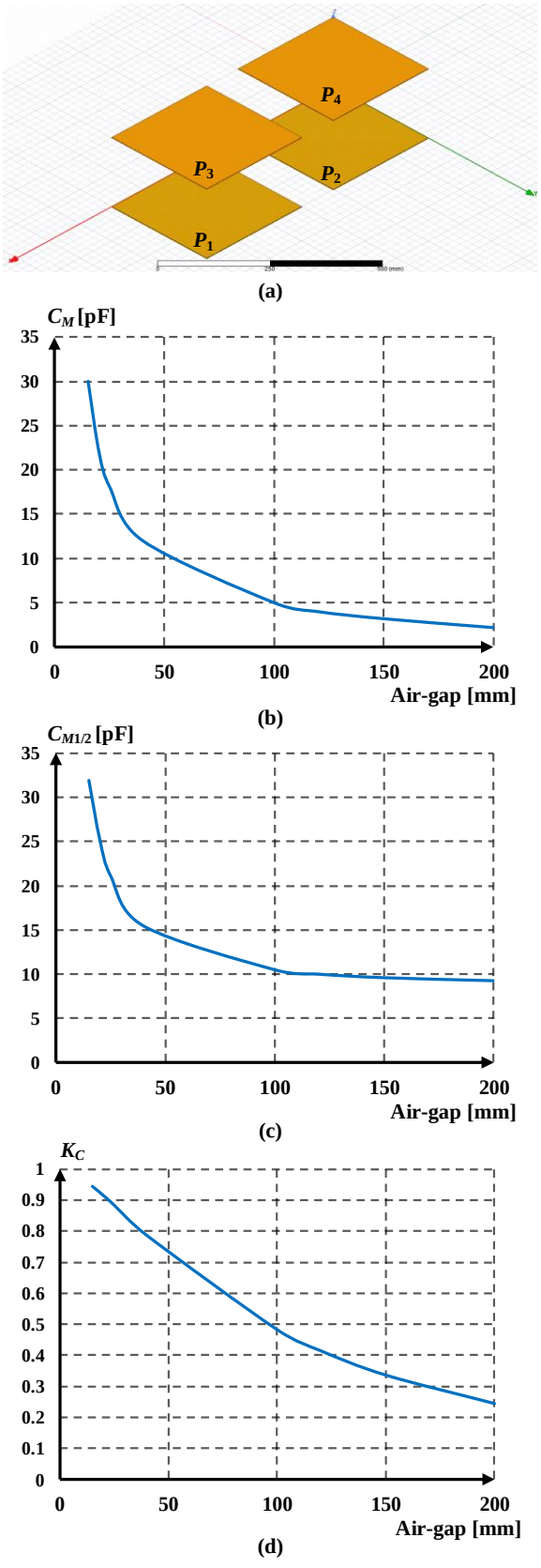

Fig. 13. Finite element analysis for the capacitive coupler design.

is due to the fact that for air-gaps larger than 100 mm, the coupler can be characterized at deep loosely-coupled region as

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can be observed from the results for the coupling coefficient shown in Fig. 13d.

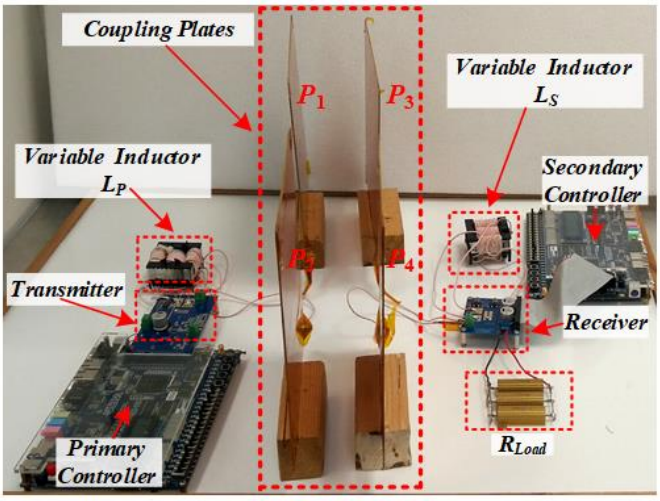
V. Experimental Verification

To validate and demonstrate the operation of the adaptive multi-loop controller, an experimental double-sided *LC* capacitive WPT prototype with four copper plates that form the capacitive coupler has been constructed as shown in Fig. 14a. To guarantee that the dominant capacitances are due the coupling plates, the capacitive coupler has been designed symmetrically based on the analysis in Section IV-F, where each plate is 300x300 mm. Fig. 14b shows the custom designed variable inductor which comprises an *E*-core type ETD49-3F3 magnetic element as discussed in detail in Section IV-A. The controller core has been fully coded in HDL and implemented on a Cyclone IV FPGA [55]. Typically, FPGAs, microcontrollers and other digital platforms provide time-resolution on the order of several hundreds of pico-seconds up to 1 ns. The implemented digital core of the controller is based on an asynchronous hardware using combinatorial circuits as previously described in [42], by doing so, finer resolution can be obtained without significant penalty of power consumption and hardware complexity. Since the coupler structure is symmetric, the matching networks have been also designed to be symmetrical; in nominal operation the inductors' values are set to $LP = LS \approx 75$ µH and the matching capacitors $CP = CS = 250$ pF. High-voltage multilayer SMD ceramic capacitors have been used in parallel to form the matching capacitors. The operating frequency slightly above the resonance $f_0 \approx 1.2$ MHz, guaranteeing soft-switching. The full-bridge inverter has been realized with GaN power modules operable in several MHz [56]. The overall nominal operating conditions and parameters of the experimental prototype are summarized in Table I. It should be noted that the values have been chosen such that for all corner scenarios (output power and air-gap) operating conditions are satisfied.

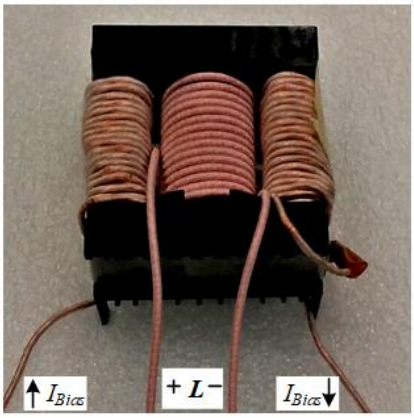
The first step of the experimental validation has been carried out by characterizing the inductance of the variable inductor, and the resulting operating frequency of the CPT prototype as a function of the bias current. Fig. 15 shows the measured results for varying the bias current in the range of 0 to 1 A. It can be seen that in the vicinity of the nominal operating conditions the inductance and operating frequency f_0 are approximately 75 µH and 1.2 MHz, respectively, for a bias current of 0.25 A. It can be observed that this custom designed inductor provides 7X inductance variation, which is translated to 2.5X frequency variation.

TABLE I – Experimental Prototype Values and Parameters at Nominal Operation

Parameter	*Value/Type*
Input voltage V_{in}	30-V
I_{out} peak-to-peak	1-A
Coupling plates	300x300 mm, copper plates
Air-gaps	20-200 mm
Full-bridge transistors	LMG5200, 80 V, 15 mΩ, Dual
Rectifier diodes	5-A/200-V, VSSC520S-M3
Variable inductors L_P L_S	~75µH
Capacitors C_P and C_S	250 pF, AVX MLLC 5
Output capacitor C_{Load}	47 µF, EEV-EB2C470SM
Operating frequency f_0	1.2 MHz



(a)



(b)

Fig. 14. (a) Experimental setup of a double-sided *LC* capacitive WPT prototype; (b) *E*-core type based variable inductor.

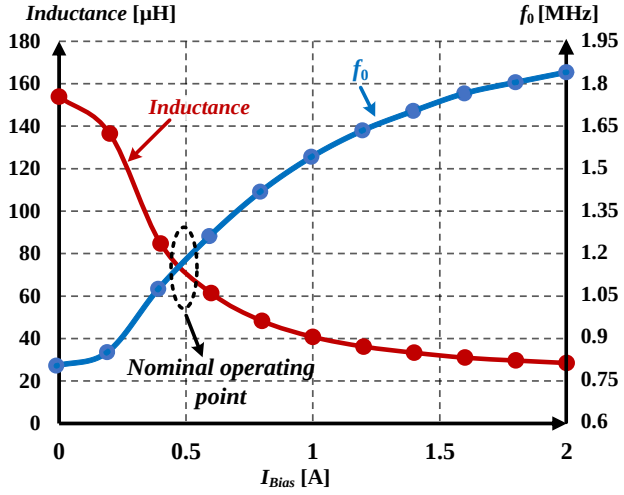


Fig. 15. Experimental measured inductance of the variable inductor and the resultant operating frequency of the CPT prototype as a function of the bias current.

Fig. 16a shows the behavior of the primary's current I_P and the secondary's voltage V_S during tuning process for an input voltage V_{in}=30 V and 100 Ω load for an air-gap of 200 mm approximately, where the quality factor of the primary side was found to be ~50. It can be observed that initially, the system is not tuned and the regulated current on the primary side has a

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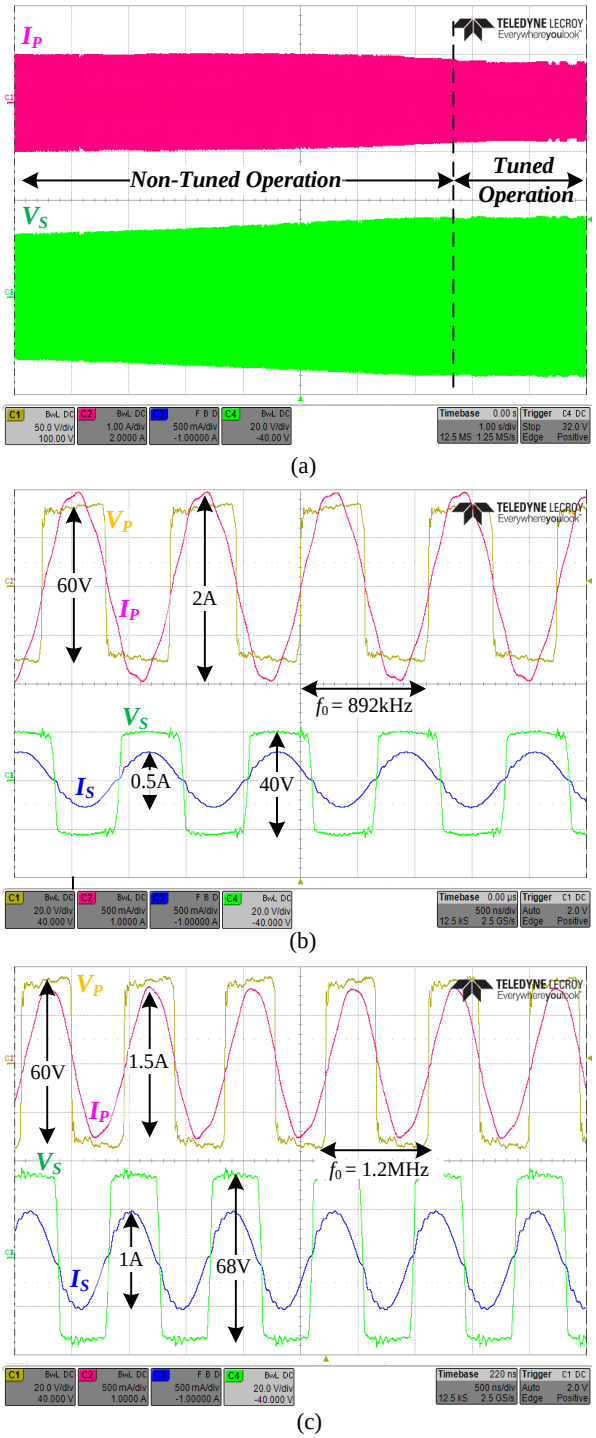

Fig. 16. Experimental results of the tuning process: (a) Full view of the envelopes of I_P and V_S, (b) Zoom-in view on the initial stage, (c) Zoom-in view on the final stage. Voltage scale 20V/div; Current scale 500mA/div; Time scale 500ns/div.

higher peak amplitude compared to the one at the end of the tuning procedure. This is due to the fact that at the beginning the system has some pre-defined values (switching frequency, bias currents etc.) that are not calibrated for the target operating conditions of this particular experiment, and best operating conditions are not satisfied, thus undesired circulating current is drawn from the source. On the other hand, at the end of the tuning procedure the voltage V_S has a higher peak amplitude, since the system is calibrated to resonance and is operated under

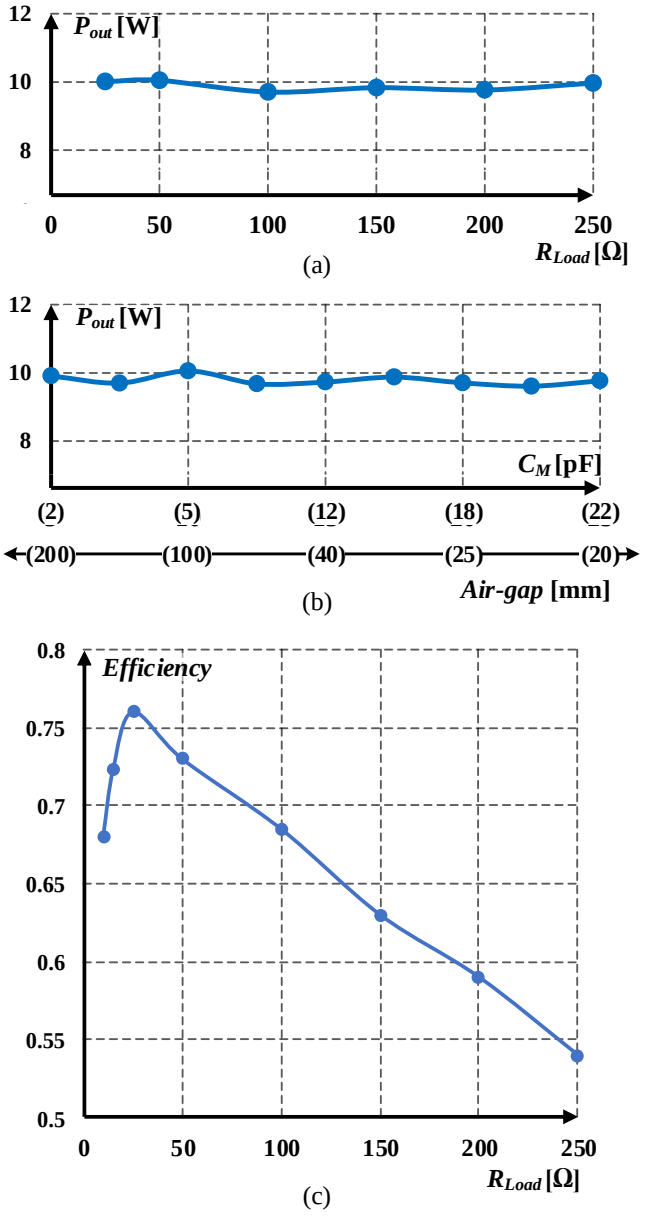

Fig. 17. (a) Measured output power for various loads, (b) Measured output power for various air-gaps, (c) Efficiency as a function of the load.

(local) optimal power transfer conditions according to the target current. Fig. 16b and Fig. 16c show a zoomed-in views of the tuning process with the waveforms of the switching nodes voltages and resonant currents upon initialization (Fig. 16b) and the end (Fig. 16c) of the tuning process. It can be seen that the switching frequency increases from 892 kHz to 1.2 MHz. The output parameters (I_S and V_S) also increase, delivering more energy to the load by more than 2.5 times, while the transfer efficiency has improved considerably (over four times). In addition, it can also be noticed that the primary current *IP* is slightly lagging the primary voltage *VP*, which is the necessary condition to enable soft-switching operation.

To demonstrate the effectiveness of the new multi-loop controller for capacitive WPT systems and showcase of the quality of the performance in closed-loop, the experimental prototype has been also tested for a target power of 10 W over various output load resistances, whereas the coupling

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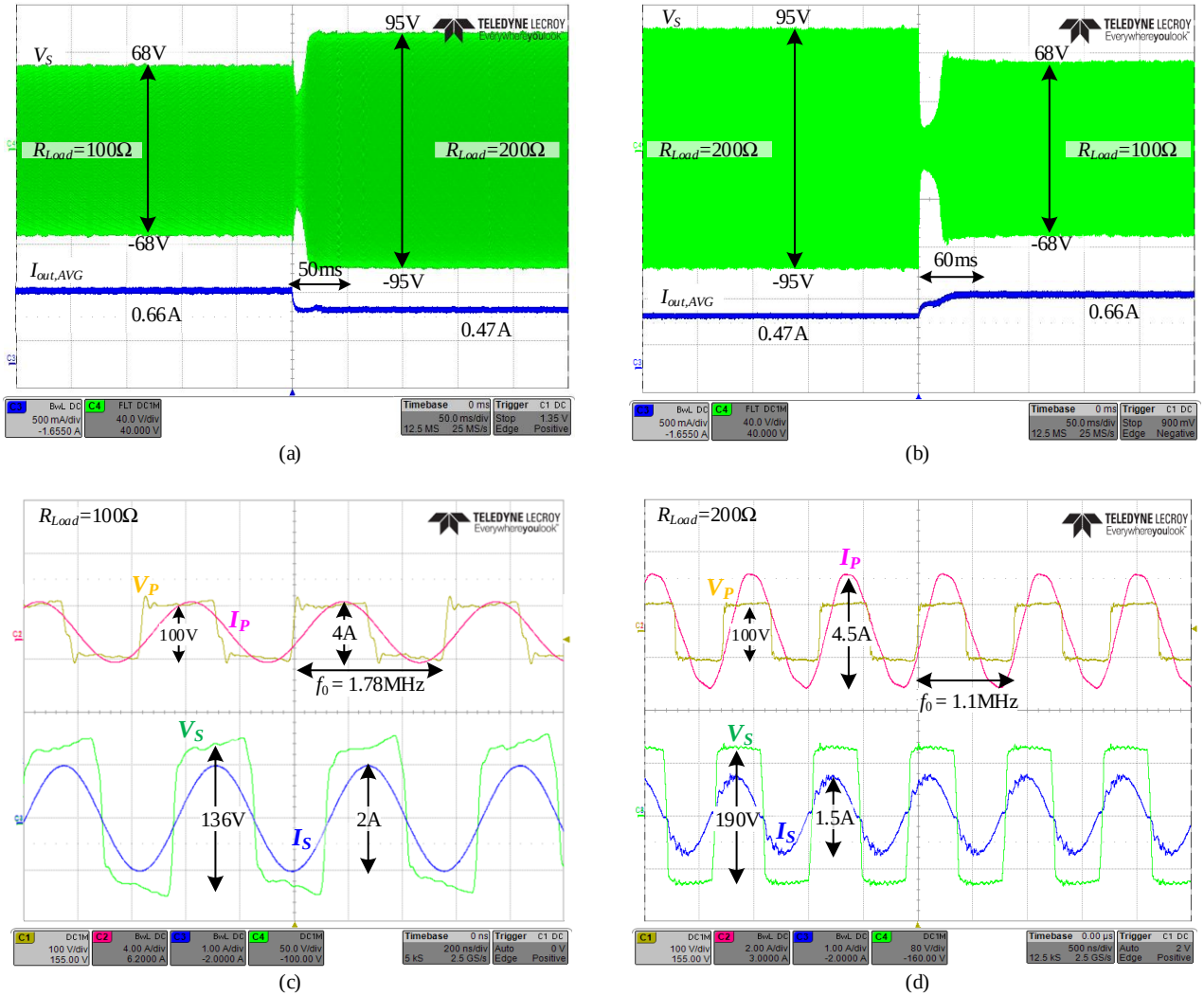

Fig. 18. Experimental results of the tuning process in response to a load step from 100 Ω to 200 Ω: (a) Full view of the envelopes of V_S and $I_{out,AVG}$ for unloading; (b) Full view of the envelopes of V_S and $I_{out,AVG}$ for loading; (c) Zoom-in view on the voltages and current of the primary and secondary on steady-state for 100 Ω; (d) Zoom-in view on the voltages and current of the primary and secondary on steady-state for 200 Ω.

capacitance C_M≈2 pF, as shown in Fig. 17a. A virtually constant power delivery is obtained throughout the load range. In the experiment of Fig. 17b the coupling capacitance has been varied to demonstrate the closed-loop operation under variations in the distance or displacement of the coupling plates. The experiments have been conducted with constant load resistance of R_{Load}=100 Ω, and varying the air-gaps up to the range of 200 mm, this translates to capacitance range of approximately 2–to-22 pF. Similar to the variable load test, it can be seen that, aside from measurement deviation, the output power is well regulated at a constant value. These two measurements validate the closed-loop operation of the self-tuned CPT system, which provides regulated power delivery regardless the medium or load variations. From these experiments, it can be observed that for various output loads and air-gaps the controller provides 10X regulation capabilities. Fig. 17c shows the efficiency curve as a function of the various loads, it can be observed that at the range of 25 Ω the highest efficiency is achieved, which implies that for this experiment this is the matched load resistance to maximize efficiency. Efficiency analysis of a double-sided *LC* CPT system is not a key objective in this paper, and comprehensive efficiency analysis on this configuration is detailed in [15]. It should be emphasized that to achieve constant output power, these measurements have been performed by manually adjusting the reference current in the primary side, $I_{ref,P}$, emulating wireless communication between the transmitter to the receiver.

To further validate the controller approach and demonstrate the operation for higher output power and larger air-gap, the input voltage has been increased to 50 V at an air-gap of 250 mm. Demonstrated in Fig. 18 are load transients of 100 Ω to 200 Ω, for approximately 45 W output power. It can be seen in Fig. 18a that for a load of 100 Ω the average output current, $I_{out,AVG}$ is 0.66 A, voltage V_S toggles between 68 V to -68 V, and the output returns to power regulation within 50 ms. Fig. 18b shows a zoomed-in view of the waveforms of the switching nodes voltages and resonant currents at steady-state, it can be noticed that the operating frequency is 1.78 MHz, and the peak current of the secondary side is 1 A. For loading event from 0.47 A to 0.66 A (Fig. 18c), it can be seen that the system settles down back to the steady-state conditions within 60 ms. Fig. 18d depicts a zoomed-in views of the voltages and currents, there V_S toggles between 95 V to -95 V, I_S peaks at 750 mA, and the operating frequency is tuned to 1.1 MHz

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VI. CONCLUSIONS

An adaptive closed-loop mechanism for capacitive-based WPT systems has been detailed, analyzed and experimentally validated. The controller comprises of multiple control loops, which effectively disengage the power transfer capabilities of CPT systems from any drift or variations, and further enables spatial freedom of the transferred energy from transmitter to the receiver. The control algorithm, signal flow and the functional relationships of the multi mixed-signal controller have been addressed, and all the intricate transfer functions of the key building blocks have been derived. Based on the analysis and intuitive guidelines in this study, the control loops can be fully decoupled, and the multi-loop operation renders down to first-order dynamics, thus, the overall electrical circuitries can be quite moderate in complexity (basic PLL, bias drive, few comparators, etc.). This study also introduced a variable inductor realization that enables continuous self-tuned impedance matching. To demonstrate closed-loop operation under system variations, an experiential resonant *LC* CPT prototype in the MHz range has been constructed, with the core of the multi-loop controller has been implemented on an HDL platform. The resultant dynamic performance of the closed-loop CPT system is well validated through experiments up to air-gap of 250 mm. The new controller concept establishes the foundations for better power delivery in many wireless power applications, and may be found very beneficial in the rapidly growing field of capacitive wireless and other resonant-based wireless technologies.

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