Digital Zero-Current Switching Lock-In Controller IC for Optimized Operation of Resonant SCC

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***Abstract*—This article introduces a lock-in integrated controller for resonant switched-capacitor converter (SCC). The controller identifies the resonant period of each subcircuit on-the-fly and locks-in to the correct switching time to fully utilize the charge transfer rate for each flying capacitor. The various modules of the controller are detailed, including the autotuner and sequencer, which accommodate any mismatch, variations or drifts of component values or circuit configuration. The integrated circuit (IC) has been designed and fabricated on a 0.18 μm 5 V process resulting in effective silicon area of 0.64 mm^2. Experimental results of the controller IC operating in closed-loop are provided, demonstrating accurate lock-in for two resonators with individual independent resonant characteristics. A full-scale hardware prototype of 650 W 4:1 switched-tank-converter is used to validate the controller's operation, demonstrating excellent lock-in capabilities resulting in high efficiency of up to 98.6%.**

***Index Terms*—Integrated circuit, resonant converter, soft switching, switched capacitor, zero current switching (ZCS).**

I. Introduction

SWITCHED-CAPACITOR converters (SCCs) that have been rigorously explored over the last two decades [1]–[10] have established a dominant role in power management in datacenters and other cloud computing related applications. In light of the acceleration of the standardization of the power delivery structure that has been heavily affected by the trend-leading open-computing-project consortium [11], the necessity to step the 48 V rail down to 12 V with extremely high efficiency and very high-power density has established an application stand point at which SCC technology and its derivatives is highly superior over the inductor-based alternatives.

Power density and conversion efficiency are of key importance in datacenters applications (to maximize the amount of computing power per volume). This translates onto extremely strict conversion performance requirements at the 48–12 V level so that it would not further deteriorate the attractiveness of the overall solution. Since this application calls for a fixed conversion ratio, SCC technology renders a very attractive candidate. At medium power levels, SCCs have widely demonstrated peak efficiency over 98% [12], [13]. Results of resonant switched-capacitor based power converters (RSCCs) for datacenters applications, demonstrating peak efficiency of 98.5% around 200 W have been recently presented [14]–[16].

The primary factor that facilitates efficient power conversion for the general case of RSCC is the accuracy of the switching frequency with respect to the resonant conditions of the converter. Optimal charge transfer is achieved in the case that the conduction time of each switching state matches exactly half of the resonator's period, and that deadtime between switching states is minimized [17], [18]. In this way, the charge of the flying capacitor is fully utilized every cycle. Converter topologies with more frequent charge transfer of the output such as [19] inherently feature lower equivalent resistance, and as a result potentially more efficient than topologies with the basic charge-discharge pattern [20].

In topologies that comprise multiple switching states to complete a charge cycle [21], or in configurations with multiple resonators [22], full utilization of the charge out of each flying capacitor, every cycle, introduces complexity to the circuit controller. This mandates accurate zero-crossing information of the flying capacitor current and specific timing settings per switching state (and in some applications, per individual switch). This is since the conduction path is different for every state, which changes the resonant period. The resonant parameters per subcircuit vary as a function of the stresses on the component, loading conditions, the physical layout of the design, and drifts with temperature and over time. In addition, the timing parameters need to account for variations and the accuracy of the current zero-crossing detection (ZCD) circuit. It would be extremely advantageous to utilize a controller, which obtains the ZCD information, identifies on-the-fly the resonant period for each subcircuit, locks-in to the correct switching time, and is capable of automatically compensating any variation of the circuit—this has been pursued in this article.

The objective of this article is, therefore, to introduce a lock-in integrated controller architecture that facilitates accurate switching timing to fully utilize the charge transfer for each flying capacitor at every switching state as schematically illustrated in Fig. 1. The controller adjusts to accommodate any mismatch, variations or drifts at component values or the circuit

Manuscript received May 11, 2020; revised August 5, 2020; accepted September 26, 2020. Date of publication October 9, 2020; date of current version January 22, 2021. This work was supported in part by the Israel Science Foundation under Grant 2186/19 and in part by the Vishay Ltd., Siliconix IC division. Recommended for publication by Associate Editor M. Rodriguez. *(Corresponding author: Mor Mordechai Peretz.)*

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Digital Object Identifier 10.1109/TPEL.2020.3029976

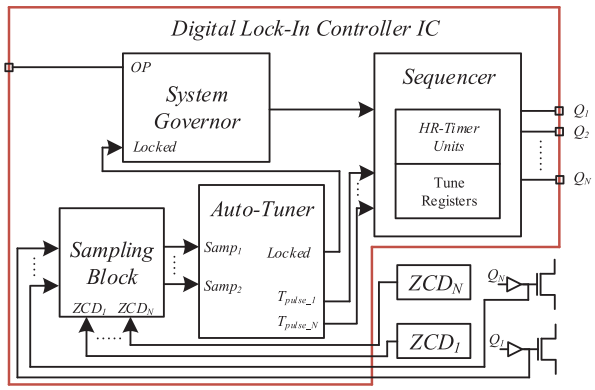


Fig. 1. Simplified schematic diagram of the digital lock-in controller IC.

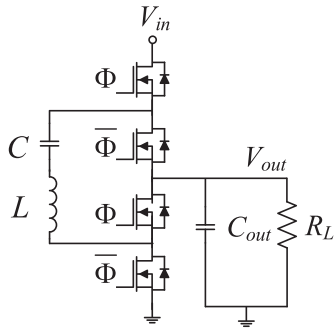


Fig. 2. Conventional 2:1 RSCC.

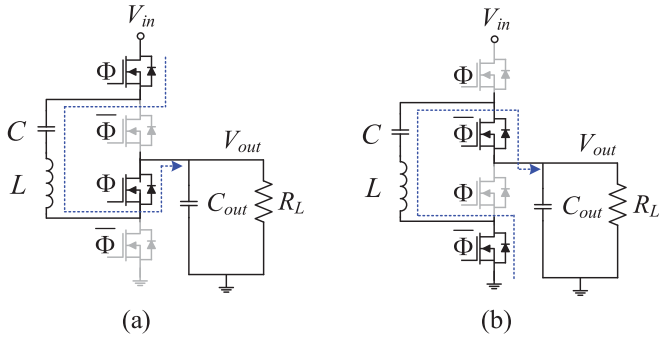


Fig. 3. Equivalent circuits of the 2:1 RSCC. (a) Charging state. (b) Discharging state.

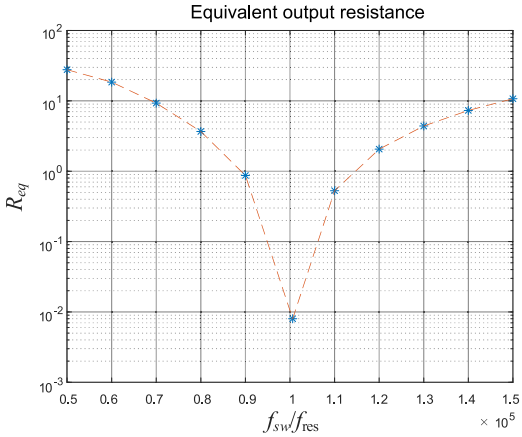


Fig. 4. Equivalent output resistance for a 2:1 RSCC.

configuration. Two lock-in architectures are presented and described in detail. One based on synchronized digital hardware and suitable for medium frequency range applications (in the range of several hundred kilohertz) whereas the second method is based on asynchronous combinatorial logic and features very high-frequency resolution, which qualifies to the megahertz range. The control method is demonstrated for two resonators, with individual independent tuning per subcircuit and switching state. It is a further objective of this article to present an all-digital IC implementation of the lock-in switching governor and detail the fundamental building blocks. A controller IC with very high-resolution gating commands and extremely small silicon area will allow further miniaturization of the overall solution without compromising on accuracy and conversion efficiency, this has been pursued in this article.

The rest of this article is organized as follows. Section II details the importance of zero current switching (ZCS) in RSCC and provides mathematical analysis of the charge transfer-rate. Section III describes the controller architecture and details its operation and the specific structure of the integrated units. Section IV details a case study of a 4:1 switched-tank converter, covering the full circuit details, operation of the controller on the specific converter as well as the details of the ZCD acquisition method. System level and performance challenges are discussed in Section V. Section VI provides postlayout simulations as well as experimental validation of the fabricated IC on a discrete prototype. Finally, Section VII concludes this article.

II. Importance of ZCS in RSCC

RSCCs have been widely discussed for being soft-switched and to some extent advantageous compared to hard-switched SCC [12]–[15], [22]. As opposed to intuition that the major difference is the effect of soft-switching itself, the dominant contributors for efficient operation is the ability to fully utilize charge transfer of the resonant tanks. This can be shown by the classic $R_{\rm eq}$ derivation and from charge transfer context. In this chapter, mathematical derivation of the charge transfer rate to the load as well as equivalent output resistance analysis is given for a conventional 2:1 RSCC, as shown in Fig. 2. The output capacitor, $C_{\rm out}$, is assumed to be much larger than the resonant capacitor C. The operation of the 2–1 RSCC can be divided into two states—a charging state and discharging state, as illustrated in Fig. 3(a) and (b), respectively. The switches are driven alternately with 50% duty ratio in two phases,Φ and $\overline{\Phi}$. The current in the LC tank has a sinusoidal shape, which dictates the optimal gating sequence to maximize the converter's efficiency and to fully exploit the charge transferred by each subcircuit.

The generic equivalent circuit model for RSCC describes the losses by an equivalent resistance connected at the output of the converter [1]. Evaluation of $R_{\rm eq}$ as a function of $f_{\rm sw}$ is analyzed and depicted in Fig. 4. Here, the equivalent output resistance

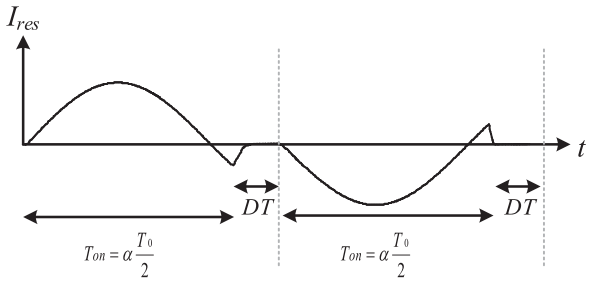


Fig. 5. Resonant tank current during late-switching operation.

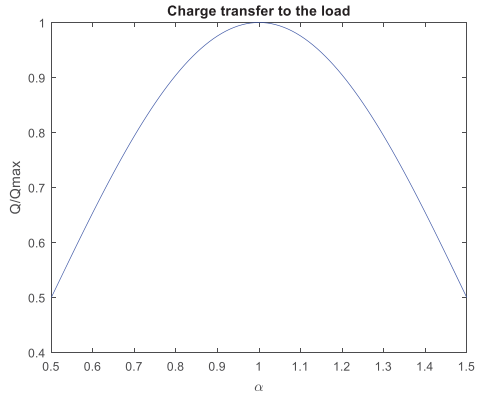


Fig. 6. Charge transferred to the load as a function of the converter switching-state.

has been calculated for a wide range of switching conditions. As can be seen, the minimum value for $R_{\rm eq}$ is when accurate resonance operation is achieved. This can also be derived from charge transfer analysis. An illustration of the resonant current is shown in Fig. 5 for a case of late-switching operation, but the analysis brought here applies for the case of early switching without any modifications. The resonant characteristics of the converter are derived from its passive components' values, and can be expressed as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad ; \quad T_o = \frac{1}{f_0}. \tag{1}$$

Including a short deadtime period between each switching state (DT in Fig. 5), the switching period is obtained by the following:

$$T_{sw} = 2T_{on} + 2DT \tag{2}$$

where $t_{\rm on}$ is the conduction time during each phase of the switching period (Φ or $\overline{\Phi}$). The resonant current can be described with the aid of (1) and (2) as

$$I_{res}(t) = \begin{cases} I_{peak}\sin(2\pi f_0 t), & 0 < t < \alpha\frac{T_0}{2} \\ 0, & \alpha\frac{T_0}{2} < t < \frac{T_{sw}}{2} \end{cases} \tag{3}$$

where α represents the switching mode of operation. In the case of $\alpha < 1$, the converter operates in early switching while late-switching occurs in cases where $\alpha > 1$. ZCS operation is obtained when $\alpha = 1$.

The output dc current equals the average resonant current during each of the switching phases, therefore, the following equation holds:

$$\frac{1}{T_{sw}/2}\int_0^{T_{sw}/2} I_{res}(t)dt = I_{out}. \tag{4}$$

By integrating (4), the peak value of the resonant current can be extracted, expressed as

$$I_{peak} = \frac{I_{out}\cdot\pi\cdot f_0\cdot T_{sw}}{1-\cos(2\pi f_0\frac{\alpha T_0}{2})}. \tag{5}$$

The charge transferred to the load during half of a switching period is derived by integrating (3), as follows:

$$Q = \frac{I_{peak}}{2\pi f_0}(1-\cos(\alpha\pi)). \tag{6}$$

The value of α that results in the maximum charge transferred to the load is obtained by taking the derivative of (6) with respect to α and equating the result to zero. Solving the resultant equation yields that maximum charge is transferred to the load in the case of $\alpha = 1$, which correlates to the case of ZCS. Shown in Fig. 6, is the relation between the charge transferred to the load as a function of the converter switching state for a given value of peak resonant current. The analysis brought here applies also for multistage RSCCs in which maximum charge transfer rate to the load occurs if ZCS operation is obtained for all resonant tanks.

III. Digital Lock-In Controller

The digital lock-in controller illustrated in Fig. 1 is described in this section in a general form and can be applied to various types of RSCC-based single or multistage converters topologies. The controller comprises the following modules as depicted in Fig. 1 (described in-detail in the sections as follows):

1) a system governor to manage, synchronize, and dictate the operation mode;
2) autotuner unit to adjust and calibrate the conduction time of the switches to achieve ZCS operation in all resonant tanks;
3) switching sequencer to generate the required drive signals to the power switches;
4) a sampling block for accurate reading of the ZCD sensors' outputs.

One possibility for tuning the drive frequency to the resonant characteristics can be performed by immediate response to the information from the zero-crossing point sensor [22], [23]. This method may be problematic for some cases due to latencies and delays in the system. An alternative approach that is utilized for high switching frequency applications [24] performs delay-locked-loop convergence of the switching frequency to the resonant one. Such utilization, as employed in this article, locks in to the desired running frequency and compensates for any variations or mismatches in the system. This operation suits well resonant conversion, in particular at high-Q, since the response of the system to variations is rather slow and carries on over several switching cycles. In the specific case on-hand, as described in this article, the main motivation of the tuning comes from thermal considerations, to achieve optimal transfer

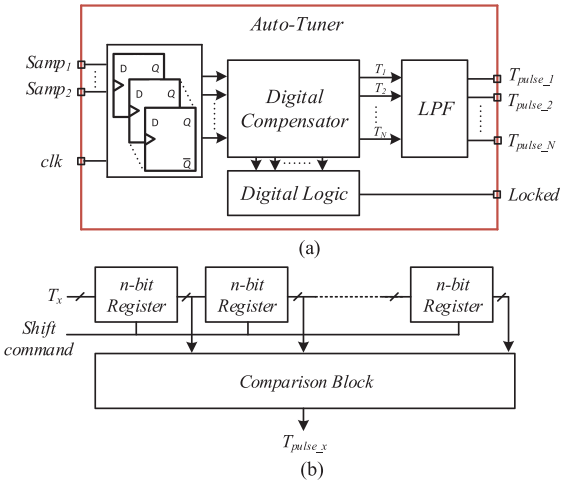


Fig. 7. (a) Internal block-diagram of the autotuner module. (b) Simplified block-diagram of the LPF.

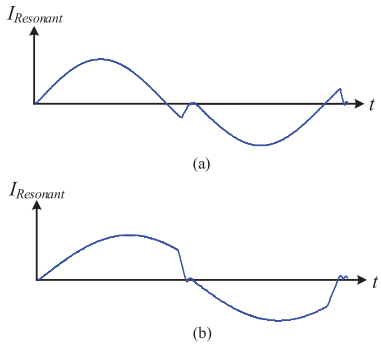


Fig. 8. Current waveform of a resonant circuit switched-OFF at: (a) Late switching. (b) Early switching.

conditions, which result in the highest efficiency conditions in the system, is a relatively slow-varying objective that can be fulfilled well with a lock-in tuning architecture.

The tuning process is performed by the relatively slow internal clock of the controller IC, resulting in a simple and straightforward realization of the *sequencer* and the *sampling* blocks. For converters operating at higher frequencies, the frequency detection, and generation units have been realized through asynchronous combinatorial logic to enable operation with higher resolution than of the one obtained by the internal synchronous clock.

A. System Governor

The governor module dictates the desired operation mode of the converter, based on auxiliary configuration (OP in Fig. 1). In the private case for a conventional RSCC, the governor decisions include light-load operation of the converter, start-up, and turn-OFF sequences as well as the applied deadtime. For more complex topologies, the system governor may dictate various switching schemes to minimize on-board periphery such as ZCD sensors in multistage converters, and even to determine the voltage conversion ratio. In this article, all synchronization actions performed by the system governor are based on an internal clock (in the specific case is 20 MHz). A feedback from the autotuner block (Locked in Fig. 1) provides the governor with the required information regarding the tuning process. To support wide range of resonant converters, start-up, and turn-OFF sequences can be reprogrammed with no hardware modifications.

B. Autotuner

The autotuning module consists of several internal units, as shown in Fig. 7(a). A digital compensation unit evaluates the sampled ZCD signals and determines whether the resonator current is zero when the transistor turns OFF. Nonzero resonant current at transistor turn-OFF will occur in case of "early" or "late" switching, as illustrated in Fig. 8. Based on the information of the polarity of the current at turn-OFF, the compensator modifies the ON-time for each resonant tank separately [T_x in Fig. 7(a)]. The ON-time of the next switching cycle is increased in case the sampled ZCD signal indicates "early" switching and decreased in case of "late" switching indication. Once the sampled signal of the ZCD indicates ZCS, the ON-time remains unchanged. The initial values that the unit starts the process with can be programmed in advance, or can be used as default, depending on the length of the start-up tuning procedure that is allowed.

The compensator block is followed by a digital low pass filter (LPF) to smooth any noise variations, and it also functions as a possible degree of compensation network in cases where additional lagging phase is required. In this article, filtering is performed by comparing a configurable number of compensator outputs, as shown in Fig. 7(b). At the beginning of each switching cycle a shift operation is performed on the register structure and the output of the LPF filter is calculated [T_{pulse_x} in Fig. 7(a)]. The tune-registers are updated only when all registers hold the same value, which completely eliminates the effect of singular non-ZCS events or inaccurate indications of the ZCD sensors on the converter's operation.

The autotuning module allows flexible choice of the resonant tank values, which determine the operating frequency of the converter. At power-up a lock-in routine is initiated in which the autotuner locates the resonance frequency of each tank. During normal running mode, the module observes the operation of the power-stage and provides fine-tuning to ensure ZCS in case the passive components drift from their values upon start-up.

C. Sequencer

The *sequencer* module executes the gating signals to the power stage based on the information from the preceding modules. It incorporates a multiphase high-resolution timer to ensure correct and precise pulse-length for single or multistage converter topologies. The gating signals are set independently per resonator (or subcircuit) of the converter so that ZCS operation can be separately realized per all resonant tanks or stages of a converter, regardless of component mismatches or variations.

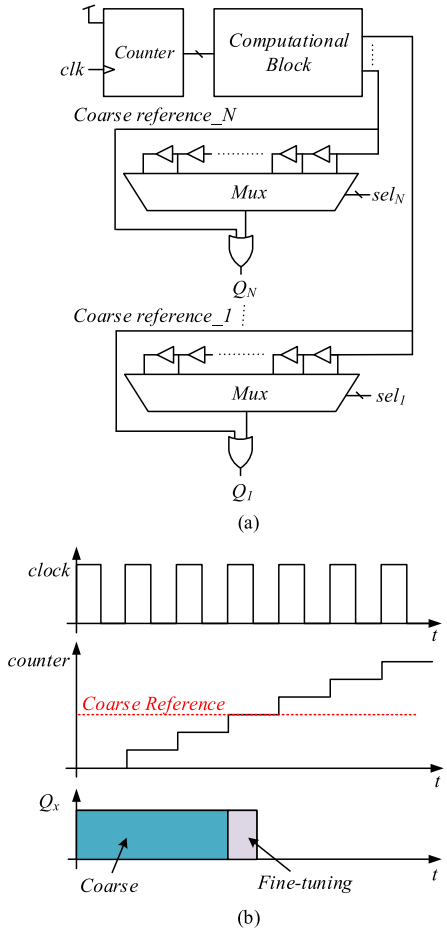


Fig. 9. (a) Simplified block diagram of the sequencer module. (b) Delay-line based high-resolution pulsewidth modulation signal.

The conventional approach to implement a high-resolution timer is by a fast-clock counter-comparator scheme [25]–[27]. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n f_s$, which translates to increased power consumption. In this article, the high-resolution pulsewidth drive signals for the power switches are produced by incorporating a coarse-counting block followed by a fine-tuning delay-line based module, as shown in Fig. 9(a). This allows a design that is based on standard cells, and enables direct synthesis with low-power consumption. As can be seen in Fig. 9(a), a counter-based signal is generated independently for each resonant tank by the information provided from the autotuner block. This signal is then delayed by the delay-line to achieve the exact ON-time for ZCS operation of all resonant tanks by setting the input of each multiplexer unit according to its *sel* command, which is supplied by the autotuner, as shown in Fig. 9(b). Protection logic and other gating-related features are also incorporated in this module to allow full completion of a sequence and to avoid overlapping of signals in case the resonant tanks operate with different drive sequences. The time resolution of the sequencer block is identical to the propagation delay of the buffer-cells used with some additional delay caused by the multiplexer. Matching the time-resolution of all drive signals, is achieved by placing all delay-lines in proximity to one another and by doing so, eliminating any variations caused by temperature or fabrication faults.

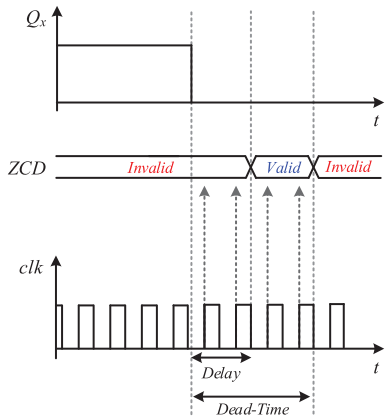


Fig. 10. Continuous-sampling based approach of the ZCD sensors.

D. Sampling Block

Inherent delay between the generated gating signals in the controller and the actual conduction of the transistors is quite common for all switch-mode applications. This delay, from a controller point of view, is generally unknown and may significantly vary as a function of the operating point or the passive components, driving circuitry, and power transistors used [28]–[31]. The information regarding the polarity of the resonant current at transistor turn-OFF, which is the indicator for early or late switching of the transistors, is only valid in proximity to the switching event. Sampling the ZCD sensors must be able to compensate, or at least consider this inherent delay so that an accurate status information is obtained, i.e., early or late switching.

In this article, two completely synthesizable approaches have been realized to acquire the information from the ZCD sensors while accounting for the abovementioned delay. The first is based on continuous sampling of the ZCD sensors at the internal clock's frequency from the turn-OFF command by the controller until the end of the applied deadtime period, as shown in Fig. 10. Here, the ZCD sensor is sampled at the beginning of each clock cycle and the acquired result is processed according to a state-machine algorithm to acquire the converter's switching-state. Once the deadtime period is over, the sampling block provides the autotuner with the valid readings for further processing and tuning operations.

The second approach requires less computational efforts during the sampling process, yet still allows sampling with greater proximity to the switching action to further minimize charge losses due to late or early switching of the transistors. This is performed by incorporating a *delay-estimation logic* (detailed in Section V), which accurately estimates the inherent delay upon start-up, illustrated as Δ_s in Fig. 11, in addition to a delay-line based structure that generates a sampling signal with a resolution of a single delay-element. Once the ZCD sensors have been

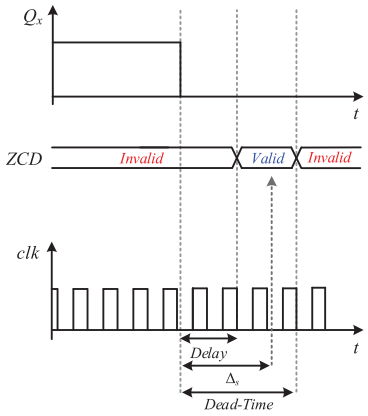


Fig. 11. Single-sample based approach of the ZCD sensors.

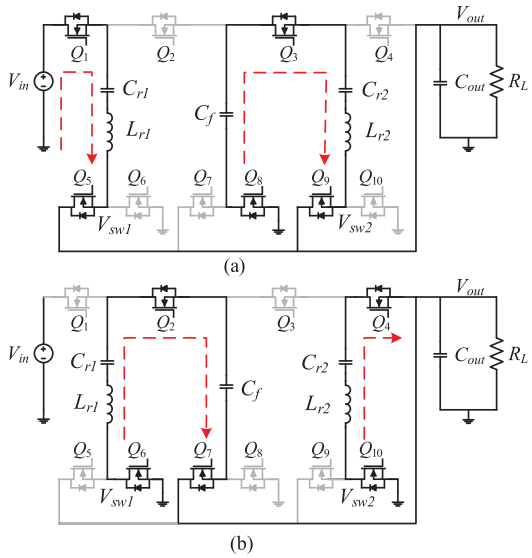


Fig. 12. Equivalent circuits of the 4:1 STC. (a) Charging operation of the resonant tanks. (b) Discharging operation of the resonant tanks.

sampled, the sampling block provides the autotuner with the acquired readings for further processing and tuning operations.

IV. 4:1 STC Control and Simulation Case-Study

As described earlier, the ON-time for each resonant tank is modified by the autotuner to achieve ZCS operation based on the polarity of the resonant current at turn-OFF. The operation of the controller is demonstrated for a 4:1 switched-tank-converter (STC) [14], which comprises two resonators, independently tuned to achieve full ZCS operation, as shown in Fig. 12. The operation of the STC can be divided into two states—charging or discharging of the resonators, as shown in Fig. 12(a) and (b), respectively, with a short deadtime period between them. The flying capacitor (intermediate element in Fig. 12) connects to a different resonator at each active subcircuit, resulting in charge transfer from the input to the output. The flying capacitor value is chosen such that it will have negligible effect on the resonant frequency of the resonant tanks ($C_f >> C_r$). Soft-charging is

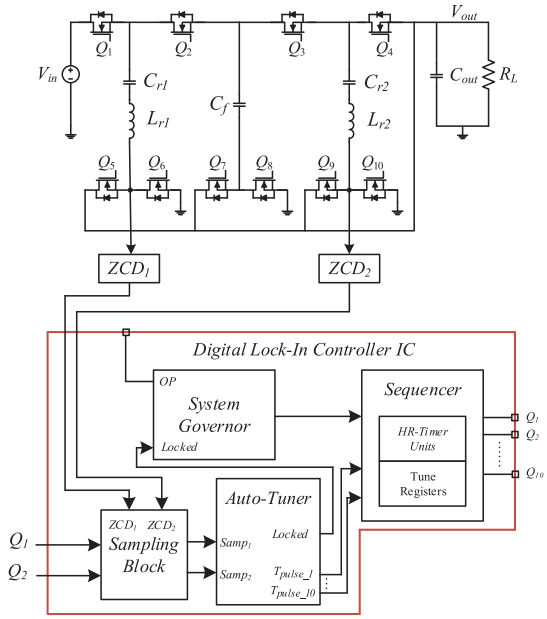


Fig. 13. Digital lock-in controller and 4:1 STC.

achieved for all capacitors in the system, and soft-switching of all switches can be achieved allowing the correct timing which is the task of the controller. For the case of 4:1 conversion ratio STC illustrated in Fig. 12, the voltages at V_{sw1} and V_{sw2} are a direct indicator to the current polarity at turn-OFF. In case of early switching, the resonant current is flowing towards V_{sw1} or V_{sw2} [as shown in Fig. 12(a)] and the voltages are clamped to $V_{\text{out}} + V_F$ (where V_F is the forward voltage of the transistor's body diode). The same applies to the case of late switching where the current is flowing from V_{sw1} or V_{sw2} [as shown in Fig. 12(b)], here the voltages will be equal to $-V_F$. Therefore, the ZCD inputs to the controller are obtained from V_{sw1} or V_{sw2}. Fig. 13 illustrates the connections between the digital lock-in controller and the 4:1 STC power stage. Two independent ZCD sensors are realized to allow consecutive as well as parallel sampling, as illustrated in Fig. 13. The gating commands, Q_1 and Q_2, indicate the end of the charging operation of the first and second tanks, respectively [see Fig. 12(a)] and mark the beginning of the deadtime period.

Fig. 14 shows a two-comparator based ZCD sensor, employed in this article, which produces a 2-b representation of the switching-node voltage. Two references are produced as a function of the output voltage, V_{th1} and V_{th2} in Fig. 14, which feed the upper and lower comparators negative inputs, respectively. This configuration acts as a small thermometric coder. The ZCD sensor produces a 2-b result indicating late-switching (2'b00), early switching (2'b11) or ZCS operation (2'b01), which is the input to the auto-tuner block, as shown in Fig. 1.

The ZCD sensor's resistors are chosen according to the following:

$$\frac{R_C}{R_B + R_C + R_A} < \frac{R_2}{R_1 + R_2} < \frac{R_B + R_C}{R_B + R_C + R_A} \tag{7}$$

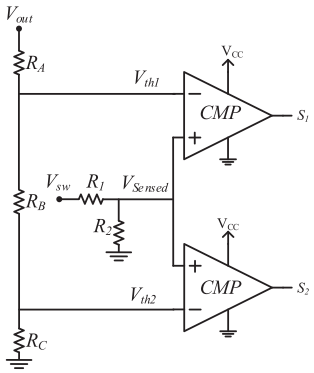


Fig. 14. ZCD sensor.

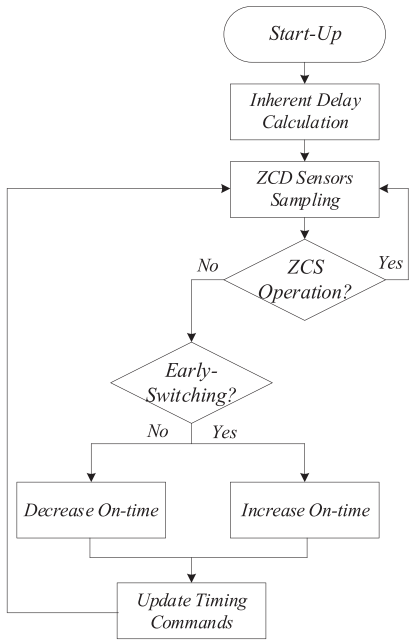


Fig. 15. Flowchart of the lock-in procedure.

where R_1 and R_2 determine the gain of the sensed switching node and R_A, R_B, and R_C determine the reference window. The sensor tracks the output voltage and produces the references so that convergence to ZCS is guaranteed, regardless of the switching-state (i.e., early or late-switching) upon start-up. The controller observes the status of the ZCD sensors after transistor turn-OFF and the ON-time for each tank is modified accordingly by the compensator.

The verification of the controller operation has been carried out on a 48–12 V STC by a set of simulations conducted in PSIM (PowerSim, Inc.); deliberate mismatch between the passive components' values was imposed to verify the effectiveness of the controller. The resonant tanks' parameters are: $C_{r1} = 2.35\ \mu$F, $L_{r1} = 70$ nH, $C_{r2} = 2.1\ \mu$F, $L_{r2} = 63$ nH, $C_f = 40\ \mu$F, and $R_L = 0.26\ \Omega$. Upon start-up, the inherent delay between the controller's gating signals to the power switches is calculated (detailed in Section V). Then, based on the ZCD sensors' readings the autotuner adjusts the timing signals for each resonant tank independently, as indicated in the flowchart of Fig. 15. Once full-ZCS operation is achieved for both resonant tanks, the controller performs fine-tuning in case of components' values drifts.

Results of the lock-in tuning process are shown in Fig. 16(a)–(e), demonstrating convergence onto tuned conditions from off-tune starting points of both resonators, where Fig. 16(c)–(e) is a zoom-in of the area marked C, D, and E in Fig. 16(a), respectively. It can be seen that the output voltage increases to approximately 12 V, which is the no-load target voltage, indicating that in the context of optimal charge transfer, the controller adequately fulfills its task. A magnified view of one period for ZCS operation of a 4:1 STC with mismatched resonant tanks is shown in Fig. 17.

As can be seen from the simulated results of Fig. 16, the controller is capable of supporting multiresonant RSCC [22], [32]. The lock-in feature of the controller tunes the ON-time of each resonator according to its resonance frequency and considers all resonant-tanks for the calculation of the total switching period (shown in Fig. 17). For topologies with inductor in series with the flying capacitor the implementation is straightforward and in many cases the ZCD sensor of Fig. 14 can be used

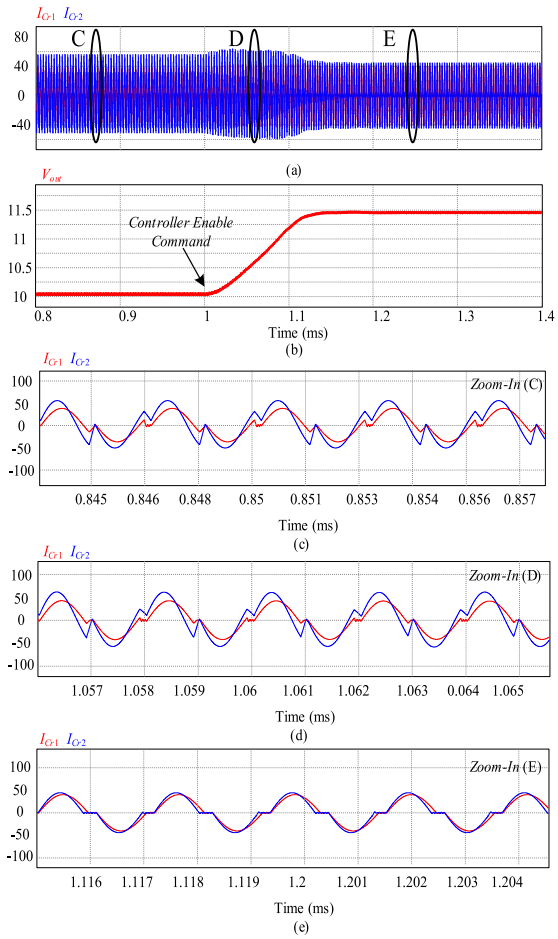


Fig. 16. Closed-loop operation of the controller for a 4:1 STC converter. (a) Resonant currents. (b) Output voltage. (c) Zoom-in on the resonant currents before controller enable command. (d) Zoom-in on the resonant currents during the convergence period. (e) Zoom-in on the resonant currents at steady state.

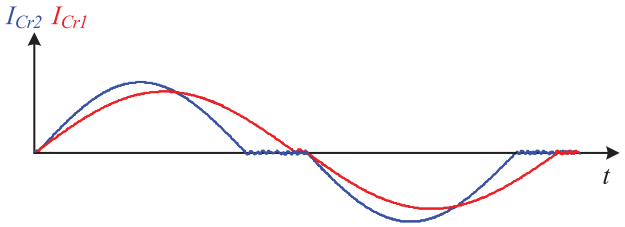


Fig. 17. Resonant currents during ZCS operation of a mismatched tank operation of a 4:1 STC.

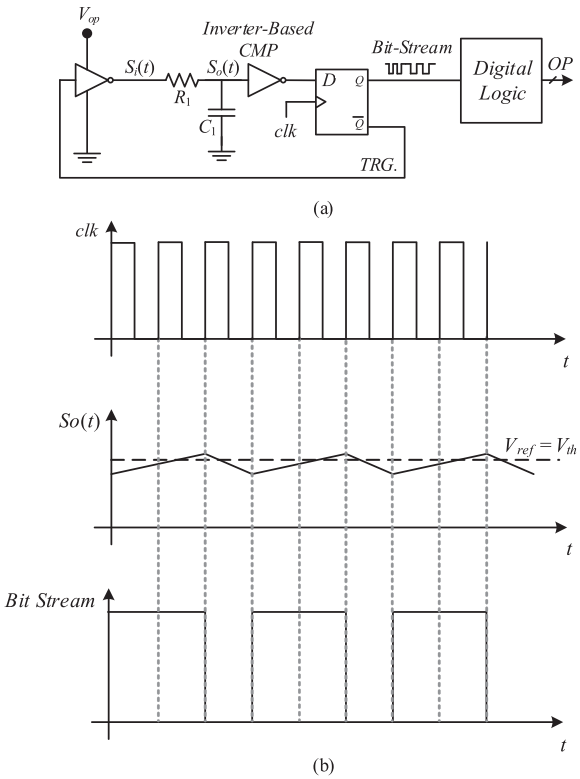


Fig. 18. (a) Simplified architecture of the single-pin configuration hardware. (b) Modulator's key waveforms.

without any modifications. The controller also supports RSCC topologies with inductor at the output node [32], but may require modifications to the ZCD sensors.

V. System-Level and Performance Challenges

A. Single-Pin Configuration

In complex controller ICs where pin-count is an important asset and it is required to provide access to a large number of operating modes, a single-pin setup is essential. This implies that programming, mode selection, or values setting are carried out according to the voltage level that is imposed on the input pin. The amount of levels that can be utilized in this approach depends on the voltage span allowed on the input, resolution, and accuracy of the detection unit. The single-pin configuration is facilitated in this article by a sigma-delta (SD) modulator and digital logic as shown schematically in Fig. 18.

The SD modulator has been realized with simplified hardware to reduce complexity and the effective area. This may come at the cost of performance or conversion speed, but since the objective of this ADC is to acquire static, or semistatic, voltage levels, the solution fits well within the specifications. As can be seen in Fig. 18, the modulator front-end is realized by a digital inverter, with $V_{\rm op}$ as the high logic level (supply). The integrator is realized by a simple *RC* network with a corner frequency of at least one order of magnitude lower than the clock frequency. Quantizer is realized by another digital inverter. The result is then held by a *D*-flipflop to facilitate a clocked bit-stream and to generate the oversampling frequency of the ADC. The resultant SD-based ADC is a hardware-efficient voltage level translator, the average voltage at node $S_o(t)$ can be expressed as

$$\overline{So(t)} = V\text{ref} = Vop\frac{CNTRn}{2^n} \tag{8}$$

where $V_{\rm ref}$ is the reference value for the modulation process (the threshold voltage of the inverter-based comparator) and CNTR_n is the number of logic-high occurrences in the bit stream for 2^n clock cycles. An illustration of the voltage at the input of the inverter-based comparator, $S_o(t)$, is shown in Fig. 18(b) along with the resultant bit-stream and the oversampling-clock.

The bit-stream is the input to the computational logic, which counts the amount of "ones" (equals to CNTR_n) with a dedicated counter which acts as a sinc LPF, and resets at predefined intervals to perform decimation. In this article, the voltage applied on the front-end inverter is translated to a digital representation every 1024 clock cycles, which results in a 10-bit representation of the desired operating mode of the controller.

B. Inherent Delay Calculation

Estimation of the inherent delay between the gating signals of the controller and the actual turn-OFF of the power transistors is performed upon start-up and every $N_{\rm est}$ STC switching cycles to account for variations of the passive components (*Nest* is set by the configurable inputs of the controller, OP in Fig. 1). Upon initiation of the delay estimation procedure, a predefined switching frequency is applied on both tanks so that early switching operation is ensured. As a result, the voltage at the switching nodes, V_{sw1} and V_{sw2}, is clamped to $V_{\rm out} + V_F$ when the power stage transistors are turned-OFF at the end of the charging phase, as shown in Fig. 19. To estimate the inherent delay, sampling the ZCD sensor is performed once every switching cycle in different locations ($\Delta_{\rm x}$ in Fig. 19) until the early switching reading from the ZCD sensor is acquired (2'b11), as shown in Fig. 19(b)–(d). The inherent delay, $\Delta_{\rm s}$, is estimated to be the minimum delay between the controller gating signals and a sampling command that acquires a valid reading from the sensor. For practical reasons, an additional small configurable delay is added to the measured $\Delta_{\rm s}$.

VI. Experimental Verification

A digital controller IC for RSCC has been designed and fabricated in 0.18 μm 5 V process. The IC layout is depicted in Fig. 20 with overall die area that is pad-limited at 4 mm^2,

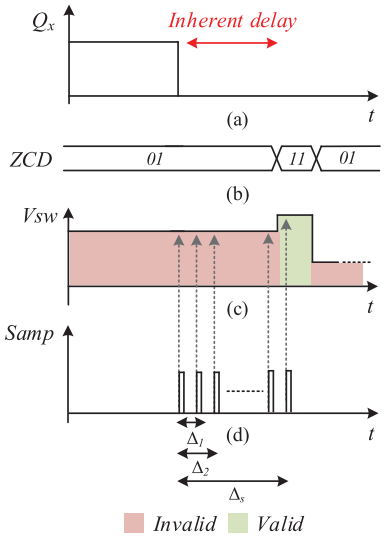


Fig. 19. Waveforms during the inherent delay calculation procedure. (a) Controller gating signal. (b) ZCD sensor. (c) Switching node. (d) Sampling signals.

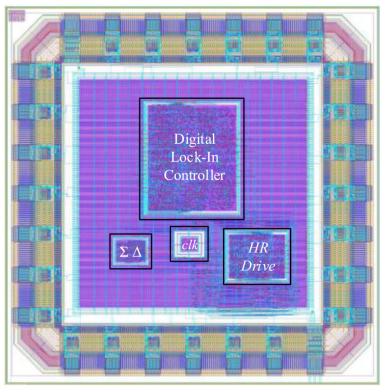
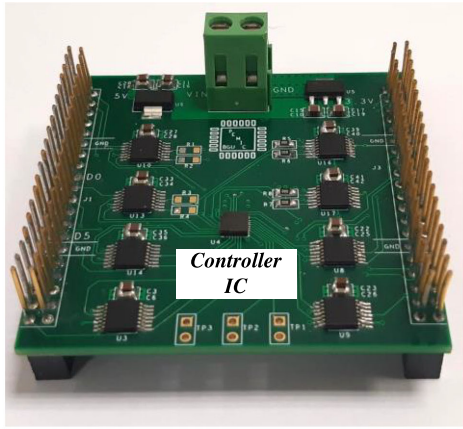


Fig. 20. Layout of the fabricated RSCC controller IC.



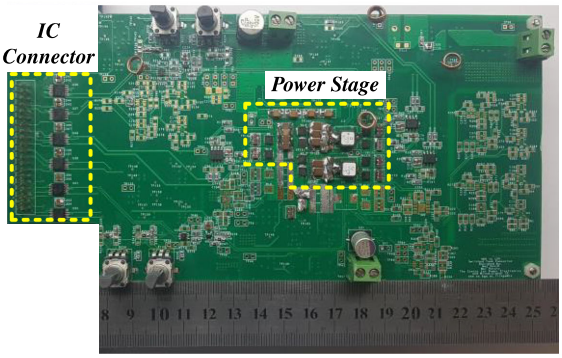


Fig. 21. (a) Controller IC PCB board. (b) Experimental prototype of a 4:1 STC for evaluation of the controller IC.

while the effective silicon used is 0.64 mm^2. The fabricated IC on a printed circuit board (PCB) is shown in Fig. 21(a). The delay of the buffer-cell used for the asynchronous logic is 200 ps and the internal clock frequency is 20 MHz.

The operation of the controller IC has been verified prior to fabrication with postlayout simulations using Cadence Virtuoso, where the IC connects to a 4:1 STC converter with a 48 V input voltage feeding a resistive load of 0.3 Ω. The power stage as well as all peripheral circuitry (ZCD sensors, SD modulator, etc.) have been added to the simulation based on the components used in the experimental setup (discussed next). A transition from late-switching open-loop operation to closed-loop ZCS operation is simulated and verified as shown in Fig. 22. The zoomed-in view of Fig. 22(b) indicates that in the case of late-switching the voltage at the switching node, V_{sw2}, is clamped as discussed in Section IV and accurately indicates the polarity of the resonant current at turn-OFF. The zoomed-in view of Fig. 22(c) shows that once the closed-loop operation is enabled, ZCS is achieved within several cycles. Average dissipated power of the controller core has also been extracted from the postlayout simulations and equals 250 μW, with negligible current drawn when the controller is not enabled.

To demonstrate the operation of the controller IC and to further investigate the capabilities of the main control units developed in this article, a full-scale hardware prototype of a 650 W 4:1 STC as well as all required peripherals for the controller operation have been designed, built and tested. The experimental PCB with the connection to the controller IC is as shown in Fig. 21(b). The experimental STC hardware has been designed on a 14-layer PCB and it is rated for 650 W. The effective board area of the 4:1 power stage is 5 cm $\times$ 2 cm. The resonators have been designed symmetrically with equal resonant frequency. The components' parameters and values are detailed in Table I. An effort has been made to choose components' values in accordance with recent publications of STC related studies to verify the effectiveness of the controller when integrated into state-of-the-art STC systems.

Fig. 23 demonstrates the controller's lock-in capabilities for the symmetrical designed 4:1 STC. Here, the input voltage of the converter is 24 V due to current probe limitations. Once the controller is enabled, the output voltage rises, which is a direct indication for the increased charge transfer rate achieved by reaching ZCS of both resonators. Shown in Fig. 23(b) and (c) is zoom-in on the resonant currents and the switching nodes' voltages during late-switching [see Fig. 23(b)] and ZCS

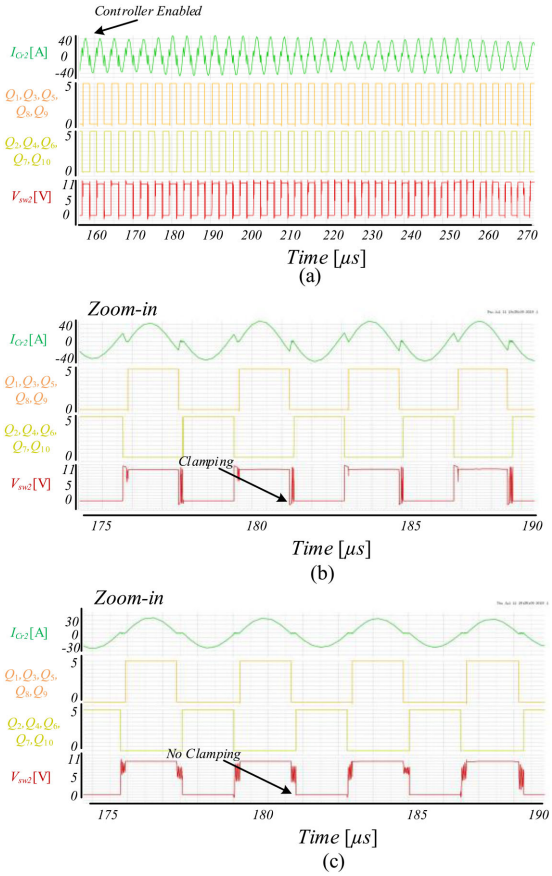


Fig. 22. Postlayout simulations controller IC for a 4:1 STC. (a) Transition from late-switching to ZCS. (b) Zoom-in during open-loop operation. (c) Zoom-in after convergence to ZCS operation.

TABLE I
EXPERIMENTAL PROTOTYPE VALUES AND PARAMETERS

Component	*Value*
Input voltage V_{in}	48V
Output power	650W
Resonant capacitor C_{r1}, C_{r2}	2.35μF
Resonant inductor L_{r1}, L_{r2}	70nH
Flying capacitor C_f	40μF
Q_1-Q_4	40V/2.5mΩ
Q_5-Q_{10}	25V/1.3mΩ

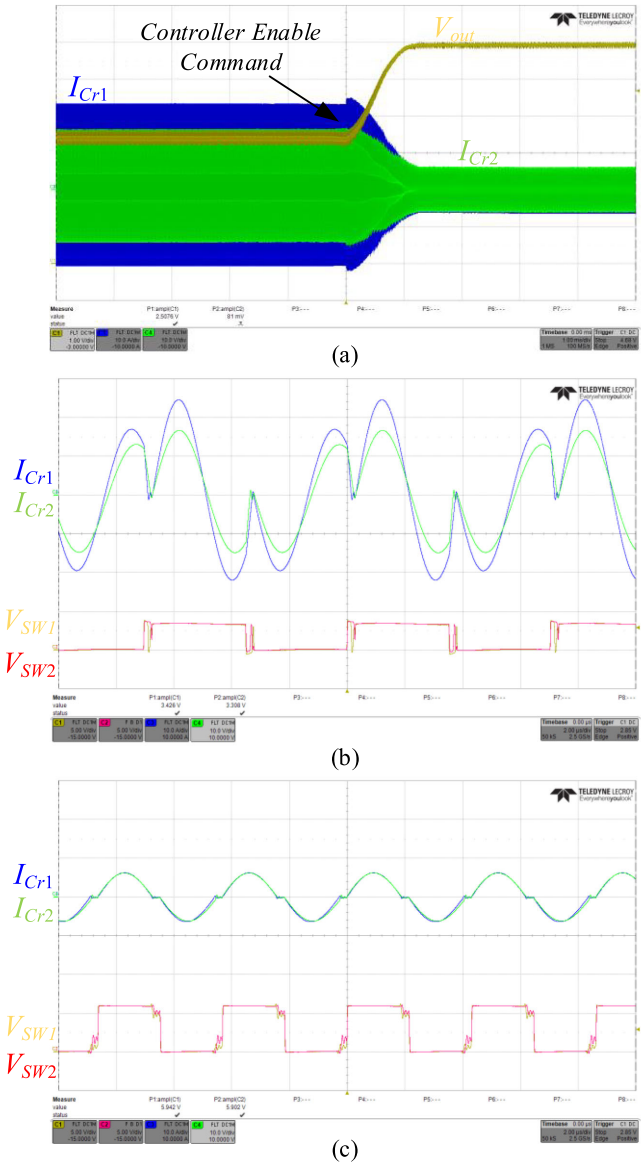


Fig. 23. Experimental results of a 4:1 STC's transition from open-loop late-switching to ZCS by the digital lock-in controller: (a) Full view of the tanks' currents and the output voltage. (b) Zoom-in view during open-loop operation on the tanks' currents (I_{cr1} – blue, I_{cr2} – green) 10 A/div, switching nodes (V_{sw1} – yellow, V_{sw2} – red) 5 V/div, time scale 2 μs/div. (c) Zoom-in view during ZCS closed-loop operation on the tanks' currents (I_{cr1} – blue, I_{cr2} – green) 10 A/div, switching nodes (V_{sw1} – yellow, V_{sw2} – red) 5 V/div, time scale 2 μs/div.

[see Fig. 23(c)]. As can be seen, the clamping of the switching nodes' voltages occurs only when the converter does not operate in ZCS. The enable command in this experiment, as well as in all other cases is randomly given to the controller and the switching frequency prior to the enable command is arbitrarily chosen and does not affect the controller's ability to converge to accurate ZCS operation.

Experimental waveforms are depicted in Fig. 24, for closed-loop operation of the system with deliberate mismatch between the resonant tanks component values ($C_{r1} = 2.62$ μF, $L_{r1} = 70$ nH, $C_{r2} = 2.35$ μF, $L_{r2} = 50$ nH). Fig. 24(a) shows smooth transition from open-loop early-switching operation to ZCS of both resonant tanks. A zoomed-in view of the resonant currents as well as the switching nodes is shown in Fig. 24(b) and (c). As can be seen, the ON-time for each resonant tank is set individually according to its resonant characteristics. In addition, the clamping of the switching nodes' voltages to $V_{\text{out}} + V_F$ is eliminated once ZCS is achieved.

Fig. 25 shows efficiency curves as a function of the load under tuned and untuned conditions for an input voltage of 48 V and

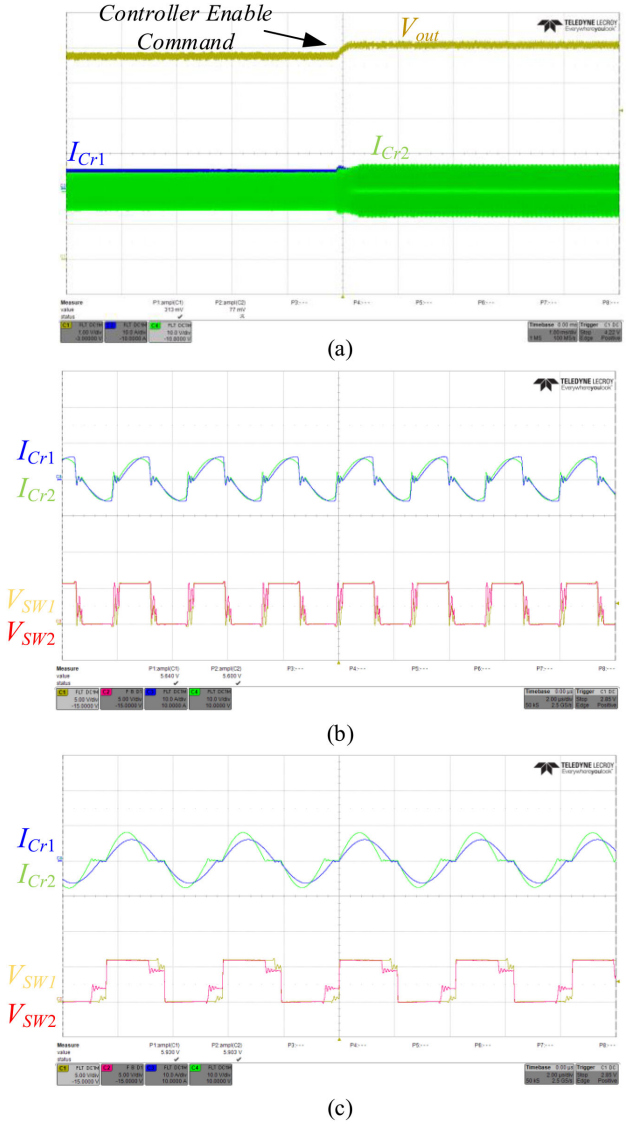


Fig. 24. Experimental results of a 4:1 STC's transition from open-loop early-switching to ZCS by the digital lock-in controller. (a) Full view of the tanks' currents and the output voltage. (b) Zoom-in view during open-loop operation on the tanks' currents (I_{cr1} – blue, I_{cr2} – green) 10 A/div, switching nodes (V_{sw1} – yellow, V_{sw2} – red) 5 V/div, time scale 2 μs/div. (c) Zoom-in view during ZCS closed-loop operation on the tanks' currents (I_{cr1} – blue, I_{cr2} – green) 10 A/div, switching nodes (V_{sw1} – yellow, V_{sw2} – red) 5 V/div, time scale 2 μs/div.

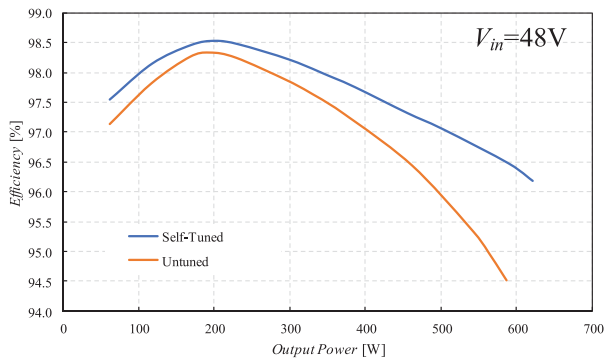


Fig. 25. STC efficiency under tuned and untuned conditions.

include drive and controller losses. The average dissipated power of the controller core has been extracted from postlayout simulation under various corner conditions and results in 250 μW. As can be seen, when the lock-in controller tunes into the resonant characteristics of the converter, the efficiency is above 97% for most of the load range and reaches peak efficiency of 98.6%. The efficiency curves of Fig. 25 demonstrate the importance of operating in ZCS, especially for high loads where rms and core losses are eminent.

VII. Conclusion

A lock-in integrated controller architecture that facilitates accurate switching timing for single or multistage RSCC based topologies has been presented. The controller adjusts to accommodate any mismatch, variations, or drifts of component values or circuit configuration, and performs tuning for each resonator independently to fully utilize the charge transfer for each flying capacitor in the system. A full-scale hardware prototype of 650 W 4:1 STC has been used to validate the controller's operation, demonstrating excellent lock-in capabilities, and high efficiency of up to 98.6%. The fully digital controller IC has been designed and fabricated in a 0.18 μm 5 V process by pure digital means, resulting in effective silicon area of 0.64 mm^2. Experimental results of the closed-loop operation demonstrated accurate tuning for two resonators with individual independent resonant characteristics.

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