Adaptive Self-Tuned Controller IC for Resonant-Based Wireless Power Transfer Transmitters

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***Abstract*—This article introduces an adaptive self-tuned controller IC for resonant wireless power transfer (RWPT) transmitters. The controller IC comprises an on-the-fly very-high-frequency tracking hardware with high resolution and an independent high-resolution digital pulsewidth modulator (PWM)-based (HR-DPWM) current programmed control. These facilitate precise frequency generation as well as adaptive tuning of the reactive components in the matching network, which translate into tight current/power regulation capabilities while retaining optimized power transfer conditions on the transmitting side. The controller IC enables to effectively disengage the power-delivery capabilities from the variations of the resonators, electrical circuits, and wireless medium. The controller core is based on a fully synthesizable digital architecture that has been realized through HDL tools, and several key building blocks have been developed and described in detail: a delay-line-based phase detector, high-resolution digital frequency synthesizer, and HR-DPWM. To fully exploit the benefits of digital electronics, reduce power consumption, and save area, the digital core of the controller has been designed completely through asynchronous architecture, eliminating the need of high-speed clock and its related hardware. The mixed-signal controller IC has been designed, implemented, and fabricated in 0.18-μm 5-V CMOS process, resulting in effective silicon area of 0.6 mm^2. To demonstrate the mixed-signal controller IC in closed-loop operation of a wireless power system, an experimental 20-W resonant capacitive-based WTP system has been designed and validated. The effectiveness of the controller is well demonstrated and evaluated at the MHz range up to 200 mm misalignment, meeting the strict requirements of resonant-based WPT systems.**

***Index Terms*—Adaptive controller IC, closed-loop wireless system, impedance matching, resonant power transfer, self-tuned transmitters.**

I. Introduction

OVER that last decade, there has been an increasing interest in the rapidly growing field of wireless power transfer (WPT) technology, which is developing into a standard feature in many daily-used applications [1]–[5]. WPT technology is the main enabler to cut the last cord, and to reduce the significant dependency of volume-sensitive portable applications on embedded bulky batteries as a reliable main source of energy [6]–[8]. Inductive power transfer (IPT) is a well-known near-field WPT method, and it is the most adopted technique in commercial WPT applications due to its simplicity, reliability, and safety [4], [9]–[11]. Another near-field method is capacitive power transfer (CPT) that is potentially with better efficiency characteristics, lower volume, and construction complexity [12]–[17].

A main bottleneck of both IPT and CPT methods is that the power transfer capability and efficiency highly depend on the distance and alignment between the transmitter and receiver [7], [14], [18]–[21]. To achieve better power transfer characteristics, resonant high-frequency operation, typically in the range of multi-MHz, is utilized in WPT systems [16], [17], [22]–[31]. This is essential to compensate for the relatively low coupling of the wireless medium, enhance the transmission range, and achieve reasonable efficiency. In addition to improved spatial freedom, resonant wireless power transfer (RWPT) systems can provide energy to multiple devices with different power requirements simultaneously [24], [29], [31]. Typically, RWPT systems rely on fixed-frequency operation combined with LC-based matching networks [17], [30]–[34]. This alone, however, is not sufficient since in practice, the resonant characteristics are affected by the medium interface (even for loosely coupled systems), changes in environment, component aging, and temperature drifts, which dramatically decrease the power transfer capabilities and stability of the system. Adding the fact that typically such RWPT systems consist of a high-Q resonator, frequency mismatch results in large drop in the system performance [35], [36].

Several methods to achieve resonant frequency control for RWPT have been reported in the literature [37]–[49]; tunable impedance matching techniques have been widely adopted in RWPT to adjust the resonant characteristics to a target fixed frequency [37]–[40]. To obtain fine-tuning of the matching networks, in particular at high frequencies, considerable amount of passive components and bi-directional switches is required, and thus, the overall system is quite complex and bulky [38]–[40]. Automated frequency tracking method has also been utilized in RWPT [41]–[49]. Several studies employed frequency tuning by maximum power point tracking [41]–[44]. There, the controller

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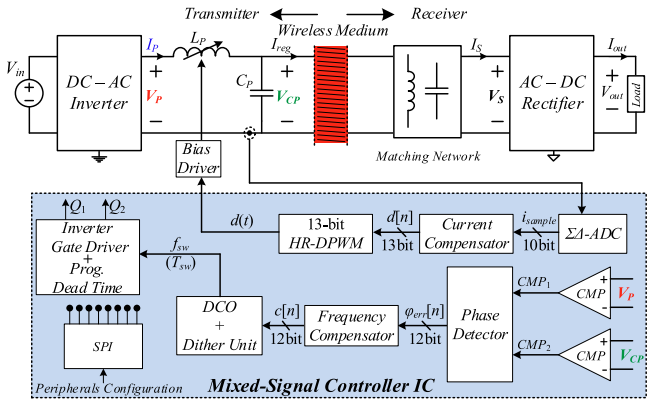

Fig. 1. Simplified schematic diagram of a WPT system with the adaptive self-tuned mixed-signal controller IC.

seeks for the peak power which is obtained at resonance, and tunes the operating frequency accordingly. The latter provides flexibility in power regulation, but comes at the cost of potential slow dynamics of the system and potential degradation of the overall efficiency. Another technique for automated frequency tuning has been utilized based on phase detection [45]–[49]. Although reasonable dynamics can be obtained, this approach introduces a major tradeoff between frequency resolution and operation range. This can be improved by custom-designed analog-oriented ICs with tailored phase locked loop (PLLs) and accurate high-frequency generation; however, the design efforts, die area, and overall power consumption significantly increase. On the other hand, digital-oriented architectures are very attractive in terms of design efforts and integration [26], [50]. The main limiting factor of digital-based frequency synthesizers is that commonly used field-programmable gate array (FPGAs), microcontrollers, and other digital platforms provide time-resolution on the order of several hundreds of picoseconds up to nanosecond [50]–[53]. Therefore, to obtain wide range high-frequency operation while maintaining a high-resolution, without significant penalty on power consumption and silicon area, *dedicated ASIC with specifically tailored hardware that can be realized through a simple design flow is required*—this has been pursued in this study.

The objective of this study is, therefore, to introduce an adaptive high-frequency, high-resolution self-tuned controller IC (Fig. 1) for resonant-based WPT systems that have been developed on the basis of all-digital standard-cell approach. The new controller IC relies on continuous tuning of the operating frequency to the resonant one, regardless of system variations and components drifts. It should be noted that although existing closed-loop methods enable to overcome some system variations and to extend the power delivery range (power levels and distance), a single control method is not always sufficient to guarantee reliable power delivery of WPT systems, particularly for dynamic WPT systems. Several works on the topic of multiple control loops have been investigated [40], [47], [54], and demonstrated the effectiveness of a multiloop controllers in the context of wireless power. Therefore, it is a further objective of this study to realize a digital architecture for controlling a continuous self-tuned variable inductor that is not based on relays or semiconductor switches, which enables a high degree of freedom on power regulation in the transmitter. The mixed-signal IC architecture is based on two independent control loops that include the following key building blocks: wide-range high-resolution phase detector, high-resolution digital controlled oscillator (DCO), digital pulsewidth modulator (DPWM) for the bias driver of the variable inductor, custom-designed sigma-delta analog-to-digital converter (SD-ADC) programmable dead-time unit, and a serial communication interface (SPI).

The rest of the article is organized as follows. Following a brief survey of L-type resonator, Section II describes the principle of operation of the mixed-signal controller IC and details its algorithm. Section III details the architectures for the main units of the mixed-signal controller IC. System-level considerations with emphasis on limit-cycles oscillations and frequency resolution are delineated in Section IV. Experimental and postlayout verification of the controller IC are provided in Section V. Section VI concludes this article.

II. Control of RWPT Transmitters

A. Network Review of L-Type-Based Resonator

The principle of operation of the adaptive RWPT controller IC is described here, without losing generality, through a L-type series-parallel (*LC*) matching network [15], [17], [32] as delineated in Fig. 1. It should be further emphasized, that the core of the control algorithm is applicable for various near-field resonant-based WPT configurations. Assuming loosely coupled operation [13]–[15], [30], the drive frequency, f_{sw}, is near the matching networks' resonant frequency (i.e., $f_0 = 1/(2\pi\sqrt{LC})$), then the currents as well as voltages of the passive components are virtually sinusoidal [55]. This is since high-Q operation is naturally facilitated as the effective output impedance of the LC matching network in the transmitter is relatively high. Fig. 2 depicts typical waveforms of resonant L-type-based transmitters. For a full-bridge dc–ac inverter as the front-end, the inverter voltage, V_P, toggles between $V_{\rm in}$ and $-V_{\rm in}$, whereas, for a half-bridge configuration, V_P toggles between 0 and $V_{\rm in}$. In both configurations, the sinusoidal current, I_P, is in phase with V_P; additionally, it can be also seen that at resonance, the phase difference between V_P and the sinusoidal voltage across the matching capacitor, V_{CP}, is 90°.

B. Variable Inductor Realization

The variable inductor employed in this study is inspired by the prior art of [56], [57]. The structure comprises an *E*-core type magnetic element with the primary inductor on the middle, gapped leg, whereas the bias/control windings are formed on the outer, non-gaped legs [Fig. 3(a)]. If the ac component of the inductor's is small enough, so that the permeability change due to the current variations is negligibly small, the inductance value *L* can be estimated with the aid of several design parameters such as number of turns *n*, air-gap length l_g, and the effective magnetic path length l_e. Hence, the inductance *L* as a function of the bias

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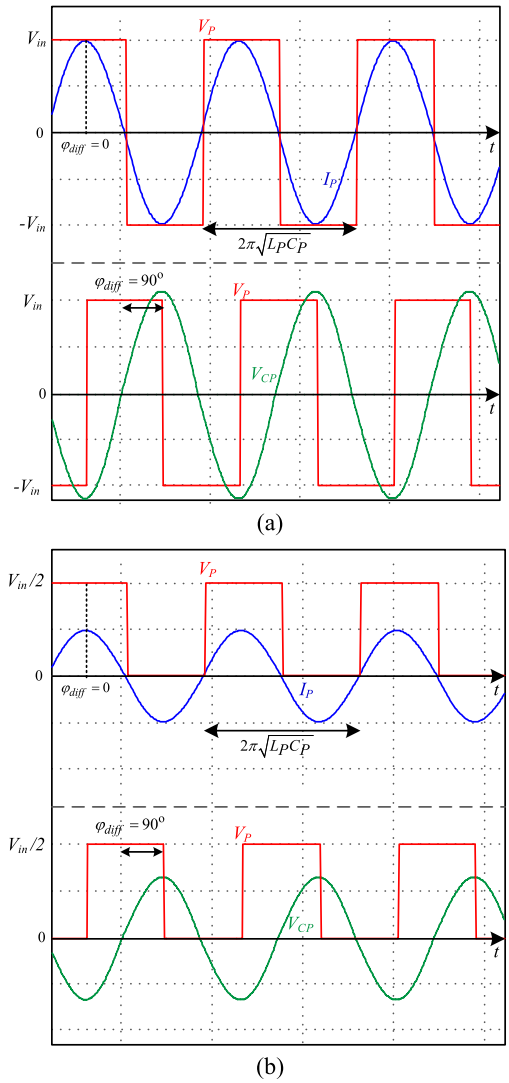

Fig. 2. Typical waveforms of an L-type based WPT transmitter operating at resonance driven by (a) a full-bridge inverter, and (b) a half-bridge inverter.

current-dependent permeability can be expressed as

$$L = \frac{n^2 \mu_0 A_e}{l_e} \frac{\mu_r(I_{\rm Bias})}{1 + 2\frac{l_g}{l_e}\mu_r(I_{\rm Bias})} \tag{1}$$

where μ_0 is the air permeability, $\mu_{\rm r}$ is the magnetic core permeability, and A_e is the core area. $\mu_{\rm r}$ depends on the bias current $I_{\rm Bias}$ and can be obtained from either the manufacturer data or by experiment [58], [59]. A simplified expression of $\mu_{\rm r}$ is given by

$$L = \frac{n^2 \mu_0 A_e}{l_e} \frac{\mu_r(I_{\rm Bias})}{1 + 2\frac{l_g}{l_e}\mu_r(I_{\rm Bias})} \tag{2}$$

where μ_{mi} is the permeability initial value, i.e., $\mu_{\rm mi} = \mu_{\rm r}$ $(H = 0)$, $H_{\rm pole}$ is the magnitude of the saturation field, and j sets the permeability slope. The variable H represents magnetic field strength, which is linearly proportional to the bias current.

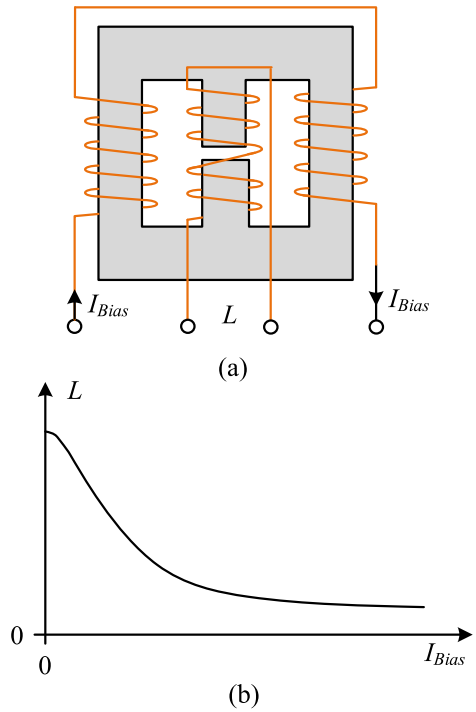

Fig. 3. (a) Variable inductor practical implementation. (b) Relationship between the inductance value and the bias current.

The relationship between H and $I_{\rm Bias}$ is as follows:

$$H\left(I_{\rm Bias}\right) = nI_{\rm Bias}/l_e. \tag{3}$$

It should be noted that the main inductor current, in the applications considered in this study (resonant type conversion), has a high ac component. Consequently, the core permeability changes over the switching cycle, which may result in distortion of the current sinusoidal shape. Since such matching networks, particularly in the context of RWPT, are designed with high-quality factor and are operated in the near vicinity of the resonant frequency, the high-frequency components are filtered out. Hence, the effective inductance as a function of the bias current can be approximated as illustrated in Fig. 3(b).

C. Controller Operation

Following the observations made in the previous sections, an adaptive controller that monitors, tunes, and enables to continuously keep the system at optimal power transfer conditions is addressed. The controller operation is facilitated by two major control loops as shown in Fig. 1. The adaptive tuning operation is performed independently per feedback loop, with its respective objective and rate. The first loop resembles in structure to a DCO that synthesizes a switching frequency, f_{sw}, which continuously follows the resonant frequency, f_0, even under variations of the system parameters. This self-driving concept ensures in WPT system, that the power conversion and transfer characteristics of the transmitter are optimized. The second control loop comprises a current compensator and a tuning unit, that adjusts the

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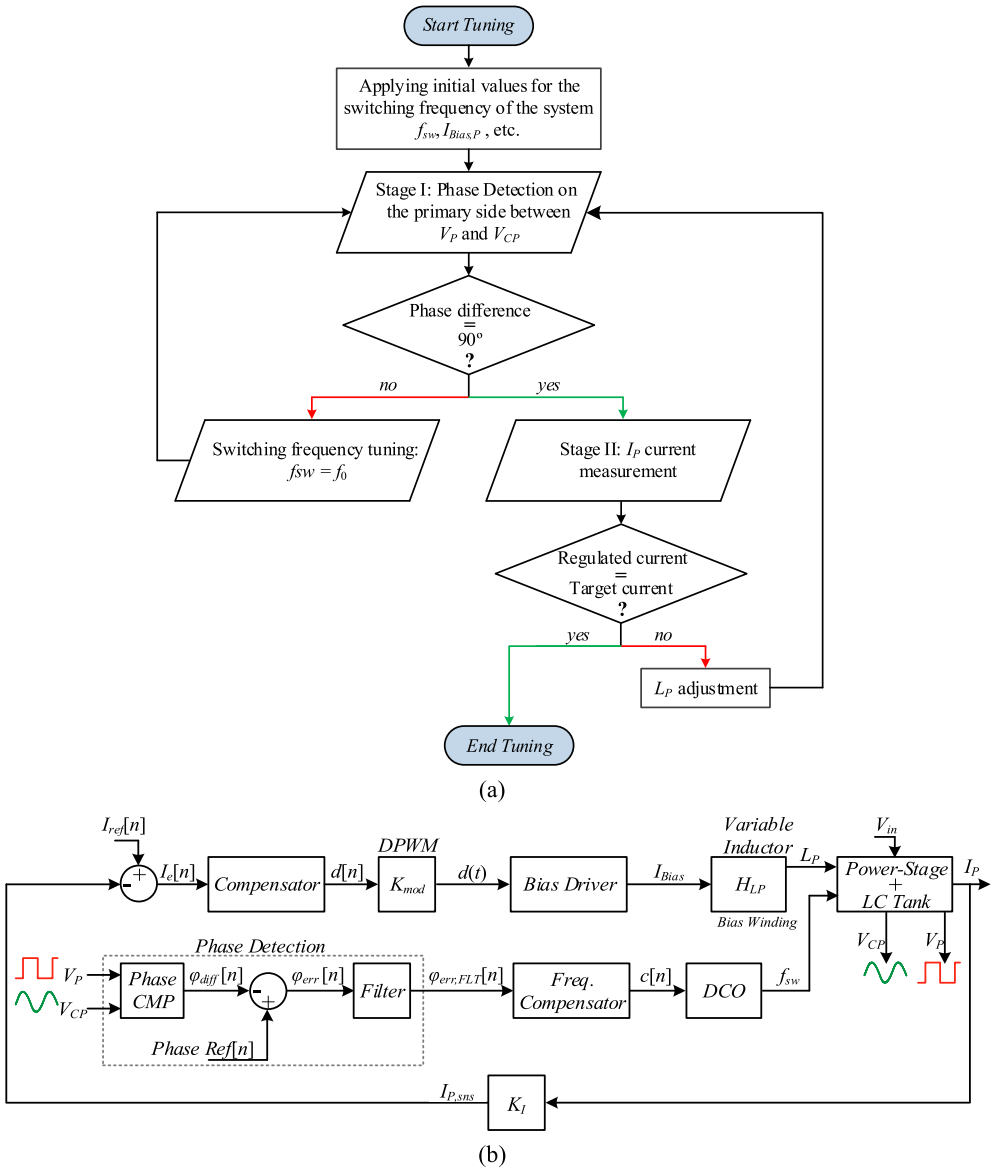

Fig. 4. (a) Tuning procedure flowchart of the controller IC. (b) Functional signal flow diagrams of the controller IC.

inductance value of L_P, such that a target current (as well as power) is regulated from the transmitter side to the wireless medium. This transforms the transmitter side into a self-tuned architecture, in which the drive frequency tracks the resonant frequency on-the-fly, and the transmitted power is regulated by adjusting the resonant network's characteristics. It should be noted that the control loops can operate independently to facilitate specific objective out of the controller.

The principle of operation of the new mixed-signal controller IC that has been realized in this study is described with the aid of Fig. 4, which shows a high-level flowchart of the tuning procedure utilizes the control loops and a functional block diagram of the controller, respectively. Since the controller IC should function as a stand-alone module, the hardware architecture includes a small volatile memory, as a part of the serial communication interface (custom-designed SPI) that is preprogrammed with a set of default values for the main parameters of the controller. On startup, the default values can be used or a new set can be loaded to the controller through the SPI. Then, the SPI internally communicates with the main units and loads the set of values per block. A benefit of this embedded feature is that the same controller hardware can be used with different power stages, matching network configurations, and parameters.

Upon initiation of the tuning procedure (Fig. 4), a default set of preloaded values are used to determine the switching frequency, f_{sw}, variable inductor, compensators parameters, etc. The inner feedback, which is the fastest loop, applies frequency tuning. There, the switching frequency, f_{sw}, to drive the dc–ac inverter is being varied by the DCO unit to match the resonant frequency of the circuit f_0. This is facilitated by measuring the voltages V_P and V_{CP} (Fig. 1), extracting the phase difference between them, and adjusting f_{sw} until the phase difference between the

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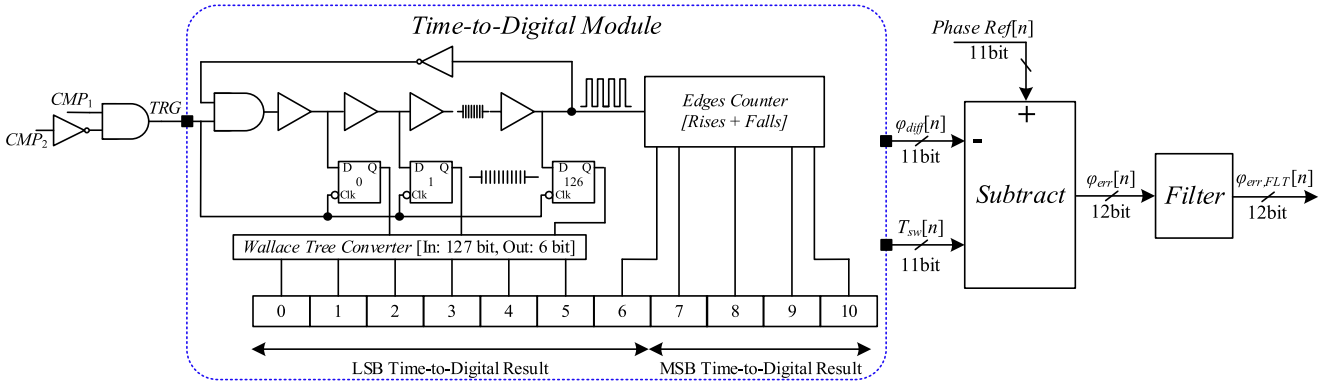

Fig. 5. Schematic diagram of the high-resolution phase detector.

signals reaches 90°. In the case that the detected phase difference between the signals is not 90°, an error signal is generated to the DCO, which in turn synthesizes new switching frequency until $f_{sw} = f_0$. In the next stage of the tuning operation, the transmitter's current, I_P, is sensed and compared to a target/reference one (Fig. 1), which is predefined by the SPI unit. It should be noted that for WPT system with multiple loads, it is essential that the controller is able to maintain constant current operation [77]. The correction signal that is generated is used to vary the inductance L_P through a bias winding until the required current is achieved. This variation of the inductor value is realized by a buck converter current driver that applies dc bias to nongapped side windings of the inductor as described in the previous subsection. Due to the variation of the inductance value, the resonant characteristics of the transmitter change, and potentially move the system out of its optimized transfer conditions. As a result, the frequency-tracking loop needs to search again and lock the switching frequency into the resonant frequency.

III. Adaptive RWPT Controller IC Architecture

The realization of the adaptive mixed-signal controller IC relies on three key enabling blocks: 1) 11-bit high-resolution wide-range phase detector; 2) 12-bit enhanced dither-based high-resolution DCO; and 3) 13-bit high-resolution DPWM (HR-DPWM) that generates gate drive signal for the bias current driver of the variable inductor. Each of the fundamental units has been implemented as an asynchronous hardware, using delay-lines (DL) [60], [61] and combinatorial circuits. By doing so, a significant portion of complex and power-hungry hardware for timing and high-speed synchronization is eliminated. Since some of the units are still based on a synchronized process, a system governor is employed to provide time-base to the switching cycle and trigger the sequential operation of the functional blocks within the switching cycle.

A. Phase Detector

Accurate wide-range phase detection is one of the key factors to achieve high-performance frequency control in RWPT systems. Thus, conventional methods for phase detection which consists of type-I detection circuit, i.e., comparators as digitizers and an exclusive-or (XOR) phase comparator [62], are not sufficient since they have narrow dynamic range of operation; additionally, there is no direct information whether the phase difference is positive or negative.

The phase detector in this study is based on a time-to-digital conversion using a DL string built of digital buffers with fixed propagation time [50], [60], [61], as shown in Fig. 5. The phase difference is translated by the time difference between the signals CMP_1 and CMP_2 (which are the digitized representations of V_P and V_{CP}), and obtained by combination of few basic operators (Fig. 5). The signal, *TRG*, triggers the DL string and starts the conversion process, such that seven LSBs of the output registers are a direct Wallace-Tree translation [50] of the DL. A counter, triggered both at rising and falling edges, is connected to the end of the string to count the repetitions of full DL string propagations; the result is conjugated as the five most significant bit (MSBs) of the output register. Once *TRG* returns to low logic level, the counter holds the number of cycles that the DL propagates throughout the pulsewidth of *TRG*, while the DL holds the residual time difference with higher time resolution, due to the partial propagation of the last run. An 11-bit result of the phase difference, $\varphi_{\rm diff}[n]$ is generated together with $T_{sw}[n]$, which represents the switching period (time representation of 360° phase range) with respect to the operating frequency of the system. This is essential, since the phase difference and the phase reference must be normalized to the time base of the synthesized operating frequency. The phase error, $\varphi_{\rm err}[n]$, is obtained by subtraction between the phase reference and $\varphi_{\rm diff}[n]$, where the MSB of $\varphi_{\rm err}[n]$ is a sign bit. Finally, to obtain noise-clean phase error signal as much as possible, $\varphi_{\rm err}[n]$ is filtered.

It should be further noted that, since the voltages of the resonator are significantly higher than the operation voltage levels of the controller and other electronics periphery, the voltages V_P and V_{CP} are scaled down using high-impedance attenuation circuit to voltage levels suitable for logic gates input such as the phase detector unit. From practical implementation perspective, if a simple resistive divider is used, the input capacitance of the logic gate introduces phase delay between the actual zero-crossing point and the digital signal transition. In the case that the phase shifts of the two measured signals are different (due to different resistive path), a systematical offset exists, and should

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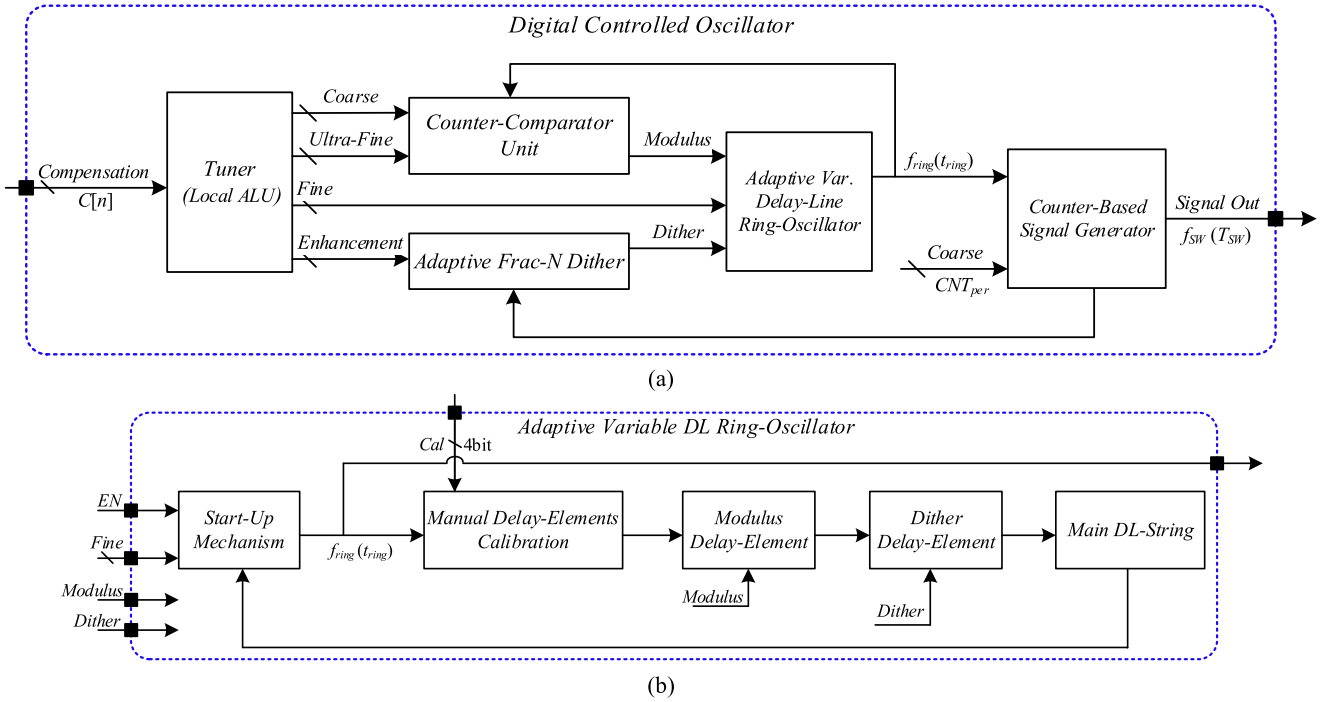

Fig. 6. (a) Block diagram of the DCO. (b) Simplified block diagram of the adaptive variable ring-oscillator.

be calibrated out. This can be solved by setting the phase reference slightly higher (or lower) than the target one, compensating for undesired offsets due to the voltages sensing paths. Another approach to minimize phase offset errors is to employ similar voltage scaling for both measured signals as much as possible; however, this might be impractical in high-voltage gain systems. At such cases, active attenuation circuits as well as adaptive calibration are required.

B. High-Resolution Digital Controlled Oscillator

The core of the DCO in this study is based on an adaptive variable ring-oscillator combined with counters-comparator units as delineated in Fig. 6(a) [63]–[65]. To obtain both wide range and high-frequency operation while maintaining a single delay-cell resolution, without sacrificing overall efficiency and silicon area, the DCO's output signal is generated based on coarse, fine, and ultrafine-tuning concept of the ring-oscillator. The coarse-tuning (also denoted as $CNT_{\rm per}$) defines how many ring-oscillator cycles are needed for generating the output period. Next, fine-tuning value controls the delay ring size, i.e., how many extra delay elements should be added to the basic ring-oscillator string to improve the resolution. Finally, ultrafine value defines how many ring cycles should have an additional delay element within the output period. Based on the ultrafine and coarse signals, a counter-comparator unit is responsible for enabling the additional delay. For a case in which finer resolution of the output signal is further required, a frequency dithering feature [66]–[69] has been embedded in the DCO. The enhancement signal defines and enables to add extra delay element to the ring-oscillator string [see Fig. 6(b)], further improving the resolution of the output period, effectively finer than a single-cell resolution.

The DCO in this study has been designed to generate frequencies between approximately 1 and 10 MHz, and the general frequency relationships of the DCO can be expressed as follows:

$$f_{\rm ring} = \frac{1}{\underbrace{Nt_{DE}}_{t_{\rm ring}}} \Rightarrow f_{sw} = \frac{f_{\rm ring}}{CNT_{\rm per}} = \frac{1}{CNT_{\rm per}t_{\rm ring}} \tag{4}$$

where $f_{\rm ring}$ is the frequency of the ring-oscillator, t_{DE} is the delay of a single delay-element within the ring-oscillator, N is adjustable overall number of the delay elements in the ring, and CNT_{per} is an integer that represents the coarse value of the counter for generating the target output frequency f_{sw} (period-T_{sw}). It should be noted that, due to possible process, voltage, and temperature (PVT) variations, and other potential postfabrication mismatches, $t_{\rm ring}$ can be also manually calibrated by adding/removing delay elements within the ring-oscillator [see Fig. 6(b)]. The frequency resolution of the DCO, $f_{\rm res}$, can be calculated as the LSB change in $CNT_{\rm per}$

$$\begin{aligned} f_{\rm res} = \Delta f_{sw} &= \frac{1}{CNT_{\rm per}t_{\rm ring}} - \frac{1}{(CNT_{\rm per}+1)\,t_{\rm ring}} \\ &\approx \frac{1}{CNT_{\rm per}^2 t_{\rm ring}} = t_{\rm ring}f_{sw}^2. \end{aligned} \tag{5}$$

From (5), it can be observed that the frequency steps of the DCO are limited by the module's base frequency, and increase as the square of the operating frequency, i.e., at lower operating frequency, the frequency resolution would be finer than what can be achieved at a higher frequency.

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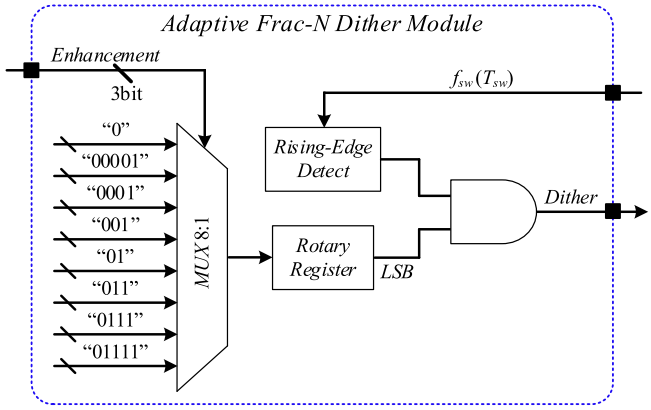

Fig. 7. Block diagram of a 3-bit Frac-N dithering module.

Since finer resolution is desired over the entire operating range, an effective, fast dynamics and low distortion, frequency enhancement dithering procedure has been employed. An adaptive 3-bit Frac-N dithering method (Fig. 7) is facilitated by dithering the DCO between $CNT_{\rm per}$ and $CNT_{\rm per}+1$ at a defined rate, varied by the required accuracy. The dither factor, n, is the number of DCO cycles needed to achieve the desired fractional frequency. Dithering is accomplished by keeping a constant period over $(n-1)$ DCO cycles (referred as base period) and then changing the last slot (n) to another period. The resultant (average) frequency using this method can be calculated by a general expression as follows:

$$f_{sw\_dither} = \frac{1}{[(n-1)\,CNT_{\rm per} + (CNT_{\rm per}+1)]/nt_{DE}} = \frac{1}{\left(CNT_{\rm per}+\frac{1}{n}\right)t_{DE}};\; n = 1,2,3\ldots \qquad (6)$$

and the enhanced frequency resolution

$$f_{res\_dither} = \frac{1}{\left(CNT_{\rm per}+\frac{1}{n+1}\right)t_{DE}} - \frac{1}{\left(CNT_{\rm per}+\frac{1}{n}\right)t_{DE}} \approx \frac{1}{n\,(n+1)\,CNT_{\rm per}^2 t_{DE}} = \frac{t_{DE}{f_{sw}}^2}{n\,(n+1)}. \qquad (7)$$

Fig. 8(a) shows an illustrative example for a frequency fraction of 0.25 $f_{\rm res}$; there the DCO generates one ($CNT_{\rm per}+1$) period every fourth cycle. Additionally, Fig. 8(b) shows a comparison between ideal infinite frequency states, Frac-N dithering method for a 3-bit frequency resolution enhancement (i.e., eight additional frequency fractions between two base DCO values), and a typical DCO operation.

C. High-Resolution Digital Pulsewidth Modulator

To accurately control the variable inductor and to avoid undesired oscillations, a high-resolution modulator is required. The conventional approach to implement HR-DPWM is by a fast-clocked counter-comparator scheme [64], [65]. In this way, n-bit resolution at a switching frequency of $f_{\rm bias}$ requires a reference clock frequency of $2^n \cdot f_{\rm bias}$. This translates to increased

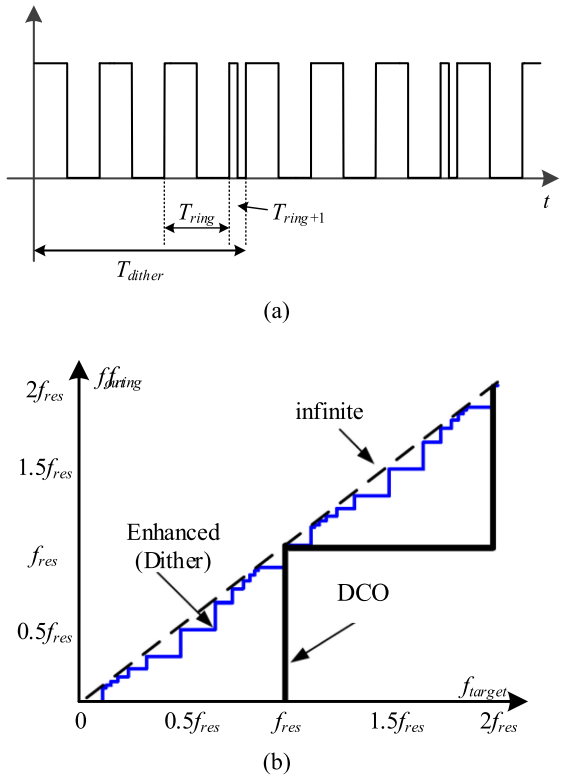

Fig. 8. (a) Dithered output signal with frequency fraction of $0.25f_{\rm res}$. (b) Output frequency versus desired frequency for typical DCO and 3-bit resolution enhancement.

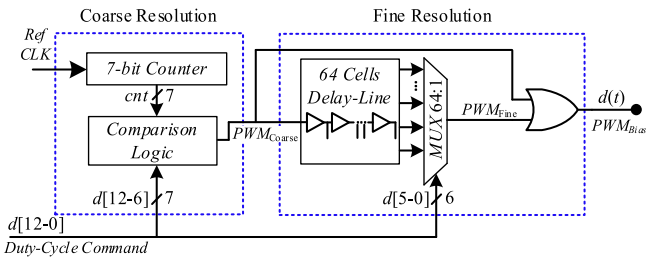

Fig. 9. Simplified architecture of the 12-bit HR DPWM.

power consumption and more complex design to realize the high-speed circuitry. Another approach to realize a HR-DPWM is based on tapped DL scheme [60], [61]. In this method, the power consumption is reduced, but the required silicon area of the design grows exponentially with the number of resolution bits.

The HR-DPWM presented in this article has been realized based on a combined coarse–fine digital counter concept [50]. Fig. 9 shows the conceptual architecture of the unit. As can be seen, it comprises two main functional units: counter-based coarse resolution PWM generator and fine-tuning delay chain combined with an OR operator. The 13-bit digital word for the duty-cycle command d[12-0] is distributed within the units. The coarse resolution PWM block is fed by a reference clock (generated by the system governor) which is being counted and compared with seven upper bits of the duty-cycle command

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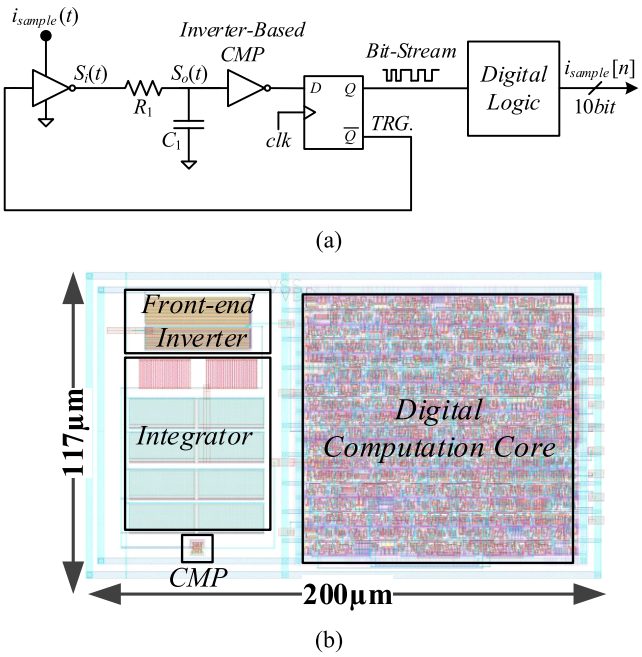

Fig. 10. (a) SD-ADC architecture. (b) Layout of the SD-ADC.

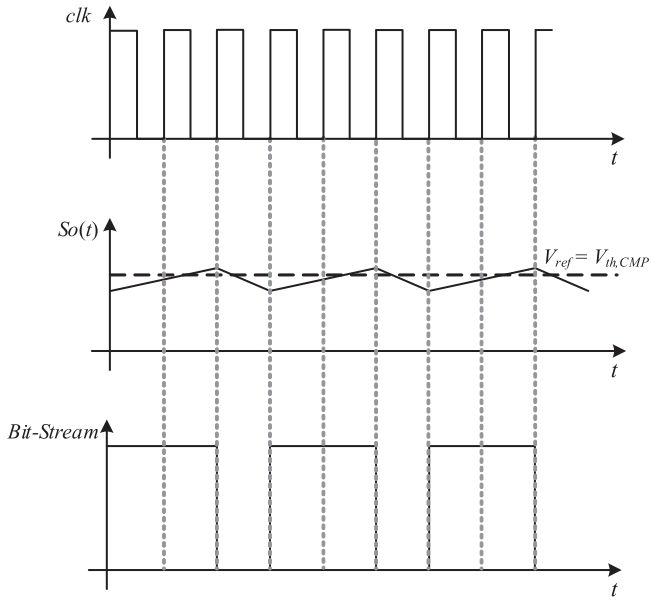

Fig. 11. Typical waveforms of the SD-ADC.

d[12-6]; the resulting signal PWM_{Coarse} can be expressed by

$$PWM_{\text{Coarse}} = \begin{cases} d[12-6] > cnt[6-0], 1 \\ d[12-6] < cnt[6-0], 0. \end{cases} \tag{8}$$

The fine-resolution PWM unit generates a string of 6-bit long DL that finely adjusts PWM_{Coarse} by the number of delay elements as specified by d[5-0]. The latter combined with the OR operator generates the high-resolution PWM output signal, $d(t)$. The switching frequency of the HR-DPWM, f_{bias}, can be expressed as function of the number of bits and the propagation time of a single delay element t_{DE} (of the fine-delay module) as

$$f_{\text{bias}} = \frac{1}{t_{DE}2^{N+M}}; \begin{cases} N - \text{number of coarse bits} \\ M - \text{number of fine bits.} \end{cases} \tag{9}$$

D. Sigma-Delta Analog-to-Digital Converter

Analog-to-digital conversion of the current control loop is facilitated in this study by a Sigma-Delta ADC [70]. The SD-ADC has been realized with simplified hardware to reduce complexity, power consumption, and effective silicon area. As can be seen in Fig. 10(a), the modulator front-end is realized by a digital inverter, with i_{sample} as the high logic level (supply). The integrator is realized by a simple RC network with a corner frequency of at least one order of magnitude lower than the clock frequency. The quantizer is realized by a digital inverter-based configuration, whereas the result is then held by a D-type flip-flop to facilitate a clocked bitstream at the oversampling frequency of the ADC. Layout of the SD-ADC with overall dimensions is shown in Fig. 10(b). The implemented ADC may come at the cost of the conversion rate; however, since at resonant power conversion, in particular, at high-Q operation, the response of the system to variations is rather slow and carries on over several switching cycles, the overall architecture of the ADC suits well with the control specifications of the current loop.

The resultant SD-based ADC is a hardware-efficient voltage level translator, in which the average voltage at node $S_o(t)$can be expressed as

$$\overline{S_o(t)} = V_{\text{ref}} = i_{\text{sample}}(t)\frac{CNT}{2^n} \tag{10}$$

where V_{ref} is the reference value for the modulation process (the threshold voltage of the inverter-based comparator) and *CNT* is the number of logic-high occurrences in the bit stream for 2^n clock cycles. An illustration of the voltage at the input of the inverter-based comparator, $S_o(t)$, is shown in Fig. 11 along with the resultant bit-stream and the oversampling-clock. The bit-stream is the input to a computational digital logic which counts the number of "ones" (equals to *CNT*) with a dedicated counter which acts as a sinc LPF, and resets at predefined intervals to perform decimation. In this study, the sampled signal applied on the front-end inverter is translated to a digital representation every 1024 clock cycles, which results in a 10-bit representation of the measured current.

E. Programmable Dead-Time

Resonant-based WPT systems are typically designed at multi-MHz switching frequencies to reduce the overall size of the wireless link and passive components. In addition to shoot-through issues of the dc–ac inverters [71], maintaining zero-voltage switching (ZVS) while controlling the power delivery is of a great importance in such MHz range power conversion systems [72], [73]. Therefore, a programmable dead-time module has been developed and realized in the controller IC, making it more robust for various operating conditions. The dead-time unit consists a string of 256 delay elements connected to an 8-channels multiplexer as shown in Fig. 12. In a similar manner

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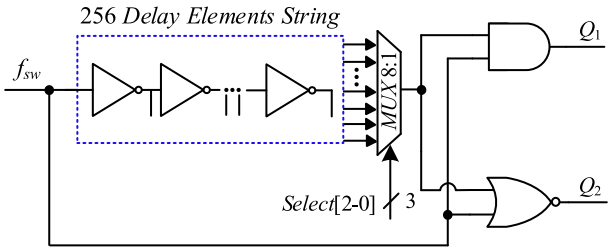

Fig. 12. Schematic diagram of a programmable dead-time module.

to the other predefined values, the dead-time period, t_{DT}, is set within the SPI memory register with initial default value, and can be programmed from approximately 5 ns up to 50 ns.

IV. System-Level Considerations

A. Limit-Cycle Oscillations in Digitally Controlled RWPT

A major practical issue that should be considered when designing closed-loop resonant-based WPT systems, and particularly digitally controlled RWPT, is limit-cycle oscillations (LCO). As originally presented in [66], [69], [74], the primary cause for steady-state oscillations is resolution mismatch of the DCO (assuming the compensators does not add quantization error) [66]. In addition to the operating-point-dependent gain that exists in resonant converters, the highest sensitivity to gain variations is located around the resonant frequency, a condition that becomes even further emphasized in resonant-operating WPT systems that operate with very high-quality factors. Since the controller targets optimal transfer conditions which are obtained at resonance (aside from slight deviation from the exact target frequency to facilitate ZVS), this calls for extremely sensitive calibration, i.e., fine frequency resolution generator at MHz range to facilitate LCO-free operation. Therefore, to ensure smooth high-frequency drive throughout the operation range (taking into account the worst-case conditions of the highest quality factor), the DCO in this study has been designed to achieve the required effective acquisition as well as control resolution such that limit-cycle oscillations are remedied. As discussed in Section III-C, frequency dithering has been embedded to enhance the drive frequency, and to provide effective frequency (over few cycles) with finer resolution than the base value. The effect of frequency resolution in resonant converter drives is depicted in Fig. 13, which is the simulated output response of a series-parallel resonator (L-type) driven by a typical 8-bit DCO and by the presented dithered-DCO with 3-bit resolution enhancement. In addition, slow-response characteristics of resonant networks due to high-Q also aid with LCO in the context of RWPT systems; since it takes the resonator several cycles to react to changes in the drive frequency, it is utilized as an averaging action. To demonstrate this characteristic, a cycle-by-cycle simulation at a resonant frequency of 4 MHz with steps of 5 kHz has been utilized. It can be observed from Fig. 14 that the convergence time, t_{step}, to ± 5 kHz step was approximately hundred switching cycles.

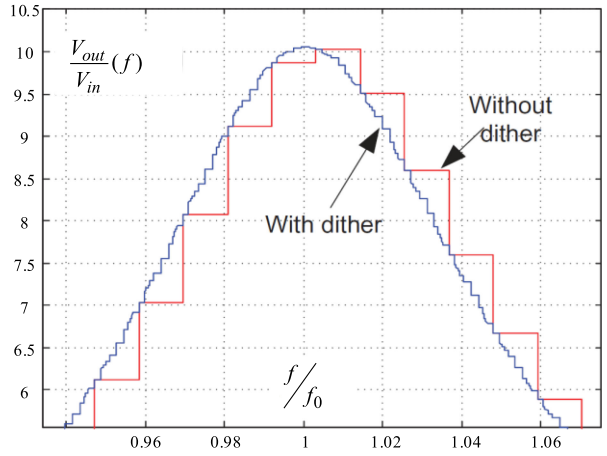

Fig. 13. Simulated frequency response (sweep) of L-type resonant network; comparison between typical DCO frequency steps and 3-bit resolution dithered-based DCO.

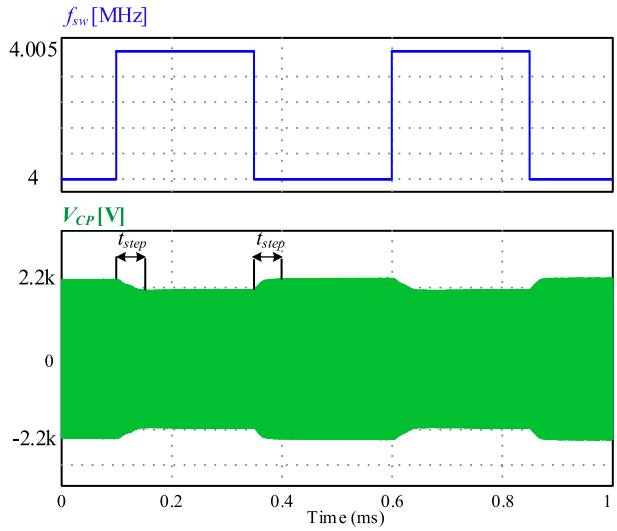

Fig. 14. Simulation results showing the convergence of the resonator's sinusoidal voltage, V_{CP}, to frequency steps of ± 5 kHz.

B. Phase Detection Signal Averaging

In addition to stability issues due to frequency resolution and LCO, noises due to the phase detection process might also result in unstable operation. Noise sources such as quantization of the time-to-digital unit and sensing or thermal noises may also affect the accuracy of the phase detection, which is then translated to inaccurate frequency compensation. To remedy this, synchronous averaging of samples has been employed to average out the phase error signal. This has been carried out by eight-word-long auto-regressive moving average (ARMA) filter [75], [76]. Although this averaging process might extend the duration of the self-tuning routine, it enables to smoothen the phase error, which results in better frequency compensation. It should be noted that the averaging window can be programmed to lower lengths in case faster responses are desired.

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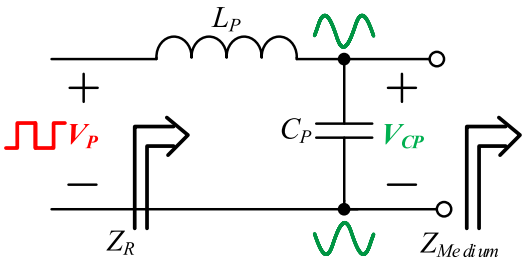

Fig. 15. Simplified equivalent circuit for the transmitting side.

C. System Bandwidth Selection

To assure reasonable dynamics of the feedback loops, and to assure sufficient decoupling of the feedback loops as well as steady-state convergence per medium settings, the system's bandwidths are assigned with respect to the transmitter's quality factor, Q, and the target operating frequency, f_{sw}, of the system. As discussed in Section IV-A, the response rate to changes in the control (drive frequency) signal might be rather slow because of the somewhat open-circuit parallel loading of L-type resonator (Fig. 15). The quality factor of the transmitter is a factor of the operating frequency as well as the resonant components and can be estimated as

$$Q = Z_{\text{medium}}(f_{sw}) \Big/ Z_R(f_{sw}), \tag{11}$$

where Z_{medium} represents the reflected equivalent impedance to the transmitting side, which is primarily determined by the coupler, and Z_R is the impedance of the resonator. The natural slow response of the resonator should be taken into consideration in the selection of the system bandwidth and overall response rate. Fortunately, the objective of the control is to track the resonant frequency of the system and to maintain a regulated current/power in the transmitter under variations of the wireless medium or other components drifts, which are the result of either mechanical movements or changes in environmental conditions that typically vary slowly.

The selection reasoning is as follows. The loop of the fastest bandwidth of the control loops is the DCO, denoted by BW_1. Therefore, for a given quality factor Q of the resonant networks, and assuming that f_{sw} is locked on f_0. Then, $BW_1$is determined as follows:

$$BW_1 = f_{sw} \Big/ 2Q. \tag{12}$$

This is set such that the loop has relatively wide bandwidth, but is with the capability of the resonant network response rate. The current control loop is set to be with slower response, typically one-ninth (1/5) to one-fiftieth (1/20) of the system's switching frequency

$$BW_2 = BW_1/10. \tag{13}$$

By doing so, the control loops are virtually decoupled and the tuning process does not depend on preceding information or data of the system to facilitate closed-loop operation.

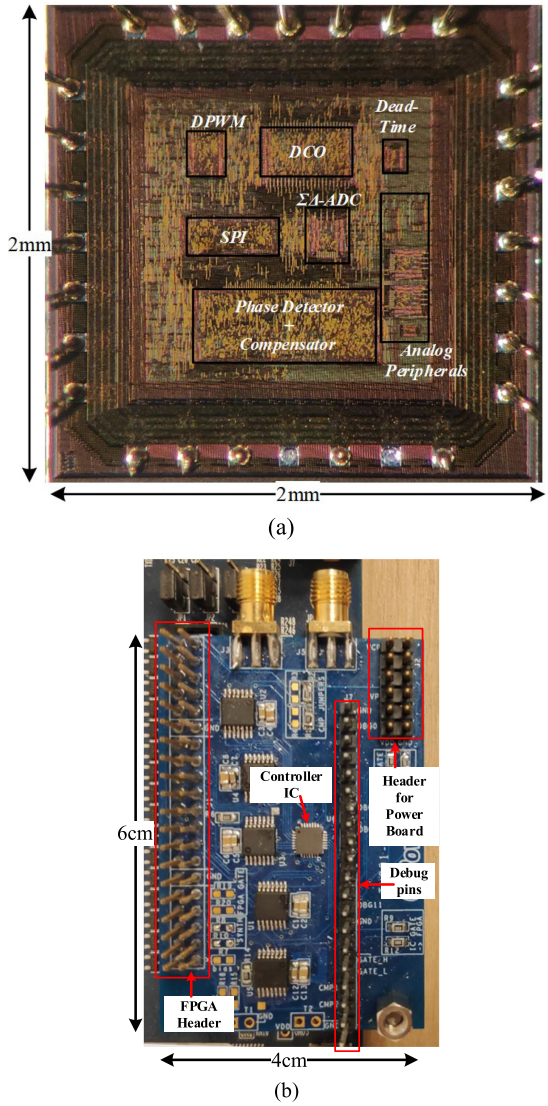

Fig. 16. (a) Micrograph of the fabricated RWPT controller IC. (b) Evaluation board of the IC.

V. Experimental Verification

An RWPT mixed-signal controller IC has been designed and fabricated in 0.18-μm 5-V CMOS process; the IC micrograph is depicted in Fig. 16(a), and the fabricated IC on an evaluation board is shown in Fig. 16(b). The overall chip area is 4 mm^2, while the effective silicon used is 0.6 mm^2. The delay of the buffer-based delay element used for the asynchronous architecture of the controller is ~200 ps, which is translated to operating frequencies range of 1.25–10 MHz. The main characteristics of the controller IC are summarized in Table I. It should be emphasized that the controller's design scales with the technology, such that its overall area and performance can be further improved by implementing it to more advanced process without significant penalty on the power consumption.

The operation of the controller IC has been verified prior to fabrication with post-layout analysis using Cadence Virtuoso, where the IC drives a full-bridge inverter at the front-end, with

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TABLE I
MIXED-SIGNAL CONTROLLER IC MAIN CHARACTERISTICS

IC Block / Parameter	*0.18-μm CMOS*
Package	28 pins 5x5 QFN
Supply voltage	5-V
Single cell delay t_{DE}	200 ps
Phase detector resolution	11-bits
Phase detector+Compensator Si area	0.225 mm^2
DCO resolution	12-bits
DCO frequency range f_{SW}	1.25-to-10 MHz
DCO Si area	0.097 mm^2
DPWM resolution	13-bits
DPWM nominal frequency	625 kHz
DPWM Si area	0.03 mm^2
ADC resolution	10-bits
ADC Si area	0.025 mm^2
Dead-time range	6.5-51 ns
Dead-time Si area	0.01 mm^2
Effective Si area *including analog peripherals and SPI	0.6 mm^2
Total chip Si area (pad limited)	4 mm^2

an external L-type resonator [see Fig. 17(a)]; $L_P = 11\ \mu$H, $C_P = 50$ pF for 6.78-MHz operation, and LP = 45 μH, CP = 35 pF for 4-MHz operation. Using high-impedance resistive divider, the voltages V_P and V_{CP} are scaled down to voltage levels suitable for the chip operation. Fig. 18(b) depicts the results for resonant operation at 6.78 MHz; as can be seen, the target phase reference (90°) is translated to decimal representation of "1864," phase difference is "1860," and thus, the error equals to 4 (with respect to 11-bit). The dead-time between the generated gate drive signals is 6.5 ns. Fig. 18(c) demonstrates resonant operation at 4 MHz; it can be noticed that although phase difference of 90° is obtained, the values are translated to different decimal representations, since the values are normalized with respect to the switching period, as discussed in Section III-A. In addition, Fig. 18 shows frequency resolution measurements at 6.78 and 4 MHz, respectively. As can be seen, the effective frequency resolution at 4 MHz is ±1.25 kHz, whereas for 6.78 MHz, the effective resolution is approximately ±4 kHz, which satisfies the allocated frequency bandwidth according to air–fuel alliance [76].

To validate the new adaptive RWPT controller IC and demonstrate operation for complete resonant-based WPT system, a resonant capacitively coupled experimental setup has been constructed as shown in Fig. 19(a) (detailed description and discussion on the system is provided in Appendix A). The capacitive coupler has been designed to be symmetrical, where each coupling plate is made of copper with overall dimensions of 30 x 250 mm. In addition, the capacitive coupler has been constructed to be dynamic, such that the wireless medium can be simply varied to different misalignments. Zoom-in views on the capacitive coupler for aligned and fully misaligned coupler are shown in Fig. 19(b) and (c), respectively. Detailed discussion on the capacitive coupler followed by Maxwell analysis is provided in Appendix B. Both the transmitter and receiver consist of an L-type network, resonating at the vicinity of 4 MHz. The variable inductor has been designed to vary between 1 and 4 μH, which is translated to frequency variation of 4–4.2 MHz. For biasing, the variable inductor TI's buck current regulator has been used

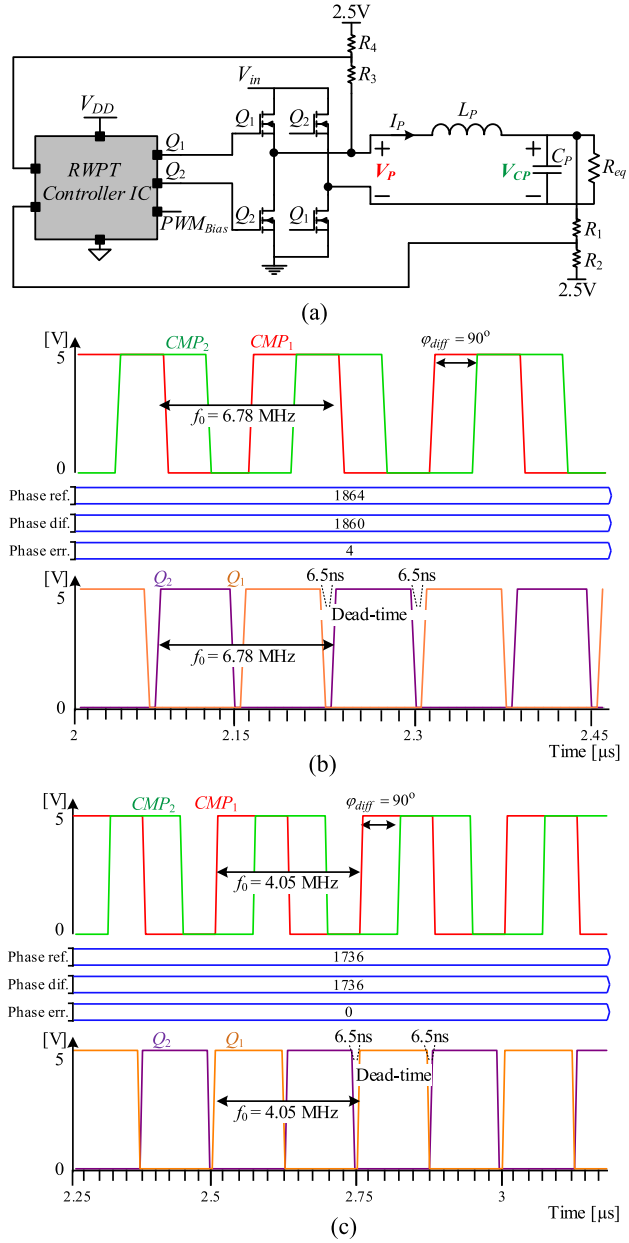

Fig. 17. Post-layout results of the controller IC. (a) Simulations test-bench. (b) Tuned operation at 6.78 MHz. (c) Tuned operation at 4 MHz.

[77]. Fig. 20(a) shows the custom-designed variable inductor which comprises an E-type EFD20-PC200 magnetic element. Fig. 20(b) shows the measured inductance as a function of the bias current up to 0.35 A, which is translated to 8× variation of inductance. The full-bridge inverter has been realized with GaN power modules suitable for multi-MHz operation [78]. The overall nominal operating conditions and parameters of the experimental prototype are summarized in Table II.

Fig. 21 shows closed-loop steady-state measurements of the system, where the receiver and the transmitter are fully aligned. As can be seen, the input voltage fed to the transmitter's resonator toggles between 35 and −35 V, and the resonant current peaks at 1 A. To obtain soft-switching throughout the entire

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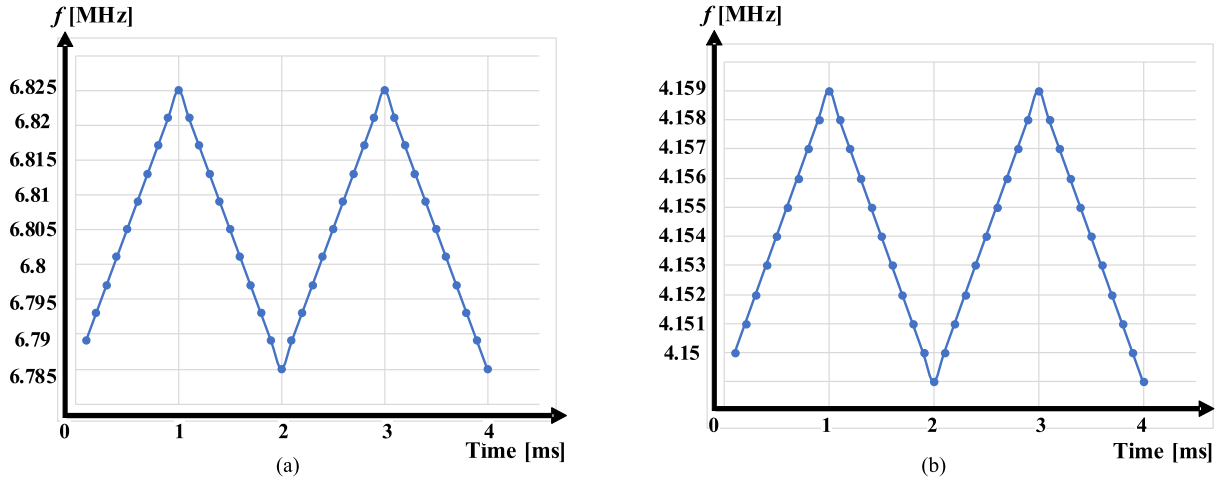

Fig. 18. Frequency resolution at the vicinity of resonant operation at (a) 6.78 MHz and (b) 4 MHz.

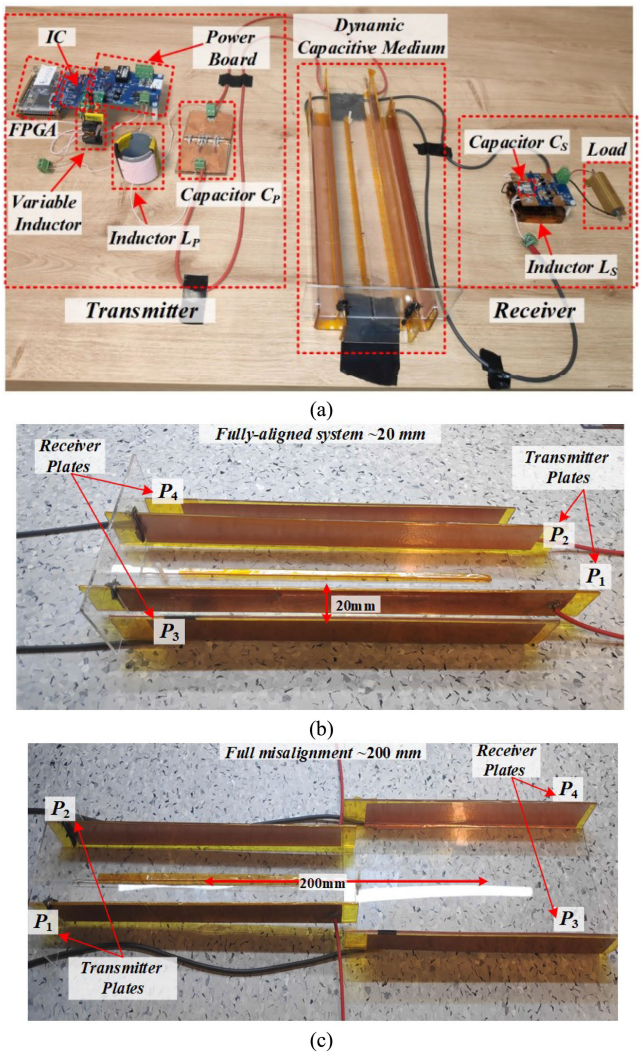

Fig. 19. (a) Resonant capacitively coupled WPT experimental system integrated with the controller IC board. (b) Zoom-in view on the capacitive-coupler for nominal orientation ~20 mm misalignment. (c) Zoom-in view on the capacitive-coupler for ~200 mm misalignment.

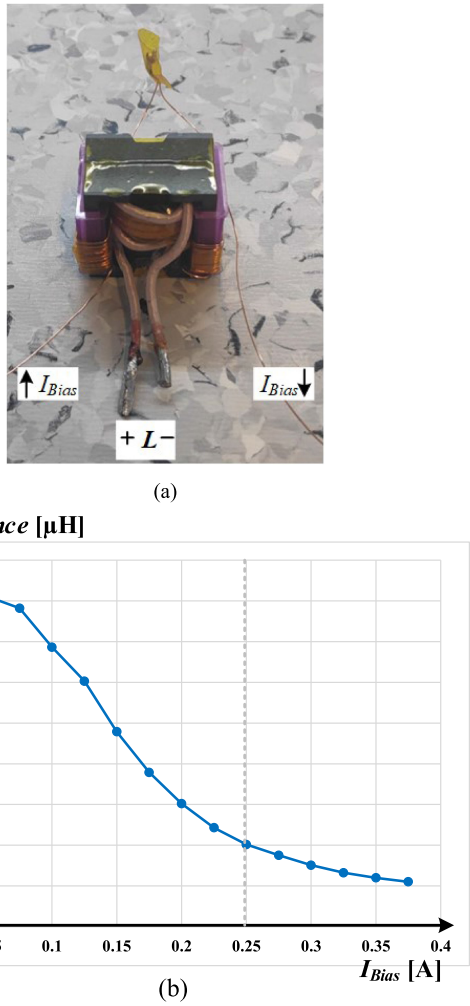

Fig. 20. (a) Variable inductor. (b) Measured variable inductance as a function of the bias current.

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TABLE II
EXPERIMENTAL PROTOTYPE VALUES AND PARAMETERS AT NOMINAL OPERATION

Parameter	*Value/Type*
Input voltage V_{in}	35-V
Transmitter's current	2-A
Load resistance	100 Ω
Nominal output power	20 W
Nominal efficiency	83%
Coupling plates	30x250 mm, copper stripes
Medium variation	20-200 mm
Full-bridge inverter	TI-LMG5200
Rectifier diodes	Vishay-VSSC520S-M3
Bias driver	TI-TPS92512DGQR
Inductors L_P and L_S	~45 µH
Variable inductor	1-4 µH
Capacitors C_P and C_S	35 pF
Operating frequency f_0	4-4.2 MHz

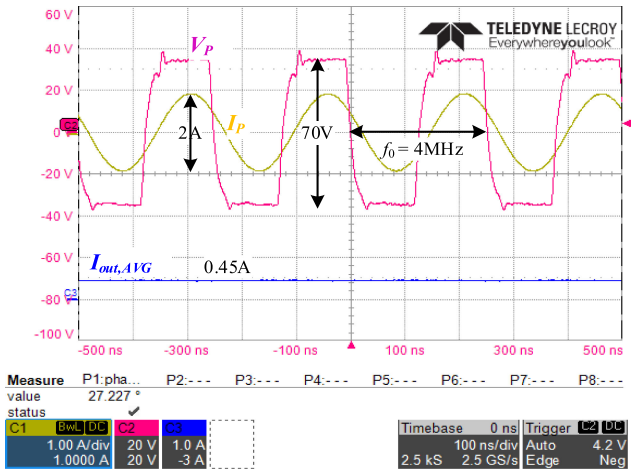

Fig. 21. Closed-loop operation waveforms at nominal conditions: $V_{\rm in} = 35$ V, $f_0 = 4$ MHz, $R_{\rm Load} = 100\ \Omega$, $I_{\rm out,AVG} = 0.45$ A. Voltage scale 20 V/div, current scale 1 A/div; time scale 100 ns/div.

operating range and to compensate for phase offsets due to the voltage sensors, the phase reference for the phase detection has been programmed to 115° (translated to 25° phase difference between V_P and I_P), which results in operation slightly above the resonance. The average output current, $I_{\rm out,AVG}$, at the receiver side is 0.45 A, which corresponds to an output power of 20 W with a peak efficiency of 83%. It should be emphasized that detailed analysis of ZVS operation is not a key objective in this study, and comprehensive soft-switching analysis for high-frequency amplifiers is previously covered in the literature [49], [72], [73].

To further validate and demonstrate the effectiveness of the controller IC, the wireless system has been tested for different medium variations as depicted in Fig. 22. It can be noticed that the measured phase difference between the signals CMP_1 and CMP_2 over the entire medium range is 115°, as predefined for the phase detector. In addition, it can be observed that at full misalignment, the receiver's resonant current, I_S, decreases due to low coupling between the transmitter and receiver. On the other hand, the transmitter is kept at resonance over the entire variation range, where its resonant current, I_P, remains virtually at 1-A peak as targeted. The latter is accomplished by the adaptive tuning of the resonator inductance and self-frequency tracking mechanism, in which for the given set of measurements, it can be seen that the frequency increases as the misalignment increases. Main parameters and values for the various misalignment experiments are summarized in Table III, including the coupling coefficient, k_C, and mutual coupling capacitance, C_M, per operating point (according to the analysis in Appendix B).

Fig. 23 shows dynamic responses of the WPT system to load changes. It can be seen that for 100 to 50 Ω step, the transmitter current, I_P, drops from 1-A peak and settles back to steady-state condition after 2 ms, whereas the load current increases from 0.45 to 0.6 A [Fig. 23(a)]. On the other hand, for 50 to 100 Ω load change (Fig. 23b), the transmitter returns to steady-state operation with target peak current of 1 A within ~4 ms, and the load current drops to 0.45 A. To further examine the dynamics of the controller, more extreme load steps have been performed. Fig. 23(c) shows the measurements for 100 to 25 Ω load change, where the average output current increased from 0.45 to 0.85 A, almost twice the nominal current. The transmitter current returns to 1 A within ~2.6 ms, whereas for the inverse load step, i.e., 25–100 Ω [Fig. 23(d)], the transition lasts 3 ms. Fig. 24 depicts transmitter's steady-state waveforms for 0.85 A output current. To achieve better ZVS operation for the higher load steps, the phase reference for the phase detection has been programmed to 125° (translated to 35° phase difference between V_P and I_P). As can be observed, for various load steps, well-regulated responses are obtained with reasonable dynamics. It should be emphasized that by employing the controller IC concept to the receiver side also will enable more degrees of freedom on the power regulation and spatial freedom, and can significantly improve the overall end-to-end performance.

VI. CONCLUSION

An adaptive self-tuned high-performance controller IC for resonant-based WPT transmitters has been detailed, analyzed, and experimentally validated. The IC comprises two main independent control loops, which effectively disengage the power transfer capabilities of RWPT from medium variations and other potential drifts, and further enables spatial freedom. The control algorithm, signal flow, and the mixed-signal controller IC architecture have been addressed. The controller has been designed and fabricated in 0.18-μm 5-V CMOS process with effective silicon area of 0.6 mm^2. The digital core of the mixed-signal controller IC has been developed on the basis of all-digital standard-cell approach and can therefore be designed using a generic digital flow procedure. In the IC design, several main enabling key building blocks have been developed: DL-based phase detector, high-resolution DCO, and high-resolution DPWM. Postlayout analysis of the controller IC demonstrates high-performance self-tuned system. To further validate the controller, an experiential resonant capacitively coupled WPT system in the MHz range has been designed and evaluated with the controller IC over various operating conditions. The resultant dynamic performance of the closed-loop system is well validated

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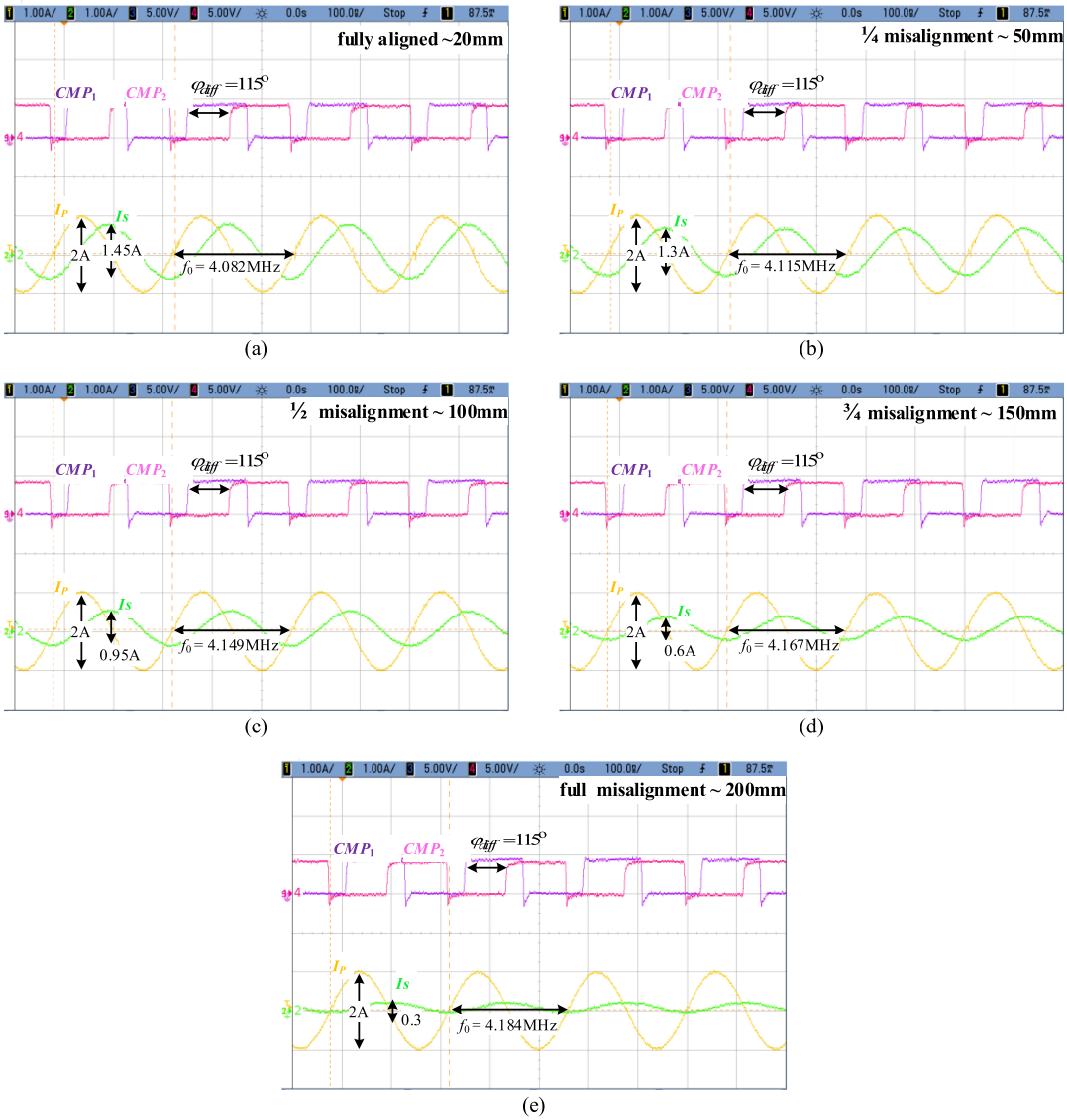

Fig. 22. Experimental measurements at closed-loop operation for different medium misalignments. Voltage scale 5 V/div; current scale 1 A/div; time scale 100 ns/div.

TABLE III
SUMMARIZED PARAMETERS AND VALUES FOR MISALIGNMENT EXPERIMENTS

Misalignment [mm]	*Kc*	*Cm* [pF]	I_P [A]	L_P [μH]	f_0 [MHz]	I_{out} [A]
20	0.92	2.2	1	45	4	0.45
50	0.69	1.8	1	44.1	4.04	0.4
100	0.50	1.4	1	43.3	4.12	0.3
150	0.33	1	1	42.4	4.16	0.19
200	0.06	0.2	1	41.6	4.24	0.08

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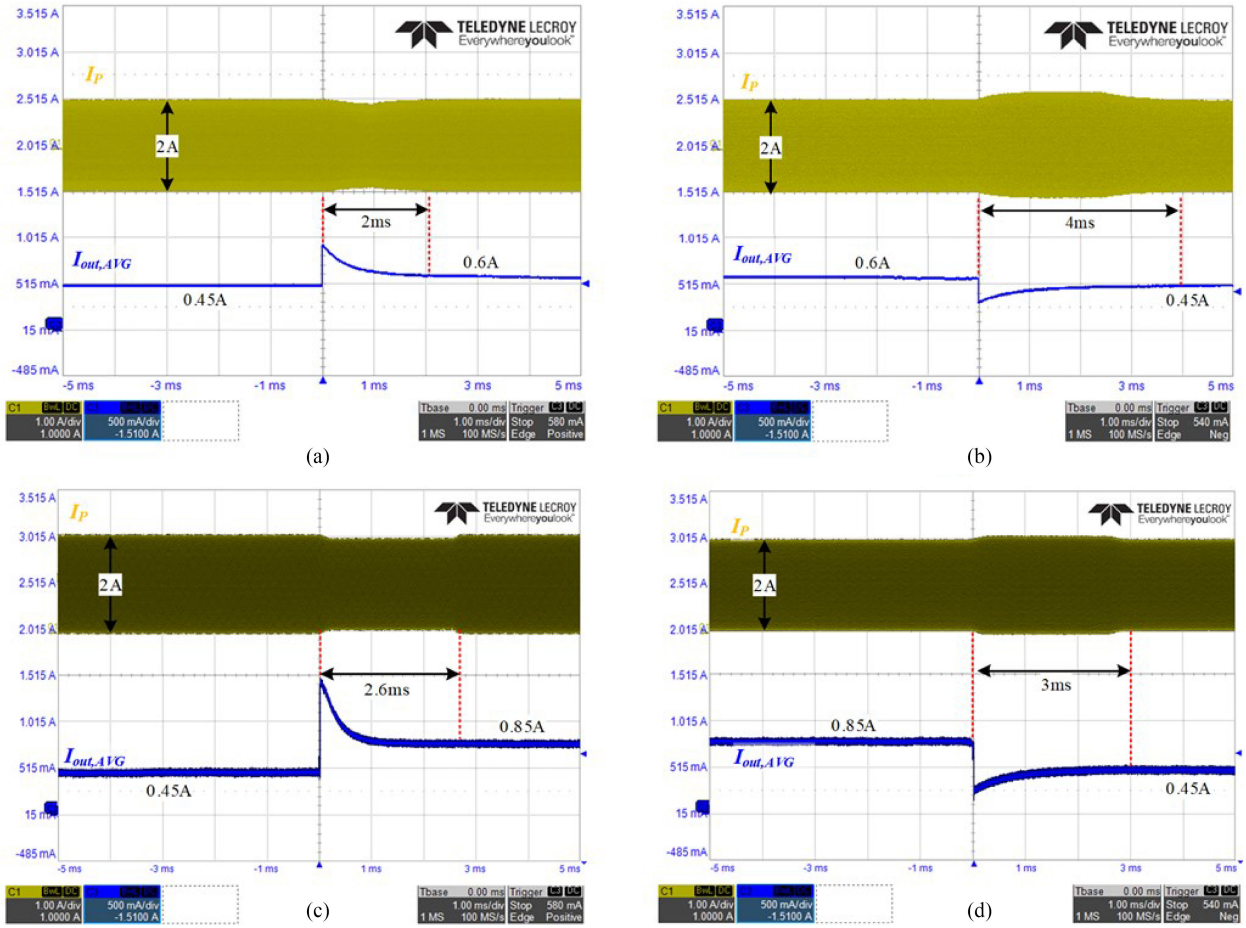

Fig. 23. Experimental waveforms for load changes. (a) Changing R_{Load} from 100 to 50 Ω. (b) Changing R_{Load} from 50 to 100 Ω. (c) Changing R_{Load} from 100 to 25 Ω. (d) Changing R_{Load} from 25 to 100 Ω. I_P (yellow trace) 1 A/div, $I_{\mathrm{out,AVG}}$ (blue trace) 0.5A/div; time scale 1 ms/div.

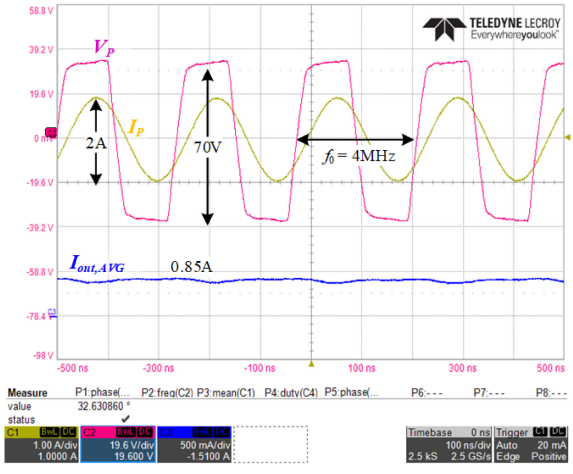

Fig. 24. Transmitter's steady-state waveforms for 0.85-A average output current. V_P (pink trace) 20 V/div, I_P (yellow trace) 1 A/div, $I_{\mathrm{out,AVG}}$ (blue trace) 0.5A/div; time scale 100 ns/div.

through experiments up to 200 mm misalignment. The new mixed-signal controller IC concept may be found very beneficial in many resonant-based wireless technologies, particularly in terms scalability and technology advancements.

APPENDIX A

This Appendix briefly describes and reviews a capacitively coupled RWPT system with L-type resonators in both the transmitter and receiver sides, as shown in Fig. 25. It should be noted that a detailed derivation of the end-to-end relationships of the system is thoroughly described and can be found in [15], [17], [79]. Therefore, only the essential in-context details have been brought up here in order to establish the foundations for power regulation control. The capacitive WPT system is driven by a full-bridge inverter in the transmitter side, and the load is fed via a diode rectifier that is connected to the receiver's resonator. Typically, the mutual coupling capacitance between the electrodes, C_M, is lower than the resonators' matching capacitances C_P and C_S [14]–[17]; given that the drive frequency, f_{sw}, is near the resonators' natural frequency (i.e., $f_{sw} \approx f_0 = 1/(2\pi\sqrt{L_P C_P}), = 1/(2\pi\sqrt{L_S C_S})$, then the currents as well as voltages of the reactive elements are virtually sinusoidal [54]. This is since high-Q operation is naturally facilitated as the output impedances of the transmitter and receiver resonant networks are relatively high. In

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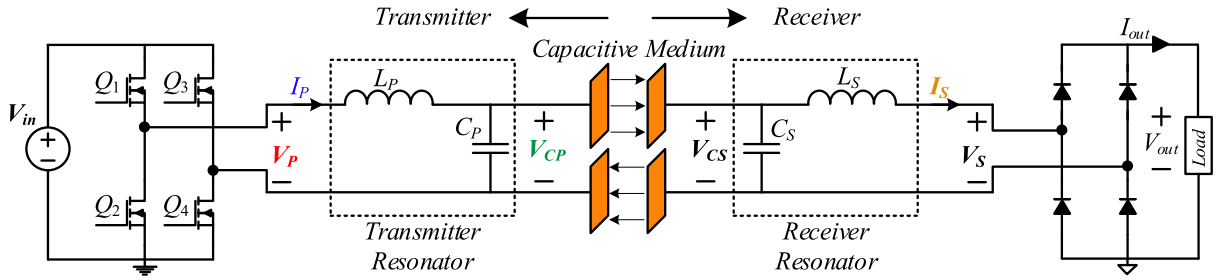

Fig. 25. Schematic diagram of a capacitive-based RWPT system with L-type resonators for both transmitter and receiver.

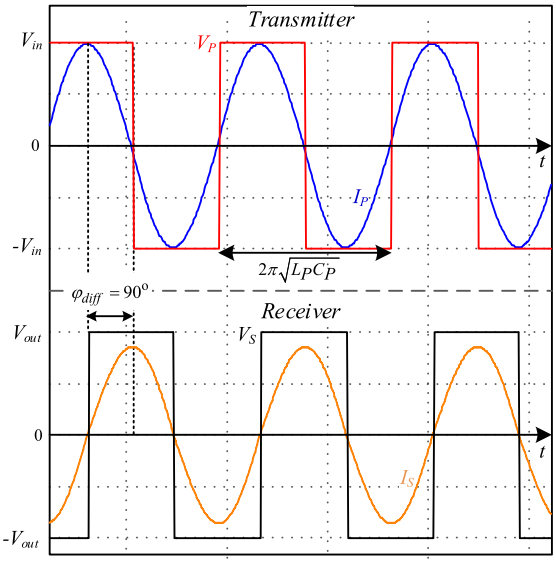

Fig. 26. Typical currents and voltages waveforms of the RWPT system: upper signals—transmitter; bottom signals—receiver.

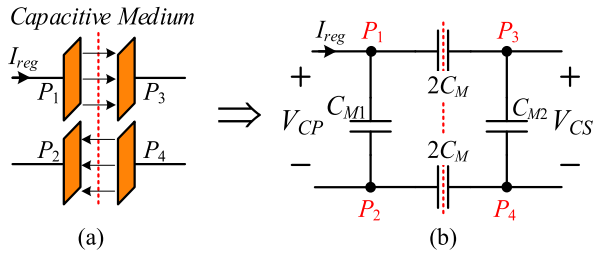

Fig. 27. Capacitive medium. (a) Simplified mechanical illustration. (b) Equivalent capacitances model.

[17], [79], it has been established that when resonant operation is satisfied, the transmitter's current, I_P, depends on the output voltage, while the receiver's current, I_S, depends on the input voltage, and thus with the aid of system parameters, the currents can be expressed as

$$I_P = \frac{2\pi f_0 C_P C_S}{C_M} V_S; \quad I_S = \frac{2\pi f_0 C_P C_S}{C_M} V_P \tag{14}$$

where C_M is the equivalent mutual coupling capacitance, and V_P and V_S are the voltages of the transmitter and receiver, respectively.

Typical waveforms of the CPT system are shown in Fig. 26. As can be seen, while the transmitter and receiver voltages V_P and V_S are square waves, the currents are sinusoidal due to high-Q operation of the circuit. Since a full-bridge inverter is used at the front-end, the transmitter voltage V_P toggles between $V_{\rm in}$ to $-V_{\rm in}$ while the receiver voltage, V_S, toggles between $V_{\rm out}$ to $-V_{\rm out}$. It can be also seen that for both the transmitter and receiver sides, the current is in phase with the voltage, whereas the receiver current I_S lags the transmitter current I_P by 90° (the same applies for the voltages V_S and V_P).

APPENDIX B

This Appendix describes the capacitive-based wireless medium that has been constructed for the experimental capacitive RWPT setup. The equivalent electrical representation of the capacitive medium is shown in Fig. 27. Here, C_M is the equivalent mutual coupling capacitance, C_{M1} and C_{M2} are the self-capacitances of the coupling plates [14]–[17]. Typically, in capacitive RWPT, the mutual and self-capacitances are lower than the resonators' matching capacitance.

To facilitate reliable estimation of the capacitive coupler for the experimental measurements, estimation of the plates capacitances has been carried out by Maxwell (Ansys) finite element analysis (FEA) tool (Fig. 28). Typically, FEA is generated by defining the geometry of the element and by setting the boundary conditions. In the context of the capacitive medium in this study, these are four symmetrical copper stripes followed by voltage excitations to the stripes. Rigorous simulation procedures over various misalignments have been carried out to determine the coupling capacitances for the constructed capacitive coupler, whereas each stripe is 30 × 250 mm. Fig. 28(a) depicts the fully aligned system which translates to 20 mm misalignment, whereas Fig. 28(b) depicts the wireless medium for 200-mm misalignment. It should be noted that for the given coupler design, the misalignment is defined as the gap between the transmitter and receiver centers, as illustrated in Fig. 28(a) and (b). The coupling capacitances of the stripes, C_M, C_{M1}, and C_{M2} have been calculated based on the equations in [14], [15] and the coupling coefficient, k_C, has been calculated by $C_M/(\sqrt{(\rm C_{M1}}$ $\rm C_{M2})$. The results for the equivalent mutual coupling capacitance, C_M, and for the coupling coefficient, k_C, as a function of the misalignment are shown in Fig. 28(c) and (d), respectively. It

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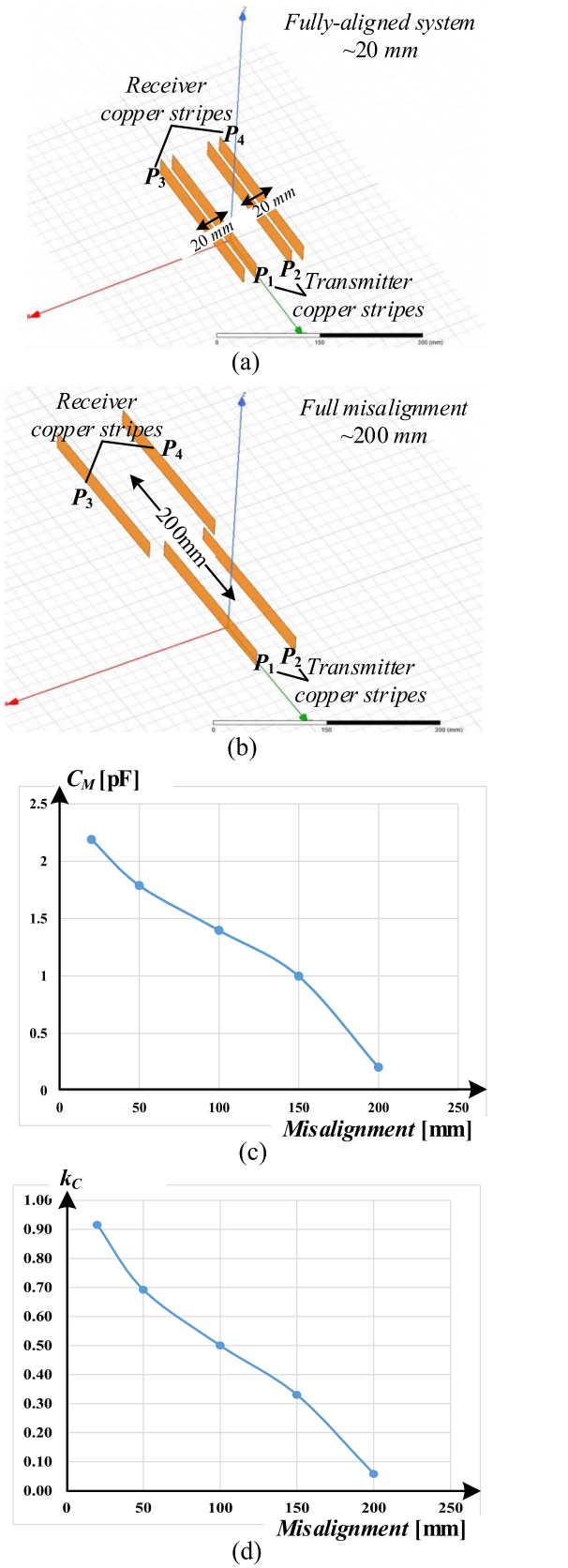

Fig. 28. Finite element analysis test-bench for the capacitive medium design. (a) Aligned coupler. (b) Fully misaligned coupler. (c) Equivalent mutual coupling capacitance, C_M, as a function of the misalignment. (d) Coupling coefficient, k_C, as a function of the misalignment.

can be observed that C_M decreases by approximately ten times for 200-mm misalignment, while the coupling coefficient drops to 0.06, i.e., deep loosely coupled region.

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