Digital Multiphase PWM Integrated Module Generated From a Single Synchronization Source

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***Abstract*—This article introduces a new architecture for a high-resolution digital pulsewidth modulator (HR-DPWM), which generates multiple output phases, all synchronized and derived out of a single reference source. Constructed through digital standard-cell delay chain and simple combinatorial logic, the module produces PWM signals with configurable on-time, period and time-delay (between phases) with resolution of a single delay element. To minimize the statistical error spread (e.g., jitter error) between phases, a single delay-line is utilized to generate a master time-base while combinatorial logic assigns per-phase independent duty-ratio settings. The resultant module minimizes the time-diversity error between phases, as any uncertainty in the on-time generation is identical between phases. The solution is compact, flexible and scales with the number of phases. Since the entire architecture is realized through standard cells, the solution also scales with fabrication technology and is described by HDL, which translates onto hardware using automated process. The HR-DPWM module has been designed and fabricated on a 0.18 μm 5 V CMOS process, totaling 0.08 mm^2 of effective silicon area. Experimental results of a four phase 13-bit HR-DPWM are provided, demonstrating high accuracy and linearity characteristics with time resolution of 200 ps and excellent matching and tracking between all phases.**

***Index Terms*—Delay-line, digital control, digital pulsewidth modulator, multiphase converter.**

I. Introduction

THE DESIGN of optimized digital controllers for switch-mode power supplies (SMPS) has been in pursuit by both academia and industry for many years [1]–[6]. A key reason is that digital hardware realization has several advantages such as flexibility, scalability, noise immunity, easier to configure, update or upgrade, and higher accuracy in facilitating the performance goals through systematic design procedures [4]–[10]. Controllers comprise of a compensation module, which executes the control law as well as high-performance peripheral units such as digital pulsewidth modulators (DPWM), drive circuitry and analog-to-digital converters (ADC), which are considered primary enablers of the controllers. Following the global trend of miniaturization and integration, efforts are heavily invested in the design of these peripheral units in a hardware-efficient manner so that all modules can be realized on the same die without the penalty of increased silicon area [3], [10]–[14].

In the context of digitally controlled SMPS, a high-resolution DPWM (HR-DPWM) is an essential building block to achieve the regulation accuracy, and as a result the system performance [15], [16], [19]. The conventional approach to implement HR-DPWM is by a fast-clocked counter-comparator scheme [20], [21]. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n \cdot f_s$. This translates to increased power consumption and more complex design to realize high-speed circuitry. Another approach is to realize a HR-DPWM based on a tapped delay-line (DL) scheme [13]. There, the power consumption is reduced but the required silicon area of the design grows exponentially with the number of resolution bits. A combination of both methods results in an area- and power-efficient HR-DPWM, as demonstrated for example in [22].

Realization of VRMs, or SMPS for high-performance loads often employ paralleling or interleaving multiple converters (illustratively shown in Fig. 1) to support the increased load current requirements and in particular rapid loading transitions. Power density is also improved since smaller magnetics are used per phase [5], [23], [24]. To ensure tight voltage regulation and accurate current-sharing, multiphase operation dictates synchronized operation of phases, with identical period and specified time delay between each phase, but at the same time, independent on-time settings per phase. The latter is required for specific compensation for variations or mismatches between the power-stages' switches and passive components.

Several approaches in the literature address the architectural complexity of high-resolution dedicated multiphase modulators (MPM) to derive independent, yet synchronized signals. Replication of several single-phase modulators or time-sharing of key architecture units has been covered [25]–[32]. In [26]–[28], an MPM is introduced with DL-based fine-resolution block that is time-shared between all phases operating with the same duty cycle. A primary challenge in the generation of the MPM is to minimize the error between phases, and if possible to assure consistent statistical drift of all generated signals per cycle. This can be accomplished if all generated signals are derived out of

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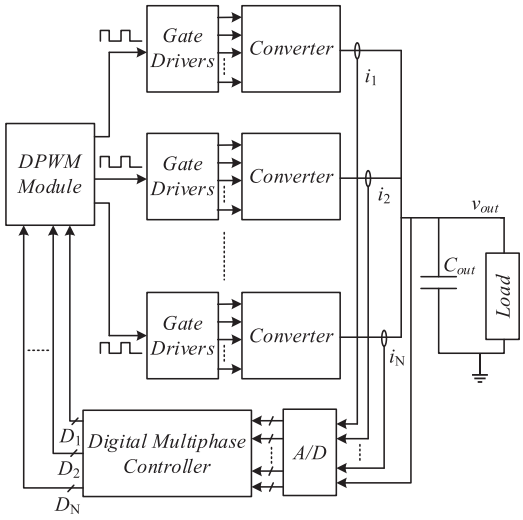


Fig. 1. Simplified block diagram of a current-mode controlled multiphase converter.

a single synchronization source—this has been pursued in this study.

To maximize the efficiency of multiphase converters, modern controllers are required to determine the number of active phases as a function of the instantaneous load current [34]–[38]. At light loads, the number of active phases is decreased to minimize the switching losses in the system, whereas for higher load currents more phases are activated to lower overall conduction losses and balance and share the loading task over several converters. Several approaches, such as in [26] and [27], determine the number of active phases as a function of the duty-cycle command, which may affect the converter's efficiency at light-loads. Therefore, to fully exploit the benefits of multiphase converters, modern state-of-the-art digital MPM include phase shedding and adding capabilities [5], [35]–[38].

The objective of this article is to introduce a new digital architecture for MPM that produces independent high-resolution drive signals derived from a single time-base source, minimizing the per-cycle systematic, or statistical error between phases, as shown in Fig. 2. The new MPM is entirely realized through hardware description langue (HDL), i.e., by pure digital means without additional custom design, and therefore is compact and efficiently scales with technology. The high-resolution drive signals are produced by simple combinatorial logic and a single DL that is time-shared between all phases while ensuring independent duty-cycle commands for each phase. The number of active phases N_{ph}, the switching frequency $f_{\rm sw}$, and the phase-shift can be set on-the-fly without any hardware modifications or performance penalties. It is a further aim of this article to detail the physical design considerations for the realization of DL-based DPWM on IC.

The rest of this article is organized as follows. Section II details the architecture of the new multiphase HR-DPWM and covers its principle of operation. Section III covers issues of practical implementation, including design flow, IC layout, and silicon size estimation. Section IV details a case study of the new HR-DPWM driving a multiphase buck converter. Experimental verification of the fabricated IC is provided in Section V. Section VI concludes this article.

II. Principle of Operation and System Description

The operation of the HR-DPWM unit (see functionality block depicted in Fig. 2) is described through the details of its configuration, its main building blocks and with a representative example of PWM signal generation. It comprises the following submodules: a) a *Governing Block* to manage, synchronize, and assign the number of active phases and duty ratio of each phase; b) *Comparison Logic* blocks to generate coarse clock signals as the base of the PWM product; and c) *Multiplexer Array* and *Output Logic* blocks, which generate the fine-tuned PWM signals.

To support interleaved operation of the HR-DPWM with individual pulse-width characteristics, the duty-cycle command for each phase is individually assigned every switching cycle and stored in a dedicated register. This is a desired feature of MPM, which enhances the effective bandwidth of the control loop [23], [24]. The number of active phases, which determines the phase-shift between two consecutive PWM signals, can be modified with every duty-cycle command update, resulting in multiple update locations along a switching-cycle. Therefore, phase shedding and adding can be carried out on a cycle-by-cycle basis, as required in state-of-the-art multiphase platforms. The information of the duty-cycle commands is separated into coarse and fine segments, which are the inputs to the HR-DPWM submodules, as shown in Fig. 2, by the following process. The coarse segment of the duty-cycle command $D_{\rm MSB}$, is processed in a synchronous manner by the digital comparison logic block, generating the clock-based contribution to the PWM signal. This block compares the counters' results with the $D_{\rm MSB}$ value, thus creating a pulse that is a multiplication of the system's internal clock (see $clk_{\rm base}$ in Fig. 2). The fine segment of the duty command $D_{\rm LSB}$, is used to generate a time-delayed replica of the HR-DPWM's internal clock with time-resolution of a single delay-element. These internal signals are fed into the output logic blocks to produce the final high-resolution PWM product.

A master time-base that produces the system's reference clock (see $clk_{\rm base}$ in Fig. 2) is realized by a ring-oscillator with N_{DE} delay elements. The base frequency can be expressed as

$$f_b = \frac{1}{2N_{DE} \cdot t_{de}} \tag{1}$$

where t_{de} is the average time delay of each delay element. The duty command consists of N_d bits as follows:

$$D = [D_{\rm MSB}, \_, D_{\rm LSB}] \tag{2}$$

where the m MSBs assigns the coarse part of the PWM signal and the $l+1$ LSBs are used for its fine-tuning counterpart. The length of the $D_{\rm MSB}$ section sets the frequency range of the HR-DPWM module. The length of the $D_{\rm LSB}$ section is a function of the shared delay-line length and is chosen according to the desired frequency of the master time-base f_b.

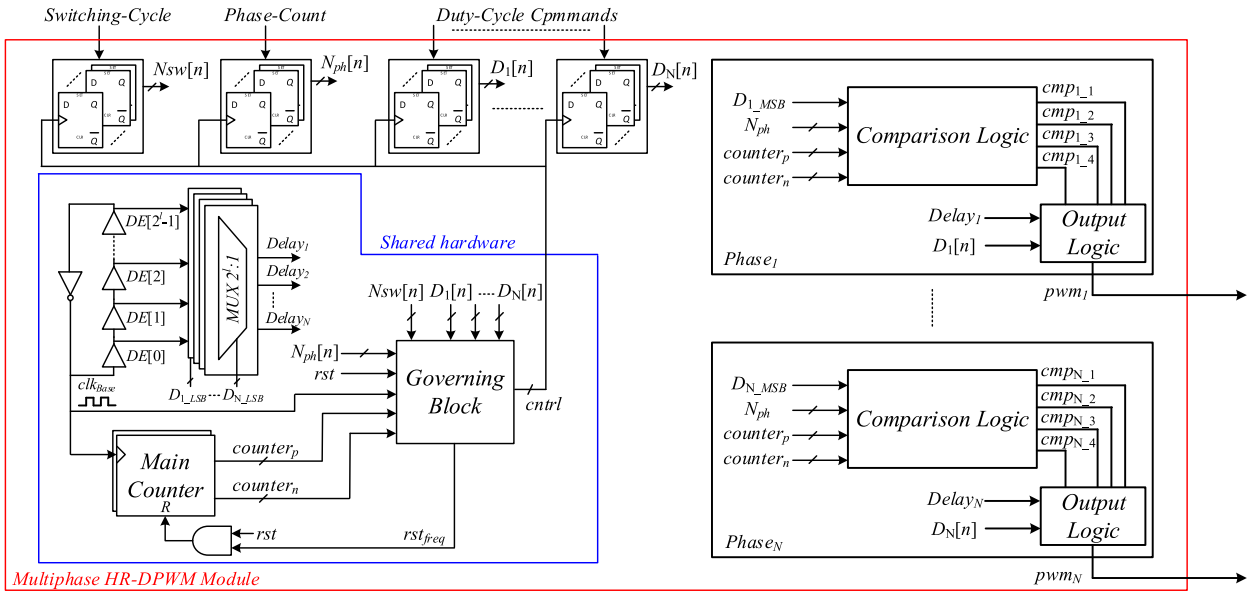


Fig. 2. Multiphase HR-DPWM architecture with single synchronization time-base.

A. Governing Block

To fully exploit the benefits of multiphase converters by utilizing a number of active phases and as a result accelerate the dynamic characteristics of the voltage regulator, the switching frequency and most importantly the duty-cycle commands can be updated with an expedited rate of

$$f_{\text{update}} = N_{ph} \cdot f_{\text{sw}} \tag{3}$$

where N_{ph} is the number of active phases and f_{sw} is the switching frequency. Should a case required to enhance the bandwidth of the controller's inner-loop (see Fig. 1) the duty-command of each phase may be sampled in multiple locations along a single switching-cycle, which leads to reduced digital control delays as detailed in [39]–[42].

The Governing Block updates the duty-cycle commands, switching frequency, and the number of active phases at predetermined locations along the switching-cycle, synchronized to the rising-edge of each phase's PWM signal, as shown in Fig. 2. This is carried out by internal signals generated in the Governing Block (*cntrl*) that divide the switching-cycle into N_{sw} sections and act as the triggers for the sampling registers (see Fig. 2).

Synchronization of all internal logic is carried out by the Governing Block, which oversees the interleaved operation of the HR-DPWM and dictates the timing locations for sampling duty-cycle commands, switching frequency, and number of active phases on-the-fly from the preceding compensation unit. The switching frequency is set according to an m-bit input signal (see N_{sw} in Fig. 2), which dictates the number of internal clock-cycles per converter switching cycle. Since multiple PWM signals are generated from the same module, the number of active phases is factored into the switching-frequency calculation, which results in a discrete set of possible frequencies.

$$f_{\text{sw}} \in \left\{ \frac{f_b}{N_{\text{sw}}} \,|N_{\text{sw}} = N_{ph}, 2N_{ph}, \ldots, 2^m \right\}. \tag{4}$$

The number of active phases also determines the phase-shift between the generated PWM signals according to the following relation:

$$\phi = \frac{180^o}{\log_2 N_{ph}} \tag{5}$$

where $\log_2(N_{ph})$ is an integer. Equations (4) and (5) indicate the phase-generation capabilities for binary-weighted multiphase converters, which are common practice in the target applications. It should be noted that the architecture presented in this article may be adjusted to produce any number of phase-shifted PWM-signals for which the phase-shift between consecutive signals will be equal to $360^o/N_{ph}$. This will require additional constraint on the switching frequency: $N_{\text{sw}} = KN_{ph}$, where K is an integer. This is to ensure the synchronization of the beginning of each phase's switching-cycle to the reference clock, clk_{base} in Fig. 2.

B. Comparison Logic

The comparison logic blocks comprise combinatorial logic to produce the coarse part of the PWM signals and to generate internal signals utilized by the fine-tuning logic of the HR-DPWM. The inputs of the comparison logic blocks are the number of active phases, the MSBs of the duty-cycle command and the outputs of an m-bit counter block (see *main counter* in Fig. 2). The phase-shift characteristics of each phase with respect to the leading one are expressed as a function of the blocks' inputs as follows:

$$d_{ph} = \frac{N_{\text{sw}}}{N_{ph}} \cdot c; \quad c \in \{1, 2, \ldots, N_{ph} - 1\}. \tag{6}$$

All Comparison Logic blocks process their inputs according to the internal logic summarized in Fig. 3 in a synchronous manner utilizing the same counter block to produce four output signals (see cmp_x in Fig. 3). The first signal cmp_{x_1} is the coarse part of the PWM signal while the remaining three are used by the

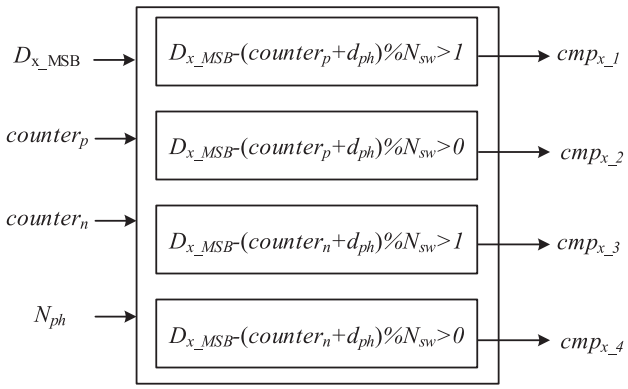


Fig. 3. Schematic representation of the comparison block's internal logic.

Output Logic blocks to construct the high-resolution fine part of the HR-DPWM outputs.

An exemplary case of a two-phase interleaved operation is illustrated in Fig. 4 with $N_{ph} = 2$ and $N_{\rm sw} = 8$. The internal clock signal $clk_{\rm base}$ along with the synchronous counters' values, $counter_n$ and $counter_p$ are illustrated at the top of the timing diagram of Fig. 4. Here, the decimal values of the duty-cycle MSB parts are 5 and 3 for the $\rm pwm_1$ and $\rm pwm_2$ signals, respectively. The outputs of the Comparison Blocks for each phase are included (cmp_{x_1}-cmp_{x_4}) according to the internal logic of Fig. 3. For example, cmp_{1_1} is high until $counter_p$ reaches the value of 5, according to the first condition of Fig. 3 and cmp_{1_2} remain high for an additional cycle according to the second condition of Fig. 3. cmp_{1_3} and cmp_{1_4} are generated in a similar manner with the only exception of the reference counter, now $counter_n$. As can be seen, these signals are shifted by $1/2T_{clk}$ with respect to cmp_{1_1} and cmp_{1_2}. As can be seen, the final high-resolution PWM signals comprise of a coarse part derived by the synchronous logic of the Comparison Blocks and a fine-tuning addition based on a time-delayed replica of the $clk_{\rm base}$ signal. Here, the value of d_{ph} is 4, according to (6), resulting in a 180° phase-shift between the two interleaved PWM signals.

It should be noted that similar architecture can be derived that would be based on triangular counters as discussed in [39] and [42] without compromising on resolution or increased hardware requirements. It involves an additional down-slope for the shared counters ($counter_p$ and $counter_n$) and minor adjustments to the Comparison Logic blocks to support the signal generation during the down-slope segment of the triangular counters cycle.

C. Multiplexer Array and Output Logic

The Output Logic block of each phase produces the high-resolution PWM signal as a function of the Comparison Logic blocks' outputs and two additional input signals: the duty-cycle command and the corresponding $Delay_x$ signal, as illustrated in Fig. 2. The $Delay_x$ signal is produced by the multiplexer array fed by the delay-elements of the ring-oscillator, as shown in Fig. 5(a). Therefore, the $Delay_x$ signal is a time-delayed replica of $clk_{\rm base}$ with time-resolution of t_{de}, which results in 2^l available time-delayed signals for the fine-tuning operation

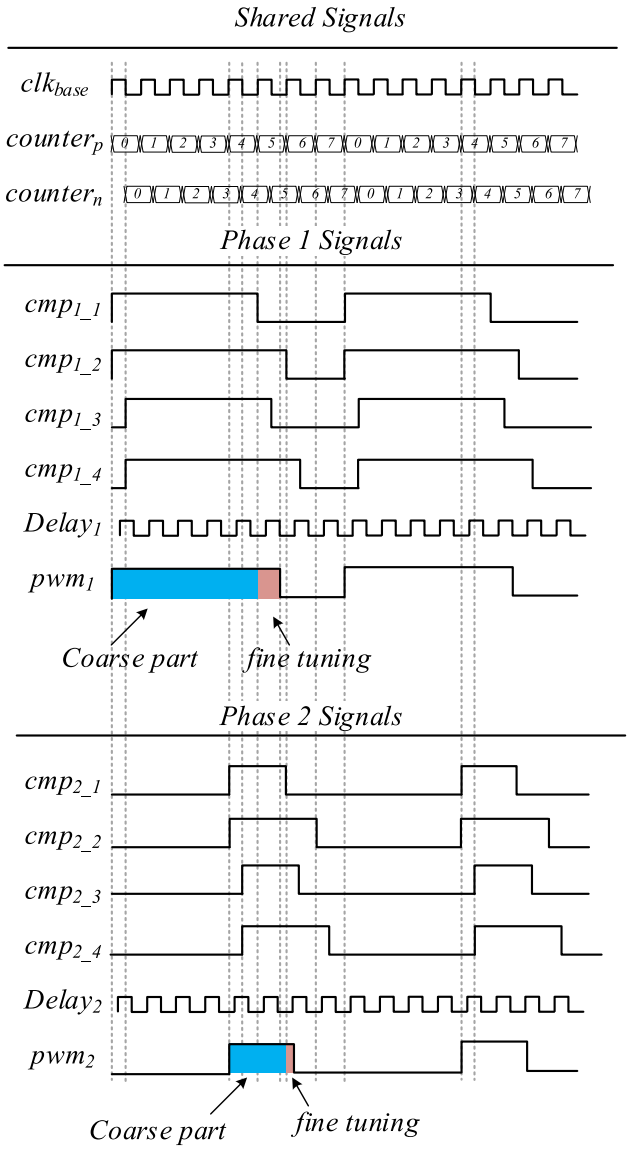


Fig. 4. Timing diagram of the internal signals and the produced PWM signals for a case of two-phase interleaved operation. Signals $cmp_{\rm x}$ are clock-based signals, while $Delay_{\rm x}$ are time-based replicas of $clk_{\rm base}$ with time-resolution of t_{de}.

of the HR-DPWM. Shown in Fig. 5(b) is the $clk_{\rm base}$ signal and two of its time-delayed replicas ($0<y<2^l$).

Therefore, a single delay-line that is also used for the generation of the master time-base is utilized by the multiplexer array to generate all delayed replicas of the $clk_{\rm base}$ signal. This minimizes time-diversity errors, since any uncertainty in the on-time generation is identical between all phases. Furthermore, utilization of a single delay-line by both synchronous modules such as the Comparison Logic blocks and the purely combinatorial modules such as the Output Logic blocks results in a compact design without the need to actively synchronize modules with multiple time domains.

Three simple combinatorial logic branches make up the Output Logic block. The first, as shown in Fig. 6, applies for the case where $0<D_{x\_\rm MSB}<2^m$-1. As can be seen, this branch is

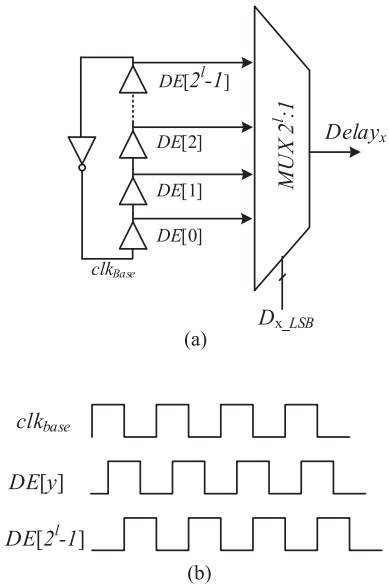


Fig. 5. (a) $Delay_{\rm x}$ generation circuit for an arbitrary phase x and 2^l delay-elements based ring-oscillator. (b) Timing diagrams of $clk_{\rm base}$ and two of its time-delayed replicas, $0<y<2^l$.

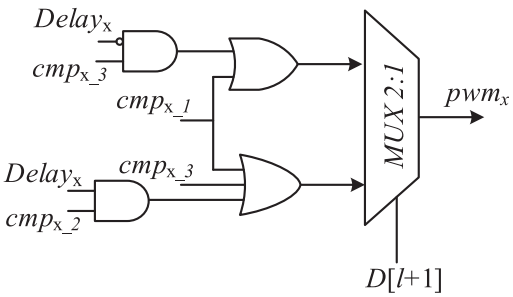


Fig. 6. Combinatorial logic of the output logic blocks.

also divided into two sub-branches as a function of the $D[l+1]$ bit, which determines if the required fine-tuning addition to the clock-based part is larger or smaller than $1/(2f_b)$. The exemplary PWM signals (PWM_1, PWM_2) shown in Fig. 4 are generated by the logic described in Fig. 6, where PWM_1 has a fine-tuning addition that is larger than $1/(2f_b)$ and the addition to the coarse part of PWM_2 is smaller than $1/(2f_b)$. For the cases where $D_{x\_\rm MSB} = 0$ or $D_{x\_\rm MSB} = 2^m$-1, the PWM signal is generated in a similar manner with minor modifications from the combinatorial logic illustrated in Fig. 6

III. IC Implementation

The realization of the HR-DPWM in this article primarily relies on an automated digital implementation flow, using vendor's standard cells. The IC implementation is described through three main steps. In the first step, each module is described in HDL (Verilog) as a standalone unit. This is done for the simplicity of the verification and functionality simulations. Then, each unit is translated into hardware using synthesis and timing verification tools into an optimized gate-level representation. In the third step, all units are integrated together onto the higher hierarchy of the HR-DPWM. Since automated place-and route tools may optimize the over-all die area at the expense of the module's linear characteristics or the matching between the different phases, the settings for area and timing constrains have been assigned to demonstrate compact fit in the silicon realization without sacrificing PWM resolution or matching attributes.

Monotonicity and linearity are important factors of DPWM generation. Modulators are often assumed as a constant gain in the compensation design and, therefore, it is essential to consider the linearity span of the DPWM generator. This issue is further elevated in the presence of asynchronous digital design such as delay-line. In this article, minimal distance as well as identical layout per-cell has been carried out throughout the delay chain in attempt to minimize the effects of variations. Furthermore, since a single delay line is used for timing generation of all phases, the tight placement of the chain reduces variations due to thermal drifts. Since the delay chain is programmable for selection of the time-base, this feature can be used for specific configuration of the running frequency. It should be noted that, in this particular study and IC implementation, no further calibration or active PVT compensation efforts have been carried out. The monotonicity linearity results of the fabricated modulator can be viewed later in Section V.

The multiplexer array has different time-delays between its outputs and the combinatorial logic of the different phases. These delays cannot be completely eliminated but are inherently minimized and equalized due to the symmetrical structure of the module and the aforementioned tight place-and-route procedure. As discussed in Section I, the target application of this module is multiphase platgforms with dual-loop compensation schemes in which the controller is capable of generating individual duty-cycle per-phase to compensate for any nonidealities, including uneven interconnect path delays.

As described in Section II, a single delay-line is shared between all phases to reduce the overall silicon area and to achieve highly matched characteristics between phases. The multiplexer array produces the time-delayed replicas of $clk_{\rm base}$ for all active phases from the same delay line, as illustrated in Fig. 5. Since the equivalent capacitance at the DE[x] nodes grows with the number of realized phases, logical-effort (drive) analysis has been carried out to minimize its effect on t_{de}. Here, a standard-cell based buffer string has been added between these nodes and the multiplexer array inputs to ensure proper drive capabilities, thus maximize the time resolution of the HR-DPWM. Therefore, additional phases can be added without any resolution penalty assuming the buffer string's drive capabilities are sufficient.

IV. Simulation Case Study

Using the analysis and observations from the previous sections, a set of simulations have been conducted using PSIM (PowerSim Inc.) to evaluate the HR-DPWM functionality in closed-loop operation of a multiphase buck converter, as illustrated in Fig. 7.

An average-current mode control (ACM) scheme has been realized, based on a dual-loop architecture. A timing sequence diagram for the ACM controller is presented in Fig. 10 indicating the timing locations for the sampling operation of the output

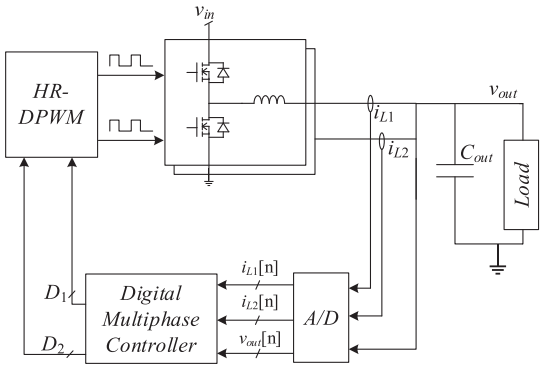


Fig. 7. Conceptual block diagram of a current mode controlled multiphase buck converter.

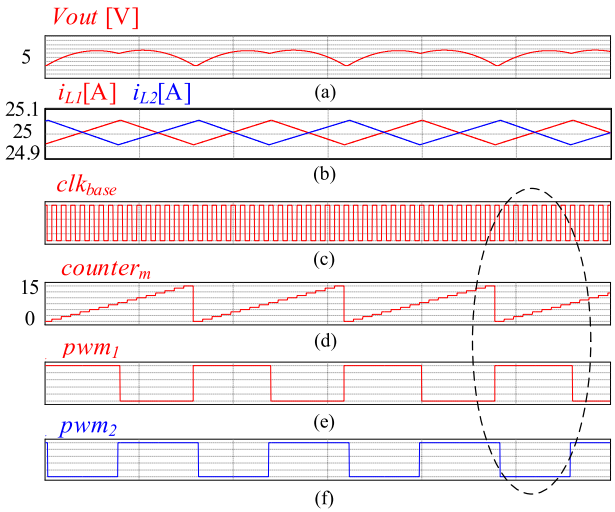


Fig. 8. Two-phase interleaved operation of a multiphase buck converter. (a) Output voltage. (b) Inductor currents. (c) clk_{base} signal. (d) $\mathrm{Counterm_m}$ signal. (e) Leading PWM signal $\mathrm{PWM_1}$. (f) 180° phase-shifted PWM signal $\mathrm{PWM_2}$. Zoomed-in view of the marked section is shown in Fig. 9.

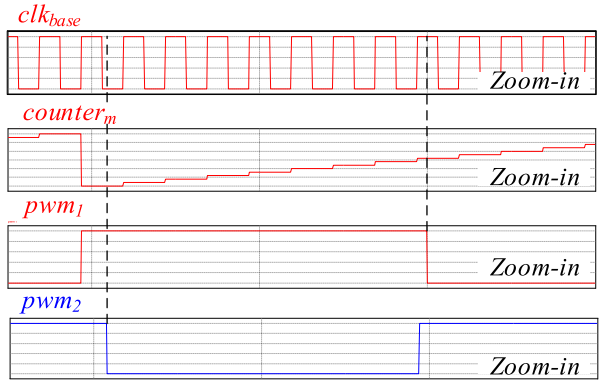


Fig. 9. Zoomed-in view of a portion of a switching cycle, as marked in Fig. 8.

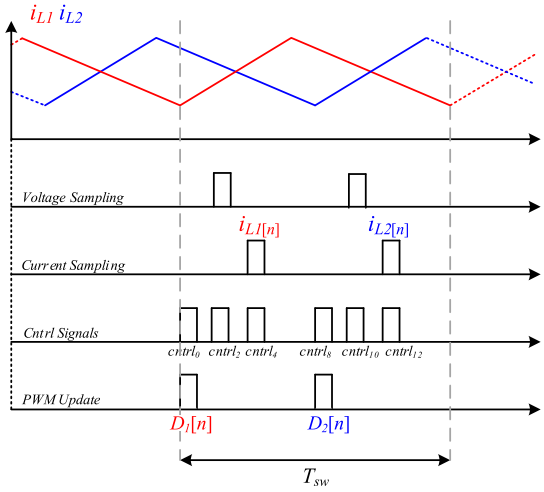


Fig. 10. Multiphase average current mode controller timing diagram.

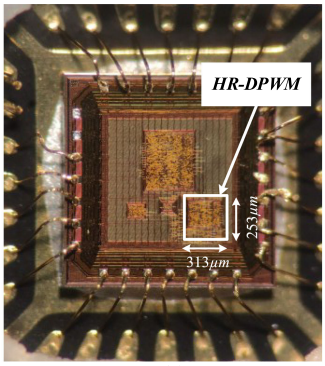
voltage and the inductor currents (i_{L1}, i_{L2}) as well as the update instances of the duty-cycle commands at the beginning of each phase. The outer voltage-loop creates a reference for the average inductor current value i_L[n]. The current error signal for each phase is calculated by comparing i_L[n] and the sampled value of the inductor current (see i_{L1}[n] and i_{L2}[n] in Fig. 7). The inner current-loop uses the current error signal to generate a duty-cycle command, which is the input to the HR-DPWM. The inherent current-sharing attributes of this control scheme results in improved thermal performance compared to conventional voltage-mode control. Analysis of average current mode control along with all practical realization considerations has been studied in detail in previous studies [5], [10].

Interleaved two phases operation of a multiphase buck converter is shown in Fig. 8 for an input voltage of 10 V and regulated output voltage of 5 V. clk_{base} signal is generated, as illustrated in Fig. 5, with $N_{DE} = 256$ ($l = 8$) and the switching frequency of the multiphase converter is calculated using (4) with $N_{\mathrm{sw}} = 16$. Different duty-cycle commands are produced by the controller to compensate for any variations or mismatches between the active phases. Here, a 20% mismatch is inserted deliberately between the power-stages' passive components and the transistors' R_{DSon} values. Such mismatch affects the ripple and the natural current balancing of the multiphase system. For such scenario, the average current mode controller produces different duty-cycle commands for the two phases, which will allow verification of the HR-DPWM capabilities to produce high-resolution interleaved PWM signals with independent on-time settings.

The output voltage is well-regulated at 5 V while maintaining accurate current sharing between the two active phases, as shown in Fig. 8(a) and (b). The clk_{base} and the $counter_m$ signals along with the resultant PWM signals, $\mathrm{PWM_1}$ and $\mathrm{PWM_2}$, are illustrated in Fig. 8(c)—(f). As can be seen in the zoomed-in view in Fig. 9, the falling-edge instance of each PWM signal compared to clk_{base} is independently determined by the LSBs of its corresponding duty-cycle command.

V. Experimental System Implementation and Validation

The multiphase HR-DPWM has been designed and fabricated in 0.18 μm 5 V CMOS process, as a part of a larger study. The chip micrograph is shown in Fig. 11(a), and Fig. 11(b) depicts the fabricated IC on a printed circuit board (PCB). The effective



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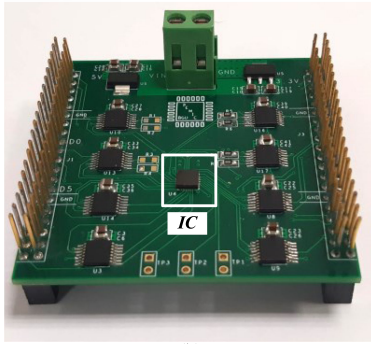
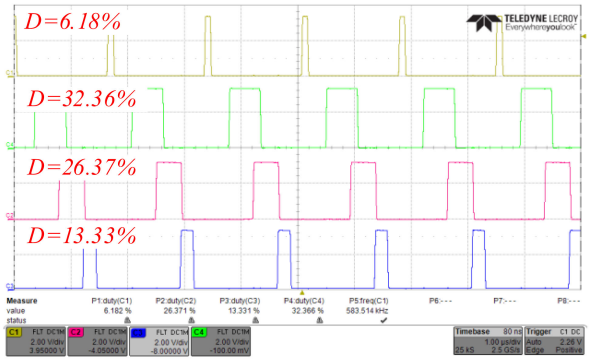


(b)

Fig. 11. (a) Micrograph of the fabricated controller IC and the DPWM module highlighted. (b) Fabricated IC PCB test board.



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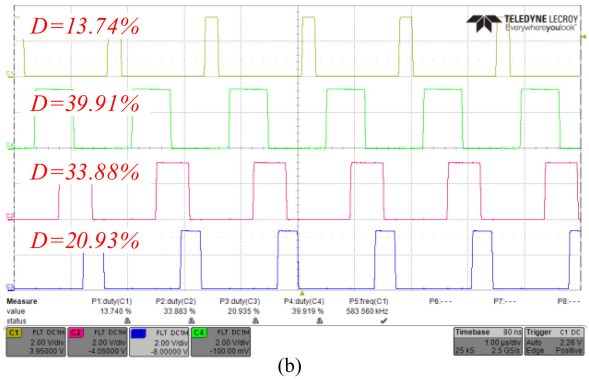


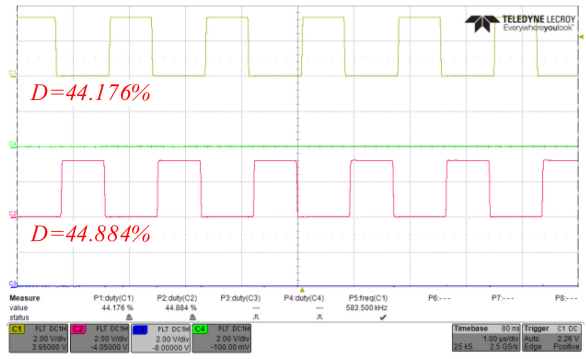
(b)

Fig. 12. Interleaved operation of the four-phase 13-bit HR-DPWM operating in switching frequency of 583.5 kHz, time scale 1 μs/div.

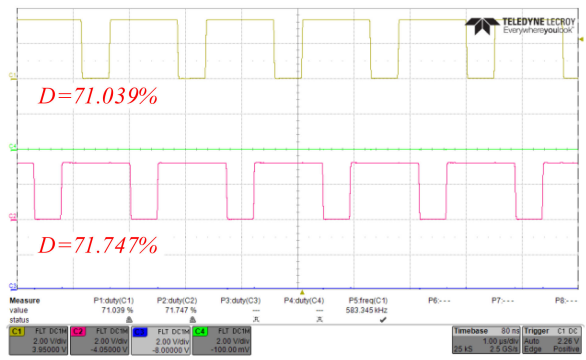
silicon area of the HR-DPWM module is 0.08 mm.^{2} The maximum number of active phases is set to $N = 4$. The clk_{base} signal is generated by a 256 delay-elements based ring-oscillator ($N_{DE} = 256$) and the duty-cycle command is 13-bit long. According to (2), the eight LSBs are the input to the multiplexer array to generate the time-delayed replica of clk_{base} with time resolution of a single delay element, the four MSBs are used to generated the clock-based signals and the remaining 1-bit of the duty-cycle command is used by the output logic blocks for the final stage of the high-resolution PWM signal generation, as described in Section II.

Fig. 12 demonstrates the HR-DPWM operation when all phases are active and different duty-cycle is assigned for each phase. The assigned duty-cycle values are $D_1 = 1012$, $D_2 = 5300$, $D_3 = 4320$, and $D_4 = 2182$ for the experimental setup of Fig. 12(a) and $D_1 = 2250$, $D_2 = 6538$, $D_3 = 5550$, and $D_4 = 3428$ for the setup of Fig. 12(b). As can be seen, the phase-shift between each phase and its consecutive is 90°, in agreement with (5) for the case of $N_{\text{sw}} = 16$ and $N_{ph} = 4$. The resulting switching frequency is 583.5 kHz, which for the case in hand results in effective duty-cycle update frequency of 2.3 MHz, according to (3).

Fig. 13(a) and (b) demonstrates the operation of two interleaved phases with different duty-cycle commands. As can be seen, the phase-shift between each phase is 180°, in agreement with (5) for the case of $N_{\text{sw}} = 16$ and $N_{ph} = 2$. Here, the difference between the assigned duty-cycle commands in each experimental setup is 116. As can be seen, the difference between the measured duty-cycle of the generated PWM signals remains



(a)



(b)

Fig. 13. Interleaved operation of two-phases with 13'd116 difference in their duty-cycle command. (a) D_1 = 13'd7236, D_2 = 13'd7352, and time scale 1 μs/div. (b) D_1 = 13'd11636, D_2 = 13'd11752, and time scale 1 μs/div.

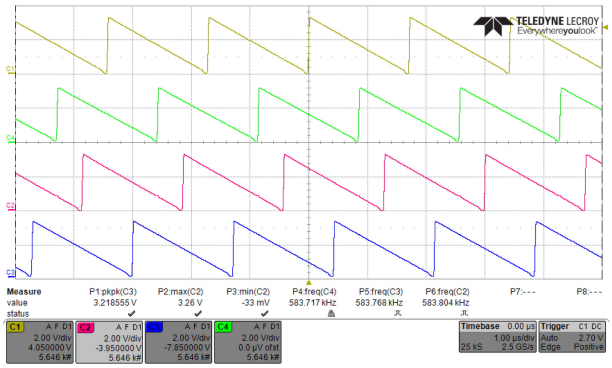


Fig. 14. Measured linearity of the four-phase HR-DPWM.

constant, regardless of the operating point. The resolution of the HR-DPWM is measured in terms of picoseconds and is a function of the delay-elements comprising the shared delay-line (see Fig. 2). It is defined as the smallest on-time difference between two PWM signals with consecutive duty-cycle commands (i.e., 1 LSB difference). To avoid measurement errors due to scope bandwidth limitations the time resolution is extracted in a two-step procedure. First, the on-time is measured for a known duty-cycle command and divided by the decimal value of D – this yields the average time resolution for the given operating point. This is carried out for multiple operating points as can be seen in Fig. 13(a) and (b) to validate that the time resolution of the module is not a function of the duty-cycle settings. Second, the on-time difference between two different phases is calculated and divided by the difference in the duty commands to validate that the time-resolution is consistent across all phases. In this realization, the time resolution of the fabricated 4-phase HR-DPWM is approximately 200 ps. This property can be further enhanced if a more advanced fabrication process is used (such as a deeper submicron process) with minor modifications or none to the HDL source code.

Fig. 14 demonstrates the monotonicity and linearity experimental verification of the fabricated IC. Ideally, for the smallest change in the duty-cycle command (i.e., 1 LSB) the generated PWM signal's on-time will increase or decrease by the delay of a buffer-cell (t_{de}). In this article, this is verified by increasing the duty-cycle command by 1 every 100 switching cycles in a cyclic manner and averaging over time. Theoretically, a right-triangular waveform is expected with constant slope—correlated to t_{de}. As can be seen in the experimental results of Fig. 14, all four phases have the same linearity and monotonicity characteristics, validating the design concept of a single synchronization source for multiphase modulators.

VI. Conclusion

A new architecture for HR-DPWM has been presented and verified through simulations and experimental data. The module generates multiple interleaved output phases, all synchronized and derived out of a single reference source. Due to the symmetrical structure of the module and the utilization of a single delay-line, any statistical error or jitter between phases is inherently minimized, since it applies for all phases in the same manner. Per-phase assignment of independent duty ratio settings is carried out by simple combinatorial logic utilizing a shared delay line resulting in PWM signals with highly matched characteristics with resolution of a single delay element. The number of active phases, switching frequency, and time-delay between phases can be set on-the-fly without any hardware modifications. The solution is compact, scalable, and is based on standard cells alone, without any custom design modules, making it an attractive candidate for integration in modern digital controller ICs.

Experimental results of a four phase, 13-bit HR-DPWM are provided, demonstrating highly linear characteristics with time resolution of 200 ps and excellent matching between all phases. The HR-DPWM has been designed in a digital-oriented approach and implemented on a 0.18 μm 5 V CMOS process resulting in total silicon are of 0.08 mm.^{2}

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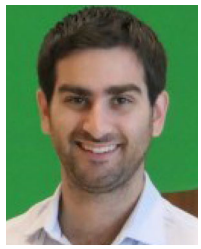

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