All-Digital Integrated Variable-Frequency Variable-Duty-Cycle Modulator With Single-Element Resolution and Single-Cycle Convergence

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***Abstract*— This article introduces a new architecture for an all-digital high-resolution (HR) variable-frequency variable-duty-cycle modulator for low-power and area-sensitive applications. Constructed through digital standard-cell delay-line (DL) and simple combinatorial logic, the modulator produces pulse width modulated signals with time-resolution of a single delay-element (DE) for both modulation parameters, thus making it a promising candidate for integration in hybrid controllers of high-frequency switched mode power supplies (SMPSs). Since the entire architecture is realized through standard cells, the solution also scales with fabrication technology and is described in hardware description language (HDL) which translates onto hardware using an automated process. The modulator has been designed on a 0.18-μm 5-V CMOS process, totaling 0.18 mm^2 of silicon area as well as on an Altera V field programmable gate array (FPGA) to demonstrate the versatility of the architecture. Experimental results of the FPGA prototype are provided as well as post-layout simulations of the ASIC realization for a variety of mitigation sequences demonstrating single-cycle convergence and time-resolution of 220 and 200 ps, respectively, with excellent linearity characteristics.**

***Index Terms*— ASIC, delay line (DL), frequency hopping, frequency modulation, high resolution (HR), integrated circuits, pulsewidth modulation (PWM).**

I. Introduction

DIGITAL architectures and realizations of controllers for switched mode power supplies (SMPSs) have been in pursuit by both industry and academia for many years [1], [2], [3], [4], [5], [6]. Beyond the conventional attributes of flexibility, scalability, and noise immunity, this approach allows for the assimilation of complex control laws and algorithms to enhance transient performance and optimize steady-state operation [7], [8]. Such control schemes may involve hybrid frequency and duty-cycle modulation to improve efficiency [9], [10], perform regulation tasks [11], [12], or execute convoluted mitigation sequences [13]. Following the miniaturization trend of IoT devices and portable consumer electronics requiring point-of-load (PoL) power conversion, such controllers are expected to operate at high switching frequencies with very high time resolution to fully exploit these state-of-the-art control algorithms [14], [15].

Synchronous realizations of such controllers conventionally rely on high-speed central processing units (CPUs) to execute the control law which allows relatively simple and straightforward reconfiguration capabilities [16], [17] but results in expensive and power-hungry solutions with large silicon area. This is since high-frequency synchronous operation requires highly balanced clock distribution networks realized through complicated clock tree synthesis (CTS) algorithms. Moreover, such controllers typically incorporate extensive periphery resources such as phase lock loops (PLLs), digital clock managers (DCMs), and memory modules. Here, the control-oriented submodules, such as the compensation units, pulsewidth modulators, sampling blocks, and so on, exploit the high-frequency clock to attain the required time-resolution attributes for the regulation tasks. An alternative approach relies on hardware accelerators designed to execute specific tasks thus achieving optimized silicon utilization with low power consumption [3], [18]. These controllers operate in an asynchronous manner, i.e., not synchronized to an external clock, by realizing a handshake algorithm between consecutive modules along the control loop [3], [18], [19]. Therefore, low-frequency clocks can be used to control the data flow between submodules while high-time resolution or high-speed capabilities are generated within specific blocks. For example, conventional PWM modulators are considered power-hungry and costly modules since their high-resolution (HR) attributes are derived from their internal high-frequency clock generation circuitries. Nowadays, efforts are made to obtain HR characteristics by incorporating dedicated modules and integrated structures to make high-frequency clocks redundant.

Pulsewidth modulators which are key components of modern controllers [20], [21], [22] can potentially benefit more than other hardware accelerators from such an approach due to their extremely HR attributes. Their respective pulsewidth modulation resolution must comply with the regulation accuracy and be higher than the analog-to-digital converter (ADC) to avoid limit cycle oscillations [23]. Moreover, these modules are characterized by their frequency and duty-cycle range,

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monotonicity and linearity characteristics, and dynamic performance. Therefore, in the context of digitally controlled low-volume SMPS, a miniaturized HR PWM modulator with lean silicon utilization capable of generating gating signals with adjustable frequency and the duty cycle is an essential building block to achieve the regulation goals.

Analog and mixed-signal PFM-PWM modulators have been perfected over the years with an emphasis on extended switching frequency range and resolution enhancement [24], [25]. These modulators are largely incorporated in analog controllers of resonant converters which utilize voltage-controlled oscillators (VCOs) with very HR attributes. However, the integration of complex analog solutions for the drive stage in low-power and area-sensitive applications such as IoT devices is not a viable option. Moreover, custom design of such modulators requires extensive redesign efforts when transitioning from one technology node to another and therefore are not generic and not suitable for cost-sensitive applications. On the other hand, digital PWMs (DPWMs) architectures offer a significant reduction in the overall cost and complexity metrics with implementation capabilities on programmable development platforms such as field programmable gate arrays (FPGAs) [26], [27], [28]. The conventional approach to implementing an HR digital pulsewidth modulator (HR-DPWM) is by a fast-clocked counter–comparator scheme [26]. Here, the required resolution and switching frequency determine the internal clock frequency. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n \cdot f_s$. This approach features a relatively small silicon area and low computational resources but may result in increased power consumption and complex design to realize the high-speed circuitry.

In order to enhance the resolution property of monolithic realizations, these architectures can be altered to include single [29], [30] or several [21] delay lines (DLs) to improve the duty-cycle resolution of the generated PWM signals. DL-based modulator architectures comprise $2^{N\text{DPWM}}$ DEs and a $2^{N\text{DPWM}+1}$:1 multiplexer which allows to enhance the time resolution while using the switching frequency as the modules' clock signal. This approach reduces power consumption but requires a large silicon area to realize $2^{N\text{DPWM}}$ DEs. For that reason, a combined architectural approach has been presented in the literature that uses both counter–comparator logic and DL structures to reduce area consumption without sacrificing resolution [29], [30]. For example, the monolithic HR-DPWM module presented in [29] achieves a time resolution of 200 ps for the duty-cycle attribute while the switching frequency resolution is bounded by the reference clock signal. Consequently, these modulators can be incorporated in constant switching frequency SMPS to enhance regulation capabilities but will result in limited improvement when integrated into resonant topology-based power supplies. Here, state-of-the-art control schemes require HR attributes for both control variables, i.e., switching frequency and duty-cycle [11], [12]. Resolution enhancement for FPGA-based realizations has been widely covered in the literature [21], [22], [31], taking advantage of modern FPGA resources such as multiport PLLs [32] and DCM modules [26], [27]. However, such an approach entails

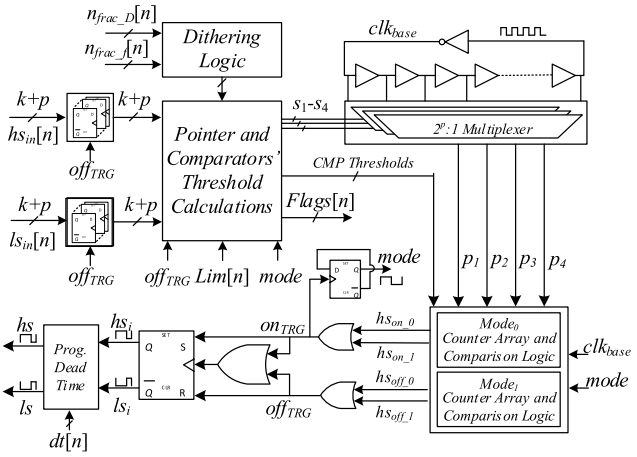


Fig. 1. Block diagram of the all-digital high-resolution variable-frequency variable-duty-cycle modulator.

significant redesign efforts when transitioning to ASIC and will result in high silicon utilization and power consumption due to the complexity of these modules.

Another approach for resolution enhancement relies on dithering algorithms rather than hardware modifications [33]. These algorithms are mainly used in digital controllers of resonant converters with high-quality factor networks for which the switching frequency is the main control variable [33], [34]. Here, frequency dithering is achieved by hopping the DPWM frequency between two neighboring values in a predefined manner such that the average frequency resolution exceeds that of a conventional DPWM. However, modern modulators cannot rely on dithering algorithms alone for resolution enhancement and usually employ dedicated hardware as discussed earlier. It would be advantageous to implement a dithering algorithm based on the HR modules of modern modulators to extend the resolution beyond that of a single delay element (DE)—this has been perused in this study.

The objective of this work is, therefore, to introduce a new HR variable-frequency variable-duty-cycle modulator (HR-VFVDM) for low-power high-frequency and volume-sensitive controller architectures, as shown in Fig. 1. Time-resolution of a single DE is obtained for both frequency and duty-cycle attributes of the generated PWM signals while ensuring single-cycle convergence operation. The HR-VFVDM does not utilize external clock resources, which makes it a promising candidate for integration in asynchronous digital controllers of high-frequency SMPS. Additional resolution enhancement is achieved through dithering of both the switching frequency and duty-cycle attributes. The modulator's architecture is DL-based and is entirely described in hardware description language (HDL) using standard-cell libraries without extensive custom design to allow fast adaption and implementation in various development or fabrication platforms. It is a further objective of this article to discuss specific realization aspects of DL-based architectures on programmable fabrics such as FPGAs and as an integrated module in an ASIC solution.

The rest of this article is organized as follows. Section II describes the HR-VFVDM architecture, covers its principle of operation, and discusses the resolution enhancement algorithm

through dithering. Section III details a case study of the new HR-VFVDM incorporated in a hybrid digital controller for a HB-LLC resonant converter. Section IV details practical implementation issues along with design and realization guidelines. Post-layout validation and experimental results are provided in Section V. Section VI concludes this article.

II. High-Resolution PFM-PWM Modulator

A. Architecture and Principle of Operation

The HR-VFVDM operates in an asynchronous manner [29], i.e., not synchronized to an external clock, and therefore its architecture is meticulously tailored to the signal paths between its submodules, as shown in Fig. 1. It comprises a register-based input stage that samples the PWM signals' on-time commands ($hs_{in}[n]$ and $ls_{in}[n]$) and dead-time ($dt[n]$) on a cycle-by-cycle basis followed by a digital computational logic that produces two sets of internal signals: s_1–s_4 and *CMP Thresholds*. The former is used as input to the ring-oscillator multiplexer array which yields time-delayed replicas of its propagating signals (p_1–p_4) while the latter is fed into the counter–comparator submodules. The *CMP Thresholds* are derived from the instantaneous on-time commands, hs_{in} and ls_{in}, as their respective k-MSBs and are utilized as the thresholds for the counter–comparator modules which produce internal signals that mark the initiation and termination of each switching-cycle segment (hs_{on} and hs_{off}). These signals are processed by the output logic block and the DL-based dead-time module to produce the resulting PWM signals, *hs* and *ls*.

The reference clock signals of the HR-VFVDM counter–comparator submodules are not confined to a specific location in the ring-oscillator as in conventional realizations but rather modified on a cycle-by-cycle basis by the internal computational blocks to accommodate the instantaneous gating commands, $hs_{in}[n]$ and $ls_{in}[n]$. This is carried out by the multiplexer array that provides direct access to all propagating signals in the DL as shown in Fig. 1, which is the enabler for the HR attributes of the modulator. Therefore, each segment of the generated PWM signal is individually produced with the time resolution of a single DE, i.e., the falling- or rising edges of the PWM signals *can be positioned without any limitations along the DL*.

The single DE resolution is derived from the ability to utilize the propagating signals of the DL via the multiplexer array in a stable and consistent manner. This highly depends on the ability to stabilize the counter–comparator modules' inputs prior to a new switching-cycle initiation. Since a non-negligible time interval is required to perform the required calculations and to allow the counter–comparator inputs to stabilize according to the instantaneous gating command, two sets of counter–comparator submodules are realized and used interchangeably in two modes of operation named $mode_0$ and $mode_1$. When the $mode_0$ hardware is used to produce the HR PWM signals, the inputs to its counterpart submodule are calculated and vice versa. This ensures that all input signals to the multiplexer array (s_1–s_4) and its outputs (p_1–p_4) are valid and stable upon a new switching-cycle initiation.

The $k + p$ bit long on-time commands, $hs_{in}[n]$ and $ls_{in}[n]$, are sampled periodically and stored in dedicated registers (see Fig. 1). The first k bits form the coarse section of the command dictating the required number of full-cycle count while the remaining p bits represent the fine-tuning addition in accordance with the DL length, i.e., 2^p DEs. Therefore, the switching frequency can be expressed as

$$f_{sw} = \frac{1}{(hs_{in} + ls_{in}) \cdot t_{de}} \tag{1}$$

and the duty-cycle as

$$D = \frac{hs_{in}}{hs_{in} + ls_{in}} \tag{2}$$

where hs_{in} and ls_{in} are the decimal values of $hs_{in}[n]$ and $ls_{in}[n]$, respectively. The "k" and "p" are chosen with respect to the desired range of switching frequencies and offer a tradeoff between silicon utilization, time resolution, and power consumption. Increasing "p" will result in a lower switching frequency for the internal clock signal (clk_{base}) but will entail a larger DL structure and accommodating multiplexers which will negatively affect the time resolution of the modulator. Consequently, decreasing its length will result in a faster internal clock and increased power consumption. The "k" value, which dictates the maximal number of full-cycle counts, sets the lower boundary for the frequency of the generated PWM signals and is chosen according to the target application. Therefore, the minimal switching frequency is derived for a given "k" and "p" values by applying (1). To comply with the maximum allowed switching frequency of a given target application, the HR-VFVDM includes a programmable set of limitations, marked as $Lim[n]$ in Fig. 1, which prohibits the execution of gating signals with out-of-scope frequency. This safety mechanism is essential since the drive commands are generated by the preceding controller modules such as compensators or filters, which are prone to inaccuracies due to noise, sampling, or calculation errors. Therefore, the switching frequency range of the HR-VFVDM can be written as

$$f_{sw} \in \left[\frac{1}{2^{k+p+1} \cdot t_{de}}, \frac{1}{Lim \cdot t_{de}} \right] \tag{3}$$

where *Lim* is the decimal value of $Lim[n]$ in Fig. 1.

In this modulator architecture, the fine-tuning mechanism introduces a delay of up to $2^p t_{de}$ between the counter–comparator triggering signals, p_1–p_4. This is carried out by utilizing the least significant bit (LSB) sections of the sampled signals to calculate the multiplexer-array inputs (s_1–s_4) with respect to their previous values according to

$$\begin{cases} s_1 = s_4 + hs_{in}[p-1:0] \\ s_2 = s_4 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \\ s_3 = s_2 + hs_{in}[p-1:0] \\ s_4 = s_2 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \end{cases} \tag{4}$$

where s_1–s_2 are associated with $mode_0$ and s_3–s_4 with $mode_1$. The multiplexer array outputs are fed into the counter–comparator submodules and act as their respective clock signals with a frequency of

$$f_{base} = \frac{1}{2^{p+1} \cdot t_{de}}. \tag{5}$$

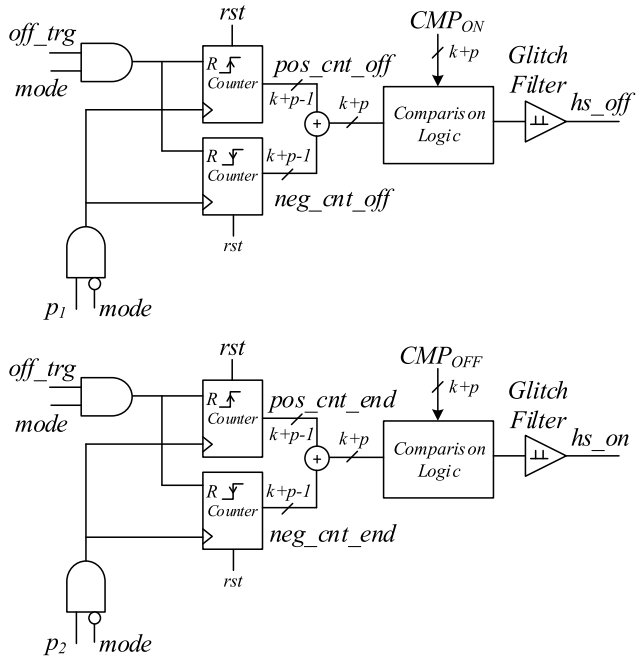


Fig. 2. Dual counter–comparator logic comprising the $Mode_0$ and $Mode_1$ submodules.

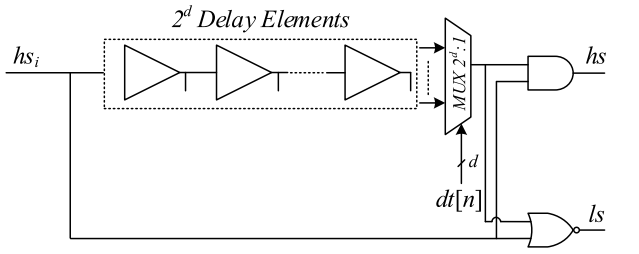


Fig. 3. Schematic of the DL-based programmable dead-time module.

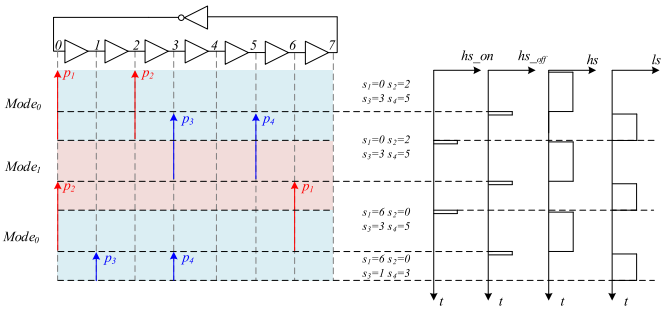


Fig. 4. Illustrative example of the operation of an HR-VFVDM with $p = 3$, hs_in[2:0] = 3'b001, and ls_in[2:0] = 3'b010.

The hardware for each mode comprises two sets of positive- and negative-edge triggered modules which are incremented at the rising and falling edges of their respective clock signals, p_1–p_4. The dual comparator structures followed by the comparison logic blocks of $mode_0$ are shown in Fig. 2. As can be seen, this submodule is deactivated when the *mode* signal is logic high and is reset at the falling edge of the *hs* signal, i.e., at the positive edge of *off_trg* signal. The p_1- and p_3-fed counter–comparator modules control the falling edge of the PWM output for $mode_0$ and $mode_1$, respectively, while p_2 and p_4 are utilized in the same manner to control its rising-edge instance. This is carried out by comparing the internal counters' values with the MSB sections of the on-time commands (*CMP Thresholds*) yielding the hs_{on} and hs_{off} signals as shown in Fig. 2 for the $mode_0$ operation segment. Accordingly, the internal high-side PWM signal (hs_i) rises at the beginning of each switching cycle with the positive-edge of hs_{on} and remains high until hs_{off} resets the SR-FF thus driving the low-side PWM signal (ls_i) with logic high value (see Fig. 1).

To facilitate power-stage switching operation without shoot-through and to comply with state-of-the-art efficiency optimization procedures by dead-time adjustments [35], [36], the HR-VFVDM supports on-the-fly dead-time modifications. This attribute is essential to achieve zero-voltage switching (ZVS) in resonant topologies, in particular, when the input voltage and loading conditions vary over time. For that reason, in state-of-the-art controller architectures, the dead time is a tunable variable that is dynamically modified to enhance efficiency, typically by locking into the minimum time period required to achieve ZVS. Therefore, an all-digital DL-based programmable dead-time module is included in the output stage of the HR-VFVDM. It consists of a string of 2^d DEs feeding a 2^d:1 multiplexer, as shown in Fig. 3. The internal signal hs_i is passed through the programmable dead-time module which dictates the time interval between the resulting *hs* and *ls* signals based on the sampled $dt[n]$ value with a time-resolution of a single DE.

The HR-VFVDM utilizes a single DL structure to obtain HR attributes as well as to control its internal submodules such as the counter–comparators blocks and sampling units. To allow synchronization with external controller modules, such as ADC, compensators, and so on, the modulator produces several flag signals to indicate key time locations such as the initiation of a new switching cycle, the falling edge of the high-side PWM signal, etc. (see Fig. 1). The controller uses these signals to control the flow of data between its submodules. This concept is discussed in [29] and [37] and used in the simulation case study of Section IV.

The operation of the HR-VFVDM and the pointers' movement along the DL are demonstrated in the illustrative example of Fig. 4 for a case of $p = 3$ and different on-time commands for the two PWM segments. Here, the LSB section of hs_in[n] is 3'b001 which results in an added time interval of t_{de} to the first segment of the PWM signal. This is carried out by positioning the p_1 and p_3 pointers one DE apart from p_4 and p_2, respectively. In a similar manner, the LSB section of ls_in[n] is 3'b010 which results in positioning p_2 and p_4 two DEs apart from p_1 and p_3, respectively, yielding a $2t_{de}$ extension to the *ls* signal. The s_1–s_4 values are calculated on a cycle-by-cycle basis according to (4) thus not confining the initiation signal, *hs_on*, to a fixed position in the DL. Moreover, the pointers calculations are carried out at the rising edge of the *hs_off* signal, i.e., at the falling edge of the *hs* signal, which ensures steady inputs to the ring-oscillator multiplexer-array module in the succeeding switching cycle.

Logical simulations carried out in QuestaSim for a 13-bit HR-VFVDM are shown in Fig. 5. Here, the DL consists of 128 DEs ($p = 7$) and the multiplexer array comprises four 2^7:1 multiplexers. The inputs of the module, i.e., $hs_{in}[n]$ and $ls_{in}[n]$, are specified at the top of the timing diagram along with the

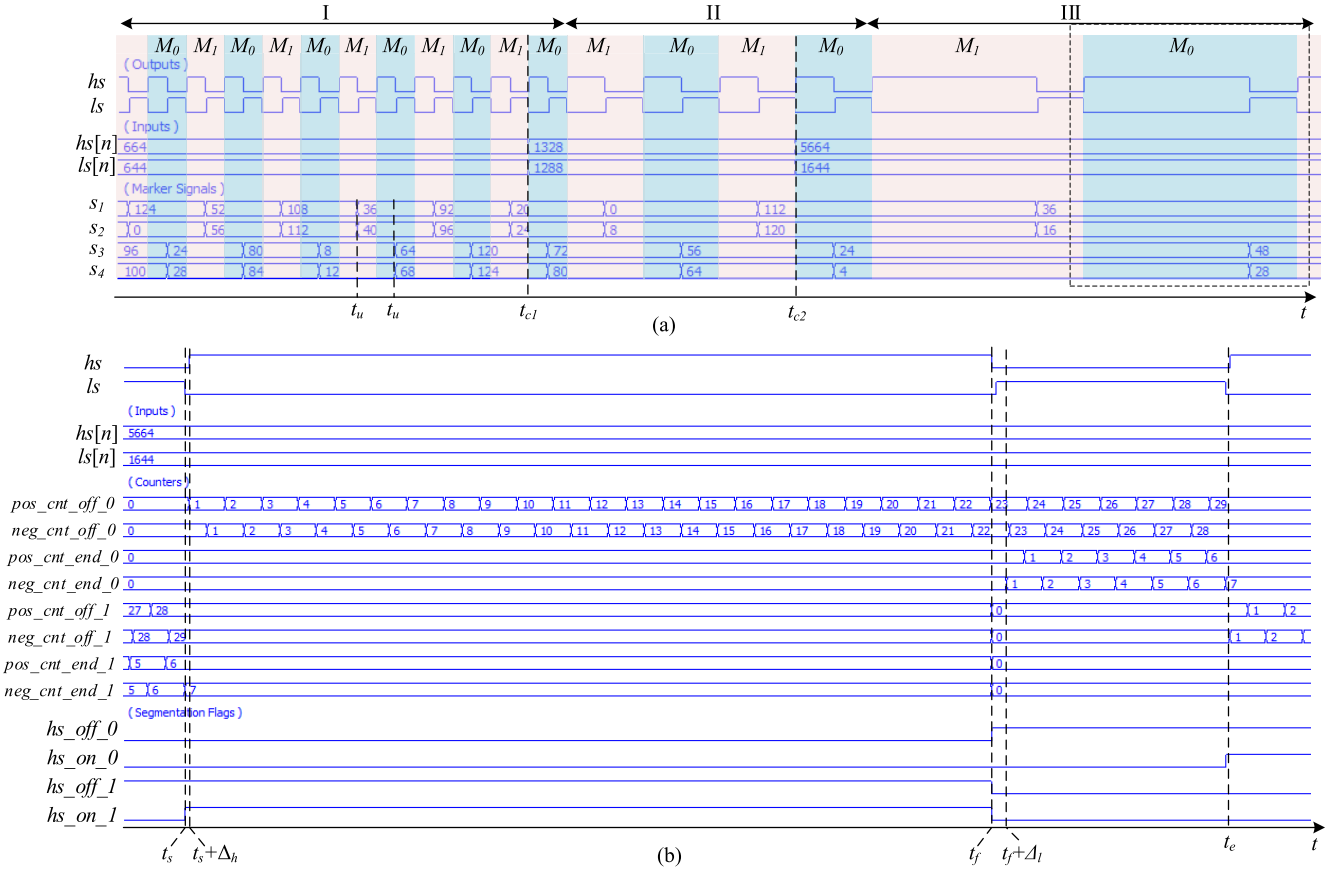


Fig. 5. Logical simulations of the HDL code carried out in QuestaSim. (a) Steady-state and transition scenarios. (b) Zoomed-in view on the counter–comparator internal signals.

mode status ($mode_0$ or $mode_1$). For simplicity reasons, the dead time is kept constant and equals 63 DEs.

Here, three exemplary switching scenarios are shown, demonstrating the single-cycle convergence and the HR attributes of the modulator: steady-state, switching-frequency modification with constant duty-cycle, and a stepwise change in both switching-frequency and duty-cycle commands. According to (4), the fine segments of the on-time commands are derived and equal 7'd24 and 7'd4 for the high-side and low-side drive signals, respectively. The coarse segments are derived in a similar manner and equal 5'd2 for both the high-side and low-side drive signals. As can be seen, s_1–s_4 signals are interchangeably updated every switching cycle according to (4) at the falling edge of hs_i signal, marked as t_u instances in Fig. 5. The first change in the on-time commands, marked as t_{c1}, maintains the duty-cycle and decreases the switching frequency by a factor of two. In this time interval, marked as Section II in Fig. 5, the on-time commands are 13'd1328 and 13'd1288 which maintain the duty cycle at 50.7%. To best showcase the capabilities of the HR-VFVDM, both the duty-cycle and switching frequency attributes are abruptly modified at the time instance marked as t_{c2} from 13'd1328 and 13'd1288 to 13'd5664 and 13'd1644. As can be seen, the resultant PWM signals nor the internal control signals suffer from noncontinuities, and single-cycle convergence is achieved.

The zoomed-in view of Fig. 5(b) demonstrates the operation of the counter–comparator structures for the marked section in Fig. 5(a) with $hs_{in}[n]$ = 13'd5664 and $ls_{in}[n]$ = 13'd1664. Here, the MSB sections of the *hs* and *ls* commands are 6'd22 and 6'd6 and their LSB sections are 7'd12 and 7'd108, respectively. Upon termination of the preceding cycle at time instance t_c [see Fig. 5(b)] the *mode* signal is inverted and $mode_0$ hardware is activated. As shown in Fig. 2, the dual-edge counter–comparator structures are triggered by the internal p_1 and p_2 signals produced by the DL-multiplexer block. Their location along the DL dictates the time delay between each PWM segment termination [t_s and t_f in Fig. 5(b)] and the following counter update instances, Δ_h and Δ_l in Fig. 5(b), with single DE resolution. The former is calculated as $hs_{in}[6:0] \cdot t_{de}$ and the latter as $ls_{in}[6:0] \cdot t_{de}$, which for the case in hand equal 1.4 and 21.6 ns, respectively. As can be seen, the $mode_1$ hardware is deactivated and its internal counters are reset at the falling edge of the *hs* signal, marked as t_f in Fig. 5(b), to allow all internal logic sufficient settling time prior to the current switching-cycle termination at instance t_e.

B. Resolution Enhancement by Dithering

The frequency resolution, f_{res}, can be calculated as the difference between two consecutive period settings, $T_{sw}[n]$ and $T_{sw}[n]+1$ according to

$$f_{res} = \frac{1}{T_{sw} \cdot t_{de}} - \frac{1}{(T_{sw}+1) \cdot t_{de}} \approx t_{de} \cdot f_{sw}^2 \tag{6}$$

where the switching period equals

$$T_{sw} = hs\_in[n] + ls\_in[n]. \tag{7}$$

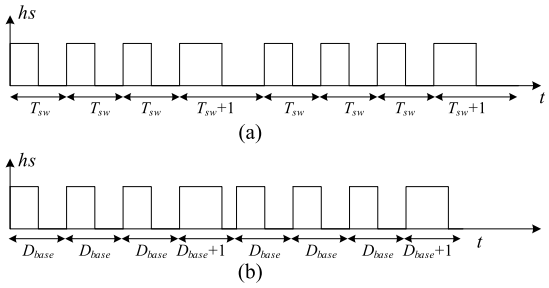


Fig. 6. Resolution enhancement by dithering. (a) Frequency dithering with $n_{frac} = 4$. (b) Duty-cycle dithering with $n_{frac} = 4$.

The duty-cycle resolution, D_{res}, is derived in a similar manner according to

$$D_{res} = \frac{hs+1}{T_{sw}} - \frac{hs}{T_{sw}} = \frac{1}{T_{sw}}. \tag{8}$$

Equations (6)–(8) highlight the resolution improvements achieved by the HR-VFVDM compared with conventional modulators and at the same time exemplify the inevitable resolution degradation at high switching frequencies.

Therefore, additional resolution enhancement at high switching frequencies is facilitated in this study by dithering the HR-VFVDM on-time commands at a defined rate, varied by the desired accuracy. The dither factor, n_{frac}, dictates the number of switching cycles needed to achieve the desired fractional frequency or duty-cycle ratio as well as the dithering range. In this study, the dither factor may be assigned a negative value thus covering the entire range of switching frequencies and duty-cycle values between two consecutive PWM commands, bounded only by the dithering resolution. Duty-cycle resolution enhancement is achieved by keeping a constant duty-cycle ratio, D_{base}, for $|n_{frac}|$ switching cycles followed by a single cycle with a modified duty-cycle command, $D_{base} + \text{sgn}(n_{frac})$. Similarly, frequency resolution enhancement is carried out by dithering the HR-VFVDM period between T_{iw} and $T_{sw} + \text{sgn}(n_{frac})$. For example, if a $0.25\,f_{sw}$ resolution is required ($n_{frac} = 4$), the HR-VFVDM will generate a single $T_{sw} + 1$ period every four switching cycles as shown in Fig. 6(a). In a similar manner, duty-cycle dithering with the same factor is illustrated in Fig. 6(b). The resultant average frequency is calculated according to

$$f_{sw\_dit} = \frac{1}{\left[T_{sw}\cdot\left(n_{frac}-1\right)+\left(T_{sw}+1\right)\right]/n_{frac}\cdot t_{de}} = \frac{1}{t_{de}(T_{sw}+1/n)} \tag{9}$$

and its respective resolution according to

$$f_{res\_dit} = \frac{1}{t_{de}(T_{sw}+1/(n+1))} - \frac{1}{t_{de}(T_{sw}+1/n)} \approx \frac{t_{de}\cdot f_{sw}^2}{n\cdot(n+1)}. \tag{10}$$

The average duty cycle is calculated by

$$D_{dit} = \frac{hs\cdot(n-1)+(hs+1)}{n\cdot T_{sw}} = \frac{hs+1/n}{T_{sw}} \tag{11}$$

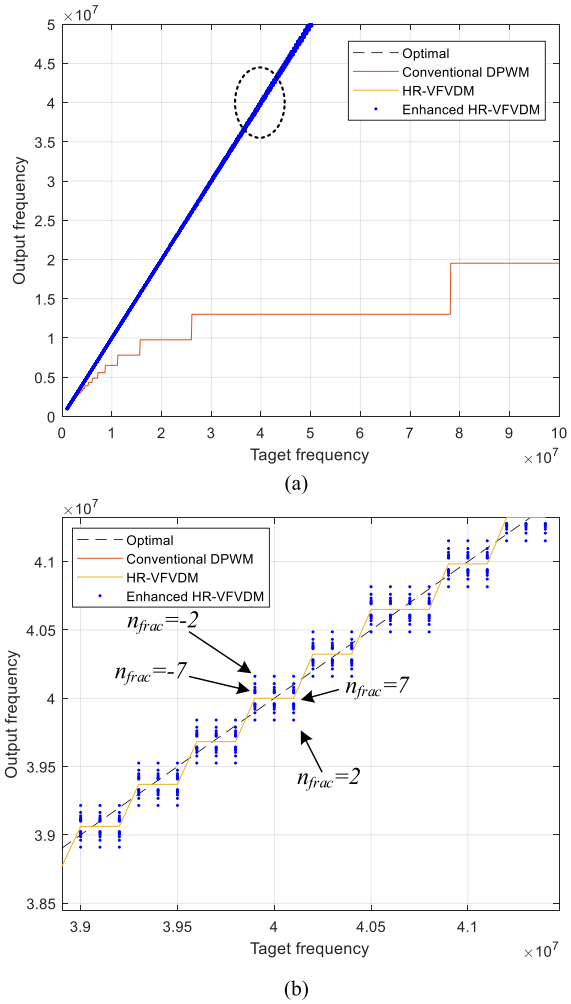


Fig. 7. (a) Possible output frequency values for a conventional DPWM, HR-VFVDM, and its resolution enhancement mode by 3-bit dithering. (b) Zoom-in view.

and the resultant resolution according to

$$D_{\text{res\_dit}} = \frac{hs+1/n}{T_{sw}} - \frac{hs+1/(n+1)}{T_{sw}} = \frac{1}{T_{sw}\cdot n\cdot(n+1)}. \tag{12}$$

Fig. 7 demonstrates the possible switching frequencies of a conventional modulator, an HR-VFVDM, and its dithering-enabled realization for a 3-bit resolution enhancement. Here, the reference clock signal is generated by a 64 DE-based ring oscillator with $t_{de} = 200$ ps. As can be seen, the conventional realization cannot exceed an output frequency of approximately 20 MHz obtained for a counter-based modulator with a base clock frequency of nearly 40 MHz that resets every other clock cycle. The zoomed-in view of Fig. 7(b) demonstrates the resolution improvement introduced by the HR-VFVDM and its enhanced mode of operation by dithering. Plotted in blue dots are the possible output frequency values for a 3-bit dithering operation ranging from $|n_{frac}| = 2$ to $|n_{frac}| = 7$ according to (9), showcasing the extended frequency range.

III. Simulation Case Study

Using the analysis and observation from Section II, a set of simulations has been conducted using [PowerSim, Inc.

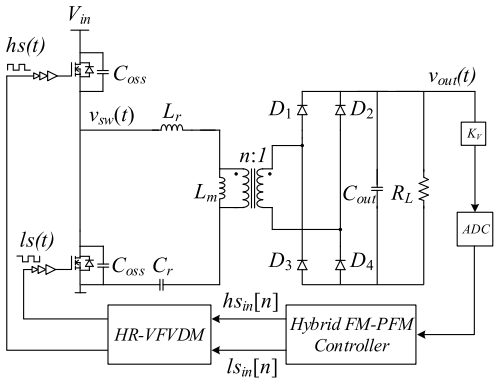


Fig. 8. HB-LLC resonant converter with hybrid FM-PWM controller and the HR-VFVDM.

(PSIM)] to evaluate the HR-VFVDM functionality in closed-loop operation of an HB-LLC resonant converter-based SMPS operating in the MHz range for low-power IoT devices [12] and to compare it with conventional modulator architecture. Here, tight output voltage regulation is achieved by simultaneously modifying the switching frequency and the duty cycle to extend regulation capabilities while utilizing simple control resources, as shown in Fig. 8. The HR-VFVDM ring-oscillator comprises 128 DEs with a propagation delay of 200 ps resulting in relatively low base clock frequency of approximately 20 MHz according to (5), making it an attractive candidate for low-power IoT devices. The transformer's turns ratio is 3:4 and the nominal values of the resonant capacitance, C_r, resonant inductance, L_r, and leakage inductance, L_m, are 0.68 μH, 37 nH, and 2 μH, respectively. Therefore, the resonant frequency equals 1 MHz according to

$$f_{res} = \frac{1}{\sqrt{L_r C_r}}. \tag{13}$$

The control scheme and the controller architecture are discussed in detail in [12].

Fig. 9(a) shows the soft-start procedure and closed-loop steady-state operation for a 5-V input to 3.3-V output HB-LLC resonant converter operating at the MHz range. Here, conventional PWM modulator architecture is realized with a time resolution of 50 ns according to (5). Once closed-loop operation is enabled, the output voltage is regulated by means of conventional frequency control. As can be seen in the zoomed-in view of Fig. 9(b), the switching frequency is adjusted by the controller and assigned two values during steady-state: 1 MHz and 1.052 MHz by comparing the internal counter value to two consecutive threshold values of 20 and 19, respectively. As can be seen, the DPWM frequency resolution is not sufficient for the desired zero-error bin which results in non-negligible low-frequency oscillations in the output voltage and resonant currents, i_{Lm} and i_r. The cyclic modification of the switching frequency between two consecutive values indicates a lack of correlation between the desired output voltage and the achievable set of conversion ratios. These oscillations significantly increase the required filtering efforts which directly translates into increased overall solution volume.

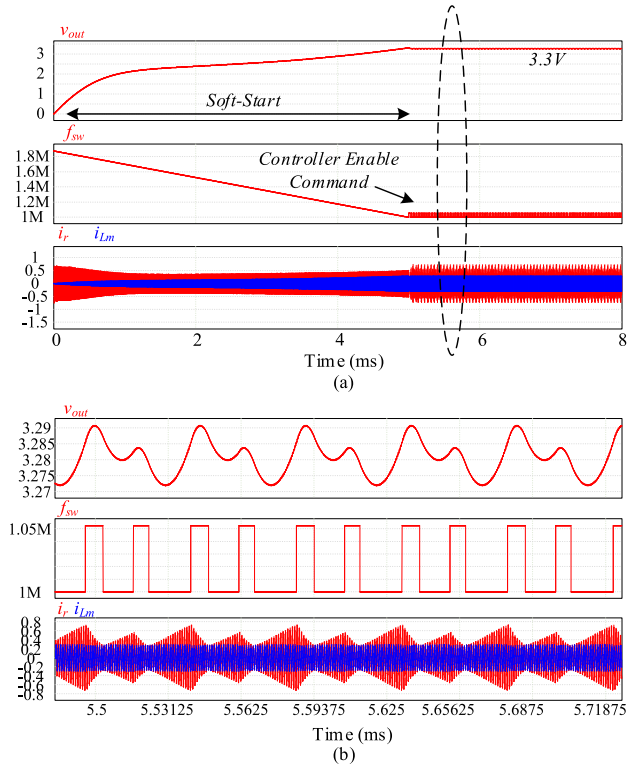


Fig. 9. Voltage mode controlled 5–3.3 V high-frequency HB-LLC resonant converter with conventional DPWM. (a) Soft-start and closed-loop operation. (b) Zoomed-in view.

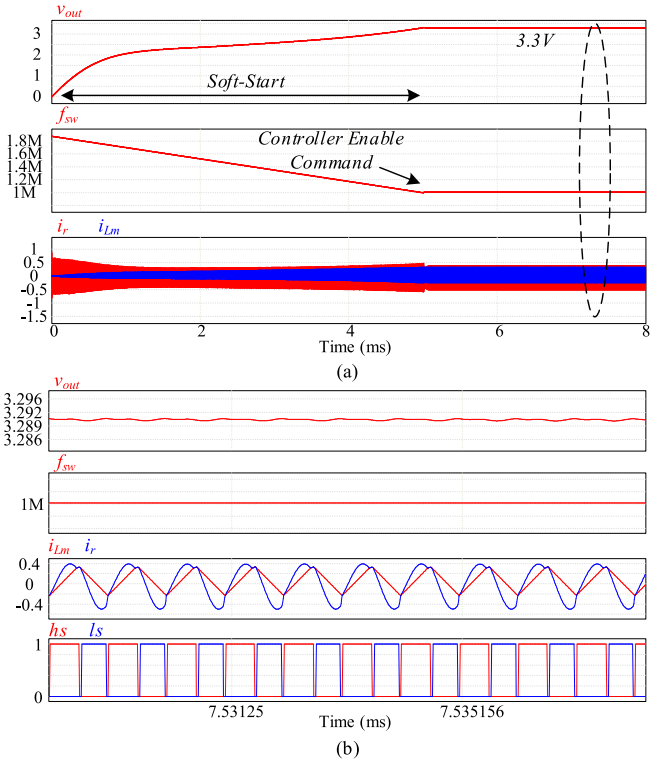


Fig. 10. Hybrid FM-PWM controlled 5–3.3 V high-frequency HB-LLC resonant converter with HR-VFVDM. (a) Soft-start and closed-loop operation. (b) Zoomed-in view.

Fig. 10 demonstrates the soft-start and closed-loop operation of the hybrid-controlled HB-LLC resonant converter enabled by an HR-VFVDM module, as shown in Fig. 8. Once the

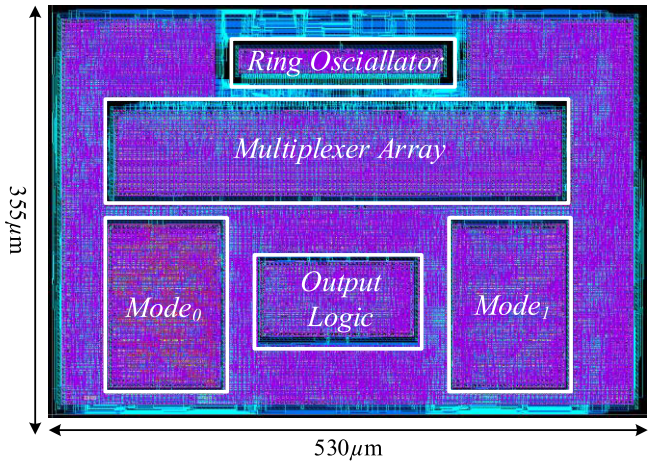


Fig. 11. All-digital HR-VFVDM layout in 0.18-μm 5-V CMOS process.

closed-loop operation is activated, the controller adjusts the switching frequency and the duty-cycle simultaneously with a single DE resolution to maintain the output voltage within its zero-error bin. The added duty-cycle modulation capabilities along with the improved frequency resolution [see (1)] result in tightly regulated output voltage without undesired oscillations. The zoomed-in view of Fig. 10(b) shows the output voltage and resonant currents along with the *hs* and *ls* gating signals operating at 1.008 MHz with a duty cycle of 54%.

IV. Cross Platform Implementation of DL-Based DPWMs

A. IC Implementation

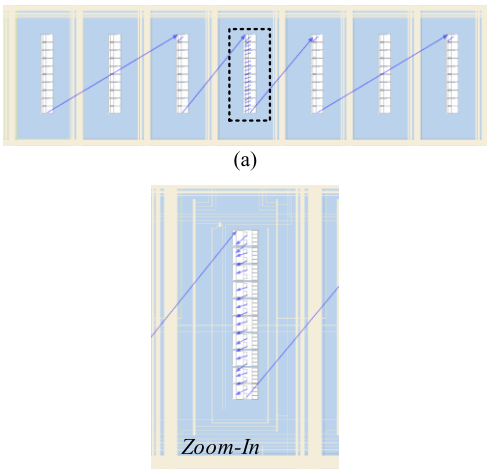
The realization of the HR-VFVDM relies on an automated digital implementation flow, using vendor's standard cells thus eliminating the need for extensive custom design. The ASIC implementation is described through three main steps. In the first step, each module is described in HDL as a standalone unit. This is done for the simplicity of the verification and functionality simulations. Then, each unit is translated into hardware using synthesis and timing verification tools resulting in an optimized gate-level representation. In this step, physical design constraints are enforced to ensure tight and dense realization of DL-based structures such as the ring-oscillator and high symmetry in modules such as the multiplexer-array which comprises several instantiations of the same submodule. In the third step, all units are integrated together into the higher hierarchy of the HR-VFVDM. Here, the automated place-and-route tools are instructed to position specific submodules adjacent to each other in accordance with the required data paths along with conventional area and timing constraints to achieve compact silicon realization without compromising on resolution. This prohibits the CAD tools to perform general area optimization but rather takes into account the asynchronous nature of the architecture and its structure as shown in Fig. 1. The resultant layout with an overall silicon area of 0.18 mm^2 is shown in Fig. 11. As can be seen, the layout encapsulates the core attributes of the design, among them the symmetry between $mode_0$ and $mode_1$ hardware, the adjacency of the DL and the multiplexer array, etc.

Integrated implementations of DL-based architectures require special attention in the design of their respective elementary DE, since it has an impact on their linearity and resolution attributes [27], [28], [38]. In DPWM architectures where the DL is used as a fine-tuning mechanism independent of the clock generation circuitry, relatively complex compensation structures are incorporated to adjust the time delay to the fundamental switching frequency to ensure the correct operation of the modulator and to account for process variations, temperature, and aging [39]. For example, a differential DE fed by a supply-insensitive replica biasing module is discussed in [38] and a delay-adjustable unit is utilized in the DPWM of [30]. To produce an all-digital realization while easing design complexity, a different approach is taken in this study in which the DL structure acts as both the internal clock generation circuitry as well as the modulator's fine-tuning module, as discussed in Section II. While the above-mentioned variations may affect the resultant time-resolution attribute of the HR-VFVDM, they will not jeopardize the correctness of its operation since the fine-tuning mechanism is inherently derived from the fundamental switching frequency. Since the modulator operates in a closed loop (for the target applications), any variation of its time resolution will be compensated by the digital control loop. Therefore, a symmetrical DE chosen from the stand cell library is sufficient to construct the DL module allowing dense and symmetrical placement as discussed earlier. TowerJazz power-management platform, as many other process design kits (PDKs), offers a symmetrical buffer cell that allows simple and straightforward implementation through HDL source codes. It should be emphasized that such a cell can also be designed as a standalone unit and included in the standard cell library for synthesis [40].

B. FPGA Implementation

The realization of DL-based architectures on programmable fabrics such as FPGAs largely follows the ASIC design guidelines with several key modifications. First, an in-depth investigation of the target FPGA should be conducted with emphasis on DL-based structures that can be exploited in the implementation of the ring oscillator or the programmable dead-time modules. For example, Xilinx Virtex FPGAs [41] include several custom-designed voltage-tolerant components (IODELAY) to perform HR delay adjustments for DDR interfaces that can be instantiated as part of the HR-VFVDM. Another resource found in modern FPGAs is the DCM module which enables clock frequency manipulations such as duplication, multiplication, division, and phase shifting [27]. Here, the phase-shifted replicas of the reference clock are utilized as delayed replicas for the purpose of fine-tuning. This approach results in highly linear and robust realization [27] but with a penalty of an extremely high-frequency reference clock due to the limited phase shifting capabilities. Moreover, such an approach may be limited due to available hardware resources and will entail additional design efforts during a transition to ASIC.

An alternative approach, pursued in this study, is realizing DL-based structures with carry-chain blocks [38] or simple look-up tables (LUTs) available in every programmable fabric



(a)

(b)

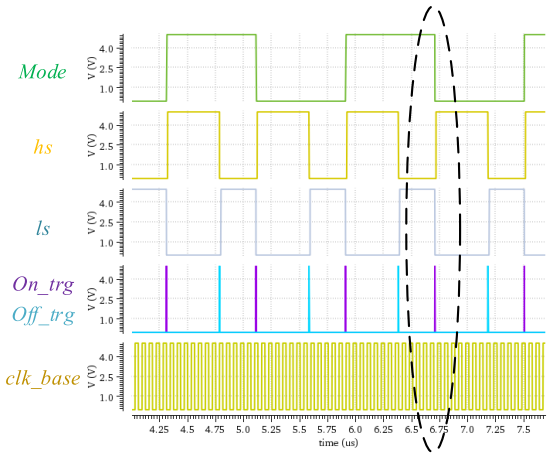
Fig. 12. (a) Manual placement of a DL structure in an Altera (Intel) Cyclone V FPGA. (b) Zoom-in view.

unit or with dedicated delay-cells that are typically instantiated to fix hold time violations in synchronous designs. For example, carry chain DL realizations exploit the low latency path traditionally used to propagate the carry bit between two consecutive adders. To ensure constant propagation delay regardless of specific DL realization, their location should be fixed and confined to a compact area. However, in most FPGAs, these cells are not found in all rows or columns of the mesh grid which results in gaps between routed regions of the DL, as can be seen in Fig. 12(a). Therefore, some degradation is expected in terms of time resolution due to the additional delay, an undesired phenomenon that can be minimized by positioning the submodules in adjacency according to the data flow. Shown in Fig. 12(b) is a zoomed-in view of a configurable logic block (CLB) and its internal routings between DEs realized as part of the ring oscillator.

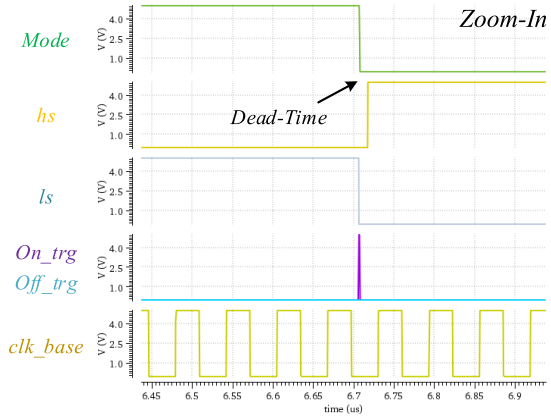
V. Post-Layout Validation and Experimental Results

To validate the operation of the new HR-VFVDM, it has been realized in TowerJazz 0.18-μm 5-V CMOS process as well as on Altera Cyclone V FPGA. The source codes, i.e., the HDL (Verilog) codes, for the FPGA and ASIC implementations are identical and were converted to hardware using Quartus environment and Cadence tools (dc and encounter), respectively. The DL comprises 128 DEs and the on-time commands, i.e., $hs_{on}[n]$ and $ls_{on}[n]$, are 13-bit long.

Shown in Figs. 13–16 are post-layout results of the integrated realization during steady-state and transient scenarios carried out in the Virtuoso environment with Cadence ADE simulation tools to account for both routing delays and parasitics. Steady-state operation is demonstrated in Fig. 13 for hs_{on} = 13'd2280 and ls_{on} = 13'd1720. The switching frequency and the duty cycle remain constant and equal 1.25 MHz and 57%, respectively. As can be seen, the *mode* signal changes periodically indicating the operating time intervals of each hardware module ($Mode_0$ or $Mode_1$ in Fig. 11). The SR-FF input signals, *on_trg* and *off_trg*, are shown to exemplify the relationships between the counter–comparator



(a)



(b)

Fig. 13. (a) Post-layout results of steady-state operation with f_{sw} = 1.25 MHz and D = 0.57. (b) Zoom-in view.

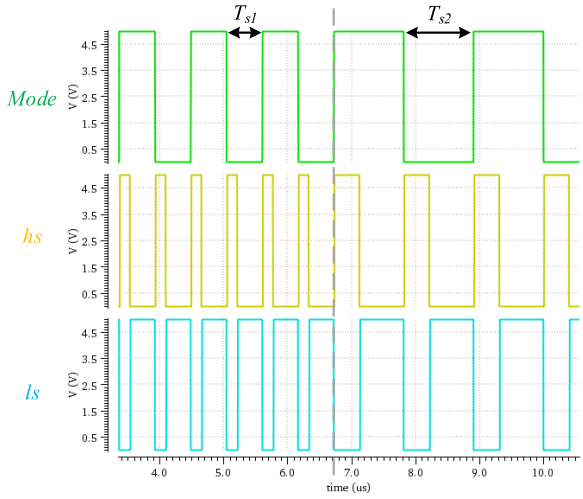


Fig. 14. Post-layout results for a stepwise change in both switching cycle segments. f_{sw1} = 880 kHz, f_{sw2} = 457 kHz, D_1 = 0.17, and D_2 = 0.29.

modules and the generated PWM signals. The HR attributes of the generated PWM signals are demonstrated in the zoomed-in view of Fig. 13(b) where the *on_trg* signal rises to logic high asynchronously to the ring-oscillator reference signal, *clk_base*.

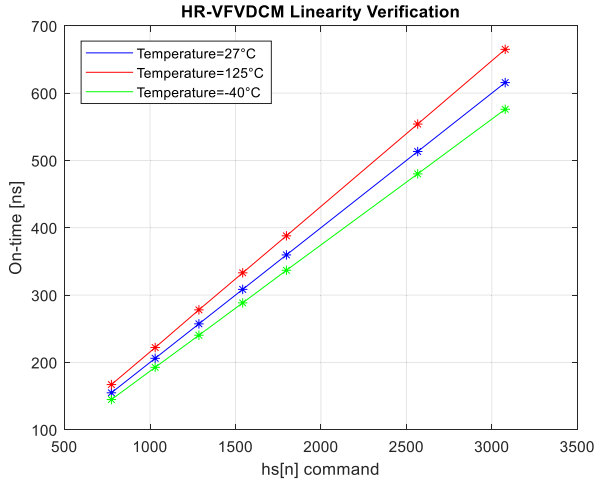


Fig. 15. Linearity verification of the HR-VFVDM for three temperature corners.

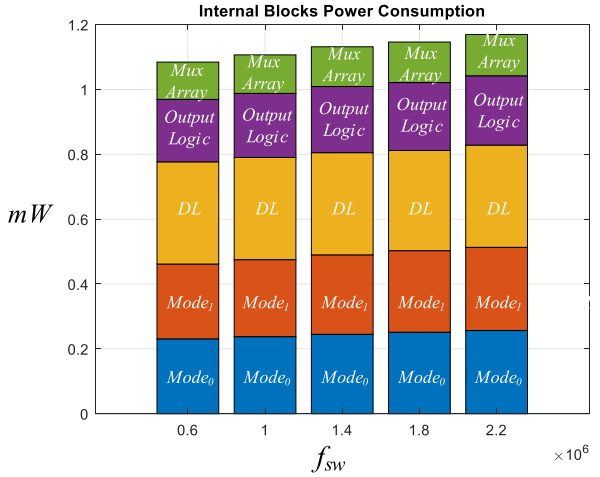


Fig. 16. Internal submodules' power dissipation for multiple switching conditions.

Fig. 14 demonstrates the modulator's response to an abrupt change in both duty-cycle and switching frequency attributes. Prior to the transition event, the switching frequency is 880 kHz, and the on-time commands of $hs_{on}[n]$ and $ls_{on}[n]$ are 13'd959 and 13'd4721, respectively. The modified values of $hs_{on}[n]$ and $ls_{on}[n]$ are 13'd3193 and 13'd7746, respectively, resulting in the new switching frequency of 457 kHz. As can be seen, the new steady-state is achieved within a single switching cycle thus validating its compatibility in advanced hybrid PFM-PWM controllers for resonant converters [11], [12].

Fig. 15 shows the *hs* pulsewidth as a function of its 13-bit on-time command for different temperature corners while the *ls* pulsewidth remains constant. As can be seen, monotonicity and linearity attributes are attained. The time resolution of the integrated realization is extracted from the post-layout simulations by calculating the slope of the pulsewidth dependency on its respective drive command, as shown in Fig. 15. For nominal operating conditions, the time resolution equals approximately 200 ps regardless of the operating point. This can also be attained from the time-domain simulations as in Fig. 14 by calculating the local derivative with respect to a given

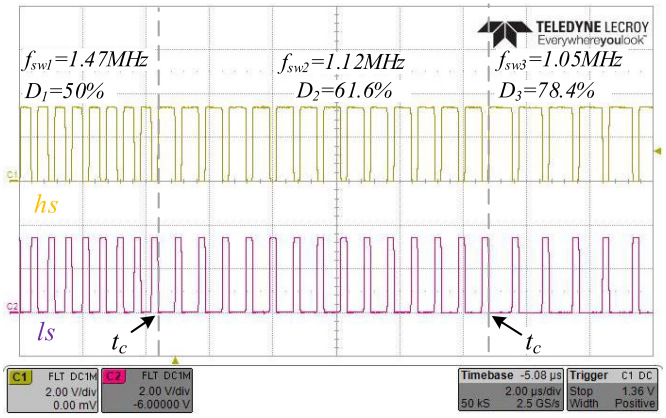


Fig. 17. Experimental results of a change in both frequency and duty-cycle attributes. $f_{sw1} = 1.47$ MHz, $f_{sw2} = 1.12$ MHz, $f_{sw3} = 1.05$ MHz, $D_1 = 0.5$, $D_2 = 0.616$, and $D_3 = 0.784$.

change in on-time commands. This property can be further enhanced if a more advanced fabrication process is used (such as a deeper submicrometer process) with no modification to the HDL code. Moreover, while the temperature has an impact on the time-resolution attribute of the module it does not affect its linearity or monotonicity characteristics. When integrated into a digital controller, the best- and worst-case time-resolution attributes are taken into consideration when designing the control coefficients in the form of small-signal PWM modulator gain to ensure accurate regulation capabilities across the entire temperature range.

Power dissipation of the internal digital blocks has been extracted for a wide range of switching conditions (600 kHz–2.2 MHz), as shown in Fig. 16. As can be seen, the total power consumption remains below 1.2 mW for the entire validated range. The dissipated power slightly increases as a function of the switching frequency due to the increased number of internal mode transitions, counter-reset operations, and control signal modifications.

Shown in Fig. 17 are experimental waveforms of the FPGA-based realization operating in the MHz range (1.47, 1.12, and 1.05 MHz) with arbitrary duty-cycle commands (50%, 61.6%, and 78.4%). In this scenario, the on-time of the low-side PWM signal, *ls*, remains constant while the duration of the high-side signal, *hs*, is extended in a stepwise manner at time locations marked as t_c in Fig. 17. As can be seen, correct operation and single-cycle convergence are obtained for concurrent changes of both switching attributes, i.e., f_{sw} and D, regardless of the relatively complicated routing of asynchronous designs in programmable platforms which confirms the design guidelines discussed in Section IV. Moreover, the frequency-hopping operation demonstrated in Figs. 14 and 17 also validates the potential incorporation of the HR-VFVDM in frequency-hopped PWM controllers and in spread spectrum clocking schemes [41].

The time resolution of the FPGA-based realization is calculated by increasing the on-time command by a predefined number of DEs and measuring the resultant change in the pulsewidth. This is shown in Fig. 18, for two consecutive 100 DEs change of the on-time command. As can be seen,

Fig. 18. Experimental time-resolution measurement for two consecutive 100 DEs increase in the $hs[n]$ command.

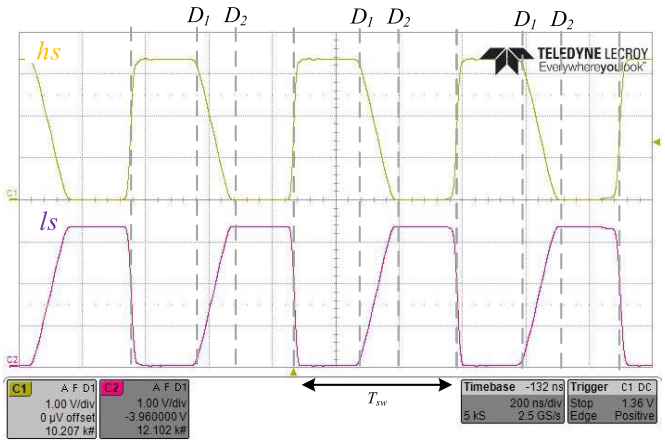
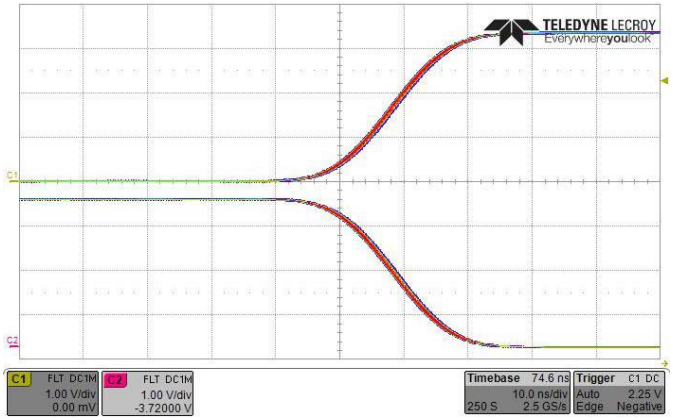
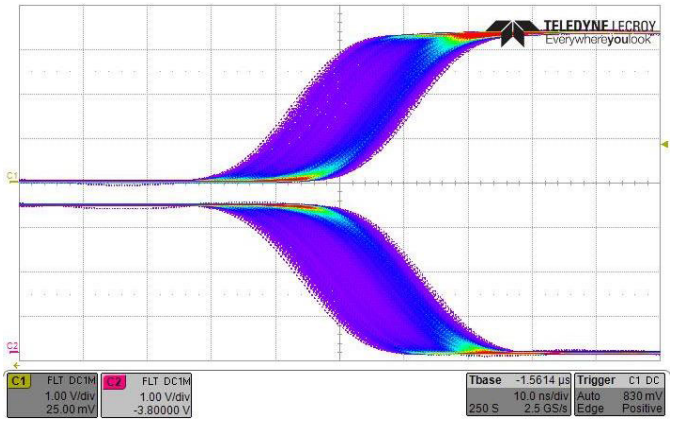


Fig. 19. Monotonicity and linearity verification for $f_{sw} = 1.95$ MHz, $D_1 = 0.4$, and $D_2 = 0.6$.



(a)



(b)

Fig. 20. Persistence measurements of two FPGA realizations. (a) Asynchronous-oriented implementation. (b) Conventional implementation.

the pulsewidth is increased by 22 ns for each alteration, and a time resolution of 220 ps is derived. The DE propagation time, t_{de}, is the main contributor to the overall time resolution of the modulator. However, interconnect delays have an effect as well which is inherently considered in the aforementioned resolution calculations.

Fig. 19 demonstrates the monotonicity and linearity experimental verification of the FPGA prototype. Ideally, for the smallest change in the duty-cycle command (i.e., 1 LSB) the generated PWM signal's on-time will increase or decrease by the delay of a buffer-cell (t_{de}). In this study, this is verified by increasing the on-time command of *hs* by one every ten switching cycles in a cyclic manner and averaging over time. To maintain constant switching frequency, the on-time command of *ls* undergoes the same procedure but with reversed polarity. Theoretically, a right-triangular waveform with a constant slope correlated with the average propagation delay of a single DE is expected for the *hs* signal and a left-triangular waveform for the *ls* signal. Here, the switching frequency is maintained at 1.95 MHz and the duty cycle varies from 40% to 60%. As can be seen in the experimental results of Fig. 19, a constant slope is obtained for both *hs* and *ls* signals forming the aforementioned triangular waveforms in the region of interest.

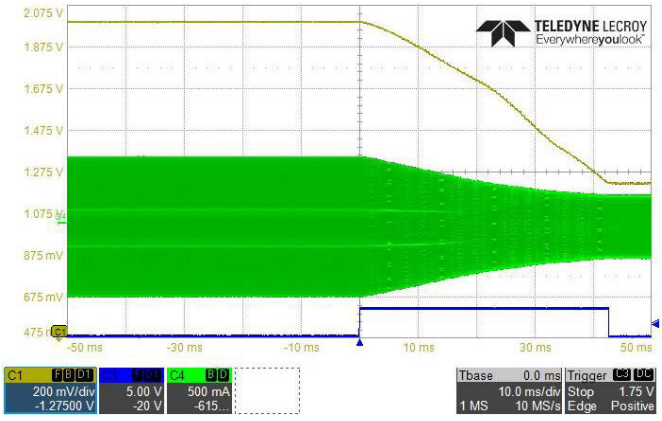
Fig. 20 demonstrates persistence measurements of two FPGA realizations at the rising- and falling edges of the *hs* and *ls* signals, respectively. The first follows the design guidelines of Section IV with predefined implementation regions for each submodule according to the signal flow and special emphasis on symmetry between $Mode_0$ and $Mode_1$ hardware. As can be seen, consistent operation is obtained thus validating the HR attributes of the design. On the other hand, the second realization which follows conventional place and route routines results in significant jitter which lowers the time resolution of the module.

Figs. 21 and 22 demonstrate the incorporation of the HR-VFVDM in a resonant-based SMPS. Here, a high-frequency HB-LLC resonant converter for low-power applications is realized with an input voltage range of 3–7 V. The nominal values of the resonant capacitance, *Cr*, resonant inductance, *Lr*, and leakage inductance, *Lm*, are 0.68 μF, 37 nH, and 2 μH, respectively. Therefore, the resultant nominal resonance frequency of the LLC tank is 1 MHz, according to (13).

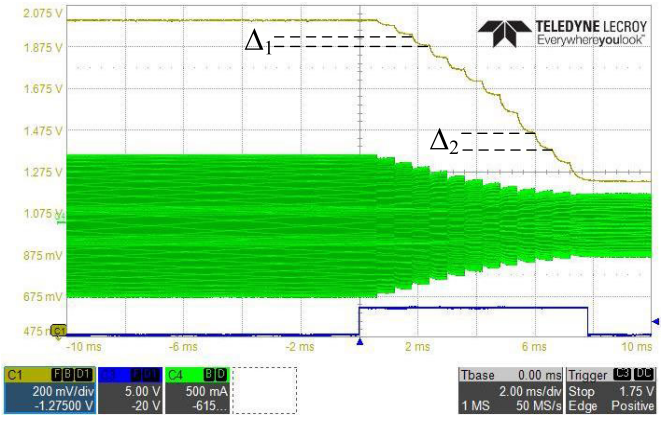
The extended gain regions attribute for the HB-LLC resonant converter is demonstrated in Fig. 21. Here, a frequency sweep from 830 kHz to 1.35 MHz is carried out with an HR-VFVDM [Fig. 21(a)] and a conventional DPWM

TABLE I
COMPARISON WITH PRIOR DPWM ARCHITECTURES

Ref.	Year	Platform	Switching frequency	Time resolution	Bits	Input clock frequency	Frequency modulation	Duty-cycle modulation
[20]	2021	Xilinx Artix-7 FPGA	<1MHz	1.25ns	10	20-25MHz	NA	Yes
[44]	2020	Kintex 7	<1MHz	50ps	15	250MHz	NA	Yes
[43]	2018	Xilinx Artix-7 FPGA	<1MHz	625ps	11	200MHz	NA	Yes
[45]	2008	0.6µm BiCD	<1MHz	1.22ns	10	25MHz	NA	Yes
This paper	2023	0.18µm 5V CMOS and Cyclone V FPGA	<2.5MHz	200/220ps	13	None	Yes	Yes



(a)



(b)

Fig. 21. Comparison of achievable voltage conversion ratios for a high-frequency HB-LLC resonant converter driven by (a) HR-VFVDM and (b) conventional DPWM.

modulator [Fig. 21(b)] with an input voltage of 4 V and a resistive load of 7.2 Ω. As can be seen the output voltage and the resonant current at the primary side are identical for the initial and final frequencies, i.e., 830 kHz and 1.35 MHz, which validates the capabilities of both modulators to produce gating signals in the tested range. Here, the drive command is slowly increased by 1 LSB at a time to allow the settling of the output voltage with respect to the new switching conditions. As can be seen, a smooth and continuous output voltage is obtained in Fig. 21(a) due to the single DE resolution. However, for the conventional DPWM of Fig. 21(b), the output voltage exhibits a very narrow range of possible gain regions compared to Fig. 21(a), which agrees with the case study of Section III. Two exemplary output voltage transitions are marked, Δ_1 and Δ_2, which highlight the degradation of the frequency resolution as the switching frequency increases, i.e., $\Delta_2 > \Delta_1$.

Fig. 22 shows closed-loop operation at the MHz range of two HB-LLC resonant converter-based SMPS with an input voltage of 7 V, output voltage of 3.3 V, and a resistive load of 10 Ω. In Fig. 22(a) and (b), a conventional DPWM module is utilized by the digital controller to generate the gating signals for the power-stage transistors (see Fig. 10). As can be seen, the controller interchangeably modifies the switching frequency (1.11 and 1.16 MHz) which results in low dc error but with significant low-frequency output voltage ripple, driving the converter into the audio band. This is due to the reduced number of gain regions at high switching frequencies as discussed in Section III and demonstrated in Fig. 21. The zoomed-in view of Fig. 22(b) shows a transition from 1.11-MHz operation to 1.16 MHz along with the resonant current at the transformer's primary side, i_r. Shown in Fig. 22(c) and (d) are the resultant waveforms in case an HR-VFVDM is incorporated into the digital controller. As can be seen, the steady-state error remains zero while operating at a constant switching frequency, which significantly reduces output voltage ripple and resonant current aberrations. In agreement with the case study of Section III, the single DE resolution is the enabler for tight output voltage regulation without low-frequency voltage ripples, which simplifies filtering efforts and drives the converter away from the audio band. Here, the converter operates with an above 50% duty-cycle ratio, taking advantage of the HR variable duty-cycle attribute of the modulator by realizing the control law discussed in [12].

Table I provides a comparison with prior DPWM architectures. The compared architectures are synthesizable, i.e., can be described by HDL, and realized as an integrated module or on programmable platforms. As can be seen, most realizations require a high-frequency external clock which is correlated with the overall time resolution and power consumption. As shown, state-of-the-art modulators realized on modern FPGAs can achieve resolution as high as 50 ps for certain operating conditions. However, since the high-frequency input clock is commonly used to obtain the HR attributes, it does not increase the possible operating frequency or support on-the-fly HR adjustments of both the duty cycle and the switching frequency. Moreover, most FPGA-based DPWM units exploit modern FPGA resources such as DCMs, which makes the transition to dedicated ASIC complex and expensive.

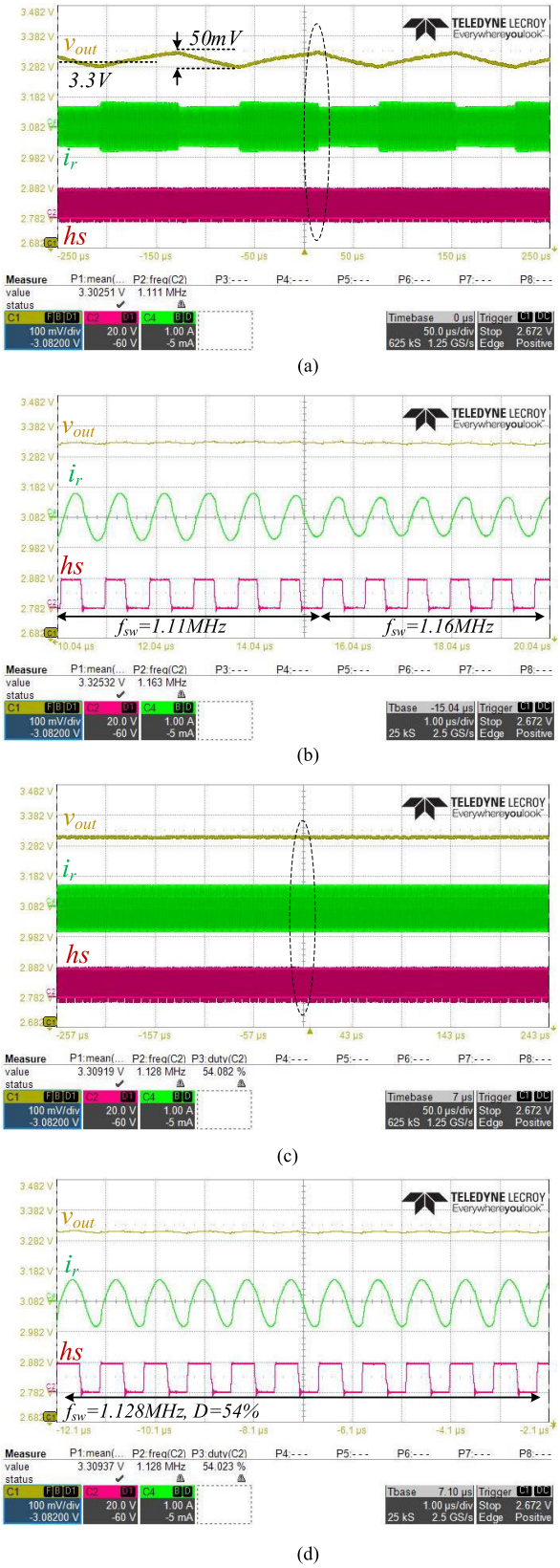


Fig. 22. Closed-loop operation in the MHz range of a HB-LLC resonant converter with input voltage of 7 V and regulated output of 3.3 V with conventional DPWM module (a-b) and an HR-VFVDM (c-d).

VI. Conclusion

A new architecture for an all-digital variable-frequency variable-duty-cycle modulator has been presented and verified through post-layout simulations and experimental data. The modulator generates gating signals with the adjustable switching frequency, duty-cycle, and dead-time attributes with the time resolution of a single DE while ensuring single-cycle convergence. This is achieved by incorporating a DL-multiplexer module and utilizing its propagating signals to implement an algorithm that allows independent on-time commands for each segment of the switching cycle. The solution is compact, scalable, and based on stand cells alone without any custom-designed modules or high-frequency clock resources, thus making it an attractive candidate for integration in low-power modern digital controller ICs.

The HR-VFVDM has been designed in a digital-oriented approach and implemented on a 0.18-μm 5-V CMOS process resulting in a total silicon area of 0.18 mm^2 as well as on a programmable logic fabric to showcase the adaptability of the architecture. Post-layout simulations of steady-state and transient scenarios are provided, demonstrating highly linear characteristics with 200-ps time resolution at nominal operating conditions and single-cycle convergence. Experimental results of the FPGA prototype show a time resolution of 220 ps and validate the design guidelines for asynchronous realizations of DL-based structures on programmable platforms.

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