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Frequency-Variant Electronic Capacitor to Simultaneously Reduce Low-Frequency DC Link Voltage Ripple and Improve Current THD of Grid-Connected Power Converters

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***Abstract*—Electronic Capacitor (EC) is a circuit typically aimed to replace (in part or entirely) the bulk DC-link capacitor of a grid-interfacing power converter in plug-and-play manner. EC is realized by a bidirectional DC-DC converter terminated with small auxiliary capacitor. The converter is controlled such that its DC-link side terminals mimic the behavior of a capacitor with much higher constant capacitance. In this paper, a modification of the classical EC control structure is proposed, imposing the DC-link side terminals to emulate a frequency-variant capacitor rather than a constant one. The proposed algorithm allows achieving simultaneous reduction of both DC link voltage ripple and grid-side current total harmonic distortion (THD) compared to ones attained by classical solutions, thus improving the trade-off between DC link voltage dynamics and AC-side current quality inevitably present in any grid-connected power converter. The proposed methodology is well-supported by experiments.**

***Index Terms*— Grid-connected converters, DC link, Electronic Capacitor, THD, Dynamic response.**

I. Introduction

MODERN grid codes impose tight power quality standards on the operation of grid-connected converters [1], [2]. In order to comply with these requirements, grid-connected inverters and power factor correction rectifiers (PFCR) are typically forced to exchange sinusoidal-shaped currents with the mains [3] – [5]. Such operation implies pulsating instantaneous power to be exchanged between mains and grid-interfacing converter DC link, imposing DC link voltage ripple across the bulk DC link capacitor terminals [6].

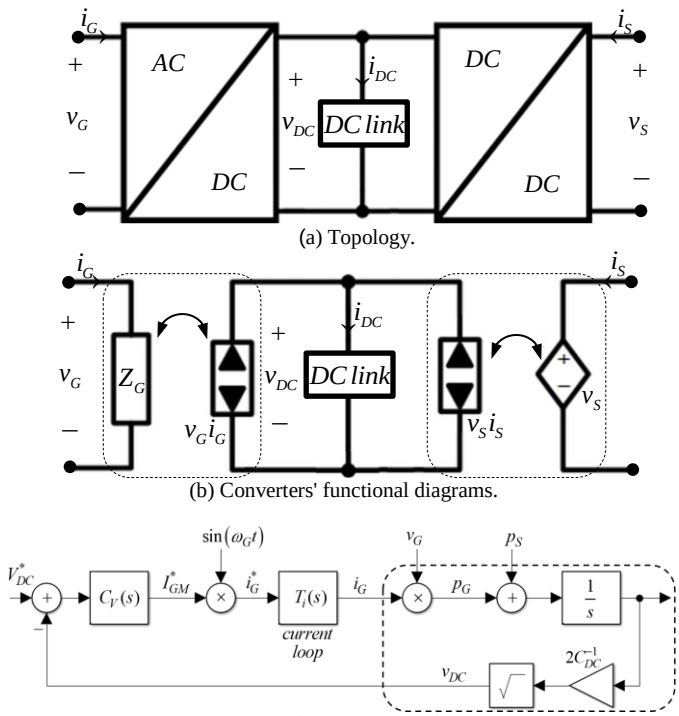
Grid-connected converters are typically regulated utilizing dual-loop (employing DC link voltage and grid-side current as outer and inner loop variables, respectively) control structure, with the outer loop usually utilizing either PI of type-II regulator [7] – [9]. While the current loop bandwidth is high (limited by switching and sampling frequencies only), the voltage loop bandwidth is relatively low (typically 5 – 10Hz) due to the trade-off between DC link voltage dynamics and the maximum allowed grid-current THD [10]. Due to the slow voltage loop response, significant amount of DC link capacitance should be utilized in order to keep the DC link voltage within tolerable limits upon load transients. Unfortunately, DC link capacitors are considered as power conversion system bottleneck in terms of reliability and/or physical size [11] – [13]. Therefore, amount of DC link capacitance should be minimized. One of the most popular approaches to DC link capacitance reduction is its full or partial replacement by active power decoupling circuits, which transfer pulsating power component into a much smaller capacitance via a bidirectional DC-DC converter thus decoupling the resulting large voltage swing from the DC link terminals to auxiliary terminals [14] – [23]. As indicated in [24], such a replacement may attain physical size and cost reduction in addition to reliability enhancement. Moreover, if local measurements only are required for active power decoupling circuit functioning in addition to the ability to mimic the dynamic behavior of a certain-valued capacitance, it may be connected across the DC link of a grid-connected converter in a plug-and-play manner. Such a circuit was proposed in [25] and is referred to as "Electronic Capacitor" thereafter. EC realization was discussed in [26] and elaborated in [27]. Dynamic limitations of EC performance due to reduced hold-up ability were revealed in [28] and enhanced in [29]. The possibility of partial DC link capacitor replacement by a reduced-rating EC was recently revealed in [30]. Unfortunately, the trade-off between DC link voltage dynamics and the maximum allowed grid-current THD is present irrespectively to employing either passive or active DC link capacitor due to the fact that the DC link characteristics "seen" by the grid-connected converter is the same in both cases.

It was recently shown in [31] that the double-mains-frequency DC link voltage ripple component (which is inversely proportional to the value of bulk DC link capacitor) is the reason for the above-mentioned trade-off. Consequently, reducing the magnitude of voltage ripple component fed back to the voltage loop by e.g. employing a notch filter in the grid-interfacing power converter voltage controller may yield improvement of either DC link voltage dynamics or grid-side current THD (or combination of both) [32]. However, the approach requires modification of grid-interfacing power converter control structure and does not lead to any DC link voltage ripple reduction since the amount of DC link capacitance remains unchanged. On the other hand, it was recently pointed out in [33] that since controllable capacitive impedance is actually emulated at DC-link side terminals of an EC, it is possible to impose either time-variant or frequency-variant behavior rather than mimicking a constant-valued capacitance. Consequently, the paper proposes to emulate a frequency-variant capacitance at EC DC-link side terminals so that original capacitance value is emulated within grid-

connected converter DC link voltage loop bandwidth and a much higher one is mimicked around double-mains-frequency, relevant for DC link voltage ripple component. As a result, while the DC link voltage dynamics remains unchanged, actual DC link voltage ripple component and hence grid-side current THD are significantly reduced. The proposed methodology is successfully applied to an off-the-shelf PFCR employing active EC-based DC link, demonstrating significant performance improvement without additional modification of an existing power stage.

II. Grid-connected power conversion system

Consider (without loss of generality) a widely-adopted dual-stage grid-connected AC/DC power conversion system depicted in Fig. 1, consisting of grid-interfacing AC/DC converter, DC link and downstream DC/DC converter. In general case, the power flow (both active and/or reactive) may be either from AC terminals to DC terminals or vice-versa.



(a) Topology.

(b) Converters' functional diagrams.

(c) Control structure for unity power factor operation.

Fig. 1. Typical dual-stage grid-connected power conversion system.

Steady-state grid-side voltage and current are described by

$$v_G(t) = V_{GM}\sin(\omega_G t) + \underbrace{\sum_{n>1} V_n \sin(n\omega_G t)}_{\Phi_v(t)}[\mathrm{V}]$$
$$i_G(t) = I_{GM}\sin(\omega_G t + \varphi_1) + \underbrace{\sum_{n>1} I_n \sin(n\omega_G t + \varphi_n)}_{\Phi_i(t)}[\mathrm{A}], \quad (1)$$

with ω_G [rad/s] signifying mains frequency, V_{GM} and I_{GM} denoting the first harmonic voltage and current magnitudes, respectively, V_n and I_n symbolize n^{th} harmonic voltage and current magnitudes, respectively, φ_n represents the phase shift between n^{th} harmonic of voltage and current, and Φ_v, Φ_i designate residual harmonic content, inevitable present in practical systems so that

$$\sqrt{\sum_{n>1} V_n^2} << V_{GM}^2, \quad \sqrt{\sum_{n>1} I_n^2} << I_{GM}^2. \quad (2)$$

In case $\varphi_1 = 0$ or $\varphi_1 = \pi$, grid-connected converter is said to operate with unity power factor. Taking into account (2), the contribution of residual harmonic content to instantaneous grid-side power may be neglected [32]. The latter is then given by

$$p_G(t) = v_G(t)i_G(t) \approx \underbrace{0.5V_{GM}I_{GM}\cos\varphi_1}_{P_G} - \underbrace{0.5V_{GM}I_{GM}\cos(2\omega_G t + \varphi_1)}_{\Delta p_G(t)}[\mathrm{W}] \quad (3)$$

where P_G denotes average power component, while $\Delta p_G(t)$ represents low-frequency pulsating (zero average) power constituent. On the other hand, steady-state DC-terminals-side voltage and current are constant, given by

$$v_S(t) = V_S[\mathrm{V}],\ i_S(t) = I_S[\mathrm{A}]. \quad (4)$$

Corresponding instantaneous power is then

$$p_S(t) = v_S(t)i_S(t) = V_S I_S[\mathrm{W}]. \quad (5)$$

Consequently, instantaneous DC-link power is given by

$$p_{DC}(t) = v_{DC}(t)i_{DC}(t) = p_G(t)\eta_G + p_S(t)\eta_S^{-1} = P_G\eta_G + P_S\eta_S^{-1} - \Delta p_G(t)\eta_G, \quad (6)$$

where η_G and η_S symbolize grid-connected and downstream converters' efficiencies, respectively. In steady-state, active power balance

$$P_G\eta_G + P_S\eta_S^{-1} = 0 \Rightarrow I_{GM} = \frac{-2P_S\eta_S^{-1}\eta_G^{-1}}{V_{GM}\cos\varphi_1} \quad (7)$$

is assured by grid-connected converter controller by regulating the average value of DC link voltage v_{DC} to a constant reference V_{DC}^*. Consequently, DC link must exchange pulsating power

$$p_{DC}(t) = -\Delta p_G(t)\eta_G = P_S\eta_S^{-1}\cos(2\omega_G t + \varphi_1) \quad (8)$$

with the grid. In classical systems, DC link is realized by a capacitance C_{DC}. Hence, steady-state DC link voltage is approximately given by [22]

$$v_{DC}(t) = \sqrt{\frac{2}{C_{DC}}\int_0^t p_{DC}(\tau)d\tau} \approx V_{DC}^* - \underbrace{\frac{\Delta V_{DC}\sin(2\omega_G t + \varphi_1)}{\Delta v_{DC}(t)}}_{\Delta v_{DC}(t)} = V_{DC}^* - \Delta v_{DC}(t), \quad (9)$$

where $\Delta v_{DC}(t)$ denotes the double-mains-frequency DC link voltage ripple component with

$$\Delta V_{DC} = \frac{P_S\eta_S^{-1}}{2\omega_G V_{DC}^* C_{DC}} << V_{DC}^*. \quad (10)$$

In order to satisfy (10), DC link capacitance of 500 – 1000 μF per 1 kVA rating is typically employed [34].

For the sake of brevity, consider a unity power factor operating grid-connected converter with $\varphi_1 = 0$ or $\varphi_1 = \pi$. In order to satisfy (7), dual-loop control structure shown in Fig. 1(c) is typically employed with outer (voltage) loop regulating the DC link voltage to a set point value V_{DC}^* using a type-II

$$C_V(s) = K\frac{\tau s + 1}{s(\sigma s + 1)} \quad (11)$$

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or PI ((11) with σ = 0) controller as voltage loop compensator, which computes the desired grid-side current magnitude I_{GM}^*.The latter is multiplied by unity-grid-voltage template $\sin(\omega_G t)$ to create the grid-side current reference i_G^*, tracked by the inner (current) loop [31]. Since voltage loop is of interest in this work, current loop is represented by complementary sensitivity function $T_i(s)$. Moreover, current loop bandwidth is significantly higher in practice than the double-grid frequency, i.e.

$$T_i(s) \approx 1 \Rightarrow i_G(t) \approx i_G^*(t) \tag{12}$$

may be accurately assumed up to $2\omega_G$ [32]. Combining (7) and (9) – (11) with (13) yields (cf. Fig. 1(c))

$$i_{GM}^*(t) \approx I_{GM} + \Delta V_{DC} \left|C_V(2\omega_G)\right| \sin\left(2\omega_G t + \arg C_V(2\omega_G)\right). \tag{13}$$

Steady-state grid-side current is then obtained as (cf. (12))

$$\begin{aligned} i_G(t) &= i_{GM}^*(t)\sin(\omega_G t) \\ &\approx I_{GM}\sin(\omega_G t) + \Delta V_{DC}\frac{\left|C_V(2\omega_G)\right|}{2}\left(\cos(3\omega_G t) - \cos(\omega_G t)\right) \\ &\approx \underbrace{I_{GM}\sin(\omega_G t) - \Delta V_{DC}\frac{\left|C_V(2\omega_G)\right|}{2}\cos(\omega_G t)}_{i_{G1}(t)} \\ &\quad + \underbrace{\Delta V_{DC}\frac{\left|C_V(2\omega_G)\right|}{2}\sin(3\omega_G t)}_{i_{G3}(t)}. \end{aligned} \tag{14}$$

Hence, grid-side current THD is obtained as

$$THD_i = \frac{rms\left(i_{G3}(t)\right)}{rms\left(i_{G1}(t)\right)} \tag{15}$$

with $rms(x(t))$ denoting the root-mean-square (RMS) value of $x(t)$. Taking into account the fact that $|C_V(2\omega_G)| << 1$ [35] while using (10) with (7), there is

$$\Delta V_{DC}\frac{\left|C_V(2\omega_G)\right|}{2} << I_{GM} \tag{16}$$

and (15) may be approximated as

$$THD_i \approx \Delta V_{DC}\frac{\left|C_V(2\omega_G)\right|}{2I_{GM}}. \tag{17}$$

It may be concluded that grid-side current THD is proportional to the magnitude of double-grid-frequency DC link voltage ripple and to the voltage controller gain at $2\omega_G$. According to (10), ΔV_{DC} is proportional to $1/C_{DC}$. On the other hand, it was shown in [28] that the proportional gain of the controller (11) K (and hence $|C_V(2\omega_G)|$) is tuned so that it is proportional to C_{DC}, i.e.

$$\begin{aligned} \Delta V_{DC} &= \frac{1}{C_{DC}}\frac{P_S}{2\omega_G V_{DC}^*}, \\ C_V(s) &= C_{DC}\underbrace{K'\frac{\tau s+1}{s(\sigma s+1)}}_{C_V'(s)} = C_{DC}C_V'(s), \end{aligned} \tag{18}$$

where $K = C_{DC}K'$ with K' and τ independent of C_{DC}. Combining (7) with $\varphi_1 = 0$, (10), (17) and (18) yields

$$THD_i \approx \frac{1}{C_{DC}}\frac{V_{GM}}{8\omega_G V_{DC}^*}\left|C_V(2\omega_G)\right| = \frac{V_{GM}}{8\omega_G V_{DC}^*}\left|C_V'(2\omega_G)\right|. \tag{19}$$

Consequently, grid-side current THD is independent of DC link capacitance value. Moreover, small-signal representation of the voltage loop plant in Fig. 1(c) is given by [31],[32]

$$P_V(s) = \frac{V_{GM}}{2V_{DC}^* C_{DC}}\frac{1}{s}, \tag{20}$$

hence the voltage loop gain

$$L_V(s) = C_V(s)P_V(s) = \frac{V_{GM}}{2V_{DC}^*}\frac{C_V'(s)}{s} \tag{21}$$

and corresponding crossover frequency [31]

$$\omega_{CV1} << 2\omega_G \tag{22}$$

are DC link capacitance value independent as well. In case the controller gain K is tuned to certain DC link capacitance C_{DC} (cf. (18)) but actual capacitance connected across DC link terminals is αC_{DC}, (19) and (21) become

$$THD_i \approx \frac{1}{\alpha C_{DC}}\frac{V_{GM}}{8\omega_G V_{DC}^*}\left|C_V(2\omega_G)\right| = \frac{1}{\alpha}\frac{V_{GM}}{8\omega_G V_{DC}^*}\left|C_V'(2\omega_G)\right| \tag{23}$$

and

$$L_V(s) = \frac{1}{\alpha}\frac{V_{GM}}{2V_{DC}^*}\frac{C_V'(s)}{s}, \tag{24}$$

respectively. For $\alpha > 1$, grid-side current THD decreases (compared to (19)), yielding steady-state performance improvement. Voltage loop gain crossover frequency now given by

$$\omega_{CV2} = \frac{1}{\alpha}\omega_{CV1} \tag{25}$$

reduces compared to (22), yielding dynamic performance deterioration. For $\alpha < 1$, grid-side current THD rises, yielding steady-state performance deterioration, while voltage loop gain crossover frequency increases, yielding steady-state performance improvement. This summarizes the trade-off between DC link voltage dynamics and grid-current THD.

III. Frequency-Variant Capacitor Concept

Note that the proportional gain of PI controller K should be tuned to C_{DC} up to ω_{CV} only. On the other hand, important matter should be pointed out according to (17): grid-side current THD is affected by the DC link voltage ripple existing solely at $2\omega_G$, i.e. (cf. (10))

$$\Delta V_{DC} = \begin{cases} \dfrac{P_S\eta_S^{-1}}{2\omega_G V_{DC}^* C_{DC}}, & \omega = 2\omega_G \\ 0, & elsewhere \end{cases}, \tag{26}$$

and voltage controller gain at corresponding frequency only. Since voltage loop bandwidth is much lower than $2\omega_G$ (cf. (25)), voltage loop gain and grid-side current THD requirements are actually frequency-decoupled. Defining a so-called "frequency-variant capacitance" as

$$C_{DC}^{FS} = \begin{cases} \alpha C_{DC}, & 2\omega_G - \Delta\omega < \omega < 2\omega_G + \Delta\omega \\ C_{DC}, & elsewhere \end{cases} \tag{27}$$

with $\Delta\omega << 2\omega_G$ (cf. Fig. 2) and applying it as the DC link capacitance instead of a constant-valued one yields (cf. (10))

$$\Delta V_{DC} = \frac{1}{\alpha}\frac{P_S\eta_S^{-1}}{2\omega_G V_{DC}^* C_{DC}}, \tag{28}$$

i.e. grid-side current THD expression (23) holds. On the other hand, (20) remains unchanged and thus (21), (22) hold as well.

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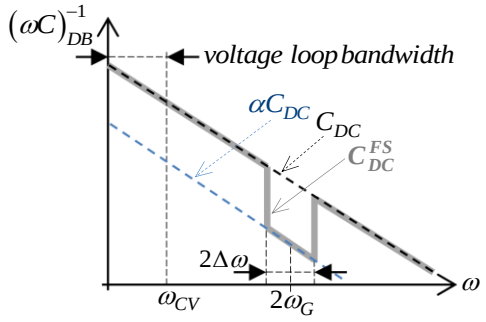


Fig. 2. Frequency-variant capacitance impedance vs frequency.

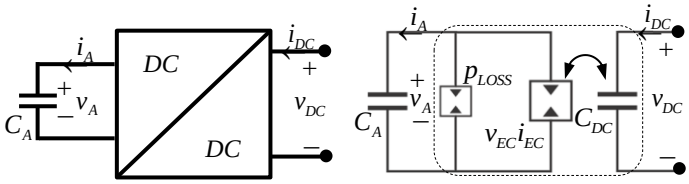
Consequently, selecting $\alpha > 1$ yields simultaneous reduction of both ΔV_{DC} and THD_i without affecting the bandwidth of voltage loop (i.e. dynamic performance is not sacrificed when steady-state performance is improved). Furthermore, it follows from (23) and (28) that selecting $\alpha >> 1$ leads to low-frequency DC link voltage ripple elimination and near-zero grid-side current THD. However, due to finite word length, residual harmonic/switching frequency content and grid-frequency deviation from its nominal value, zero ΔV_{DC} and THD_i are theoretical lower bounds which cannot be achieved in practice.

Frequency-variant DC link capacitance is suggested to be realized using EC technology, as shown in the subsequent Section.

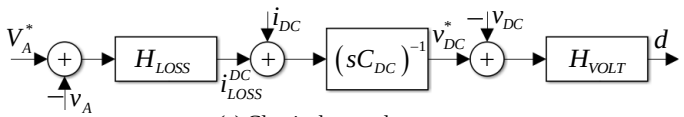
IV. Frequency-Variant Capacitor Realization

A. Classical EC essentials

EC technology may be adopted to reduce the value of actual physical DC link capacitance, yet preserving the performance of DC link voltage loop by keeping the capacitance value "seen" from the DC link terminals of grid-connected converter unaltered (i.e. C_{DC}). EC consists of a bidirectional DC-DC converter terminated by a low-valued auxiliary capacitor C_A << C_{DC} (cf. Fig. 3(a)). Classical EC control structure imposes the DC link side impedance of the DC-DC converter to follow that of C_{DC} within relevant DC link control bandwidth (typically 5 – 10Hz), as shown in Fig. 3(b) with p_{LOSS} denoting DC-DC conversion losses, reflected to auxiliary capacitor side.



(a) Topology. (b) Converter functional diagram.



(c) Classical control structure.

Fig. 3. Electronic capacitor technology.

The control circuitry is shown in Fig. 3(c), consisting of three main subsystems: losses compensation controller H_{LOSS}, aimed to compensate conversion losses by regulating the average value of the voltage v_A across auxiliary capacitor to a set point value V_A^*; *capacitance emulation*, mimicking the voltage-current relationship of the bulk capacitor C_A across DC-link side terminals of the DC-DC converter; and *voltage controller* H_{VOLT}, forcing the DC link side voltage to follow the reference v_{DC}^* by supplying appropriate duty cycle d to the modulator. An interested reader may refer to [26] for additional details.

As shown in [27] – [29], the EC is capable of replacing a bulk capacitance C_{DC} in a plug-and-play manner without altering the grid-connected converter performance, discussed in the previous Section. The technology is therefore adopted to realize a frequency-variant capacitance (27), as shown next.

B. Frequency-variant capacitance realization

Observing Fig. 2, it may be concluded that a frequency-selective capacitor may be realized by series connection of C_{DC} and a notch filter centered around $2\cdot\omega_G$, possessing gain of $1/\alpha$ and bandwidth of $2\cdot\Delta\omega$ [33]. Obviously, implementation using passive elements would probably be non-feasible due to required components' physical size. On the other hand, EC forms its DC-link side terminals impedance by the controller capacitance emulation subsystem (implemented in software of by low-power analog components), as explained in the previous subsection. Therefore, it would only be required to add the above-mentioned notch filter to the capacitance emulation subsystem without modifying either the power stage or the rest of controller subsystems. Transfer function of a notch filter satisfying the above-mentioned characteristics is given by

$$F(s)=\frac{s^2+\frac{2\Delta\omega}{\alpha}s+\left(2\omega_G\right)^2}{s^2+2\Delta\omega s+\left(2\omega_G\right)^2}. \tag{29}$$

The modified control structure is shown in Fig. 4. Bode diagram of capacitance emulation subsystem (and hence of the DC-link side impedance of the DC-DC converter in Fig. 3(a)) given by

$$Z_{DC}(s)=\frac{v_{DC}(s)}{i_{DC}(s)}=\frac{1}{sC_{DC}}F(s) \tag{30}$$

is depicted in Fig. 5 for C_{DC} = 270μF, $\omega_G = 2\pi\cdot 50$ rad/s , α = 10 and $\Delta\omega = 20\pi$ rad/s. It is well evident that $Z_{DC}(s)$ matches the impedance of 2700μF capacitance at $2\omega_G$ and of 270μF otherwise.

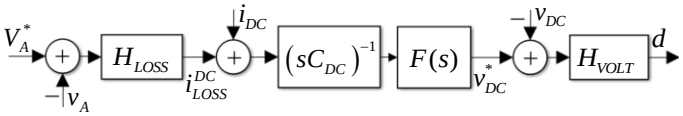


Fig. 4. Controller of frequency-variant electronic capacitor (27).

In case maximum reduction of ΔV_{DC} and THD_i is desired,

$$\alpha \to \infty \tag{31}$$

should be selected. Hence, (29) reduces to

$$F(s)=\frac{s^2+\left(2\omega_G\right)^2}{s^2+2\Delta\omega s+\left(2\omega_G\right)^2} \tag{32}$$

and an infinite capacitor effect [36], [37] is achieved at $\omega = 2\omega_G$. It is important to emphasize that EC voltage loop bandwidth (cf. Fig. 4) should be significantly higher than $2\omega_G$ so that the influence of $F(s)$ would be negligible at corresponding crossover frequency.

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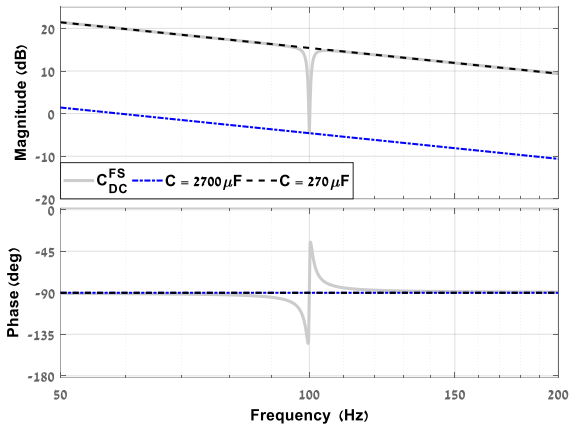

Fig. 5. Bode diagrams of (30) for C_{DC} = 270μF, $\omega_G = 2\pi\cdot 50$ rad/s, α = 10 and $\Delta\omega = 20\pi$ rad/s.

C. Grid-connected converter voltage loop stability assessment

Transfer function of the voltage loop plant in Fig. 1(c) and (20) may be reformulated as

$$P_V(s) = \frac{V_{GM}}{2V_{DC}^*}\cdot\frac{1}{C_{DC}s} = \frac{V_{GM}}{2V_{DC}^*}\cdot\frac{v_{DC}(s)}{i_{DC}(s)} = \frac{V_{GM}}{2V_{DC}^*}Z_{DC}(s), \quad (33)$$

i.e. it is formed by a scaled version of DC link impedance. When the capacitor C_{DC} is replaced by the proposed frequency-variant capacitor, combining (30) with (32) yields

$$Z_{DC}(s) = \frac{v_{DC}(s)}{i_{DC}(s)} = \frac{1}{sC_{DC}}\frac{s^2+(2\omega_G)^2}{s^2+2\Delta\omega s+(2\omega_G)^2}, \quad (34)$$

i.e. (33) becomes

$$P_{V,F}(s) = \frac{V_{GM}}{2V_{DC}^*}Z_{DC}(s)$$
$$= \underbrace{\frac{V_{GM}}{2V_{DC}^*}\frac{1}{sC_{DC}}}_{P_V(s)}\underbrace{\frac{s^2+(2\omega_G)^2}{s^2+2\Delta\omega s+(2\omega_G)^2}}_{F(s)} = P_V(s)F(s). \quad (35)$$

Corresponding voltage loop gain (21) is then altered as

$$L_{V,F}(s) = C_V(s)P_{V,F}(s)$$
$$= \underbrace{\frac{V_{GM}}{2V_{DC}^*}\frac{C_V'(s)}{s}}_{L_V(s)}\underbrace{\frac{s^2+(2\omega_G)^2}{s^2+2\Delta\omega s+(2\omega_G)^2}}_{F(s)}, \quad (36)$$

which is equivalent to adding a notch filter to the PI controller, as proposed in [32]. However, the effect is attained here without actually altering the original DC link voltage controller of the grid-interfacing converter. As shown in [31], DC link voltage loop crossover frequency ω_{CV} of practical single-phase 50Hz-mains connected converters typically resides between $2\pi\cdot 5$rad/s – $2\pi\cdot 15$rad/s (i.e. $\omega_{CV} < \omega_G$) to attain grid-side current THD of 5% or below for minimal phase margin of 40°. Consequently, if the original loop gain $L_V(s)$ is stable, modified loop gain $L_{V,F}(s)$ would be stable as well in case the influence of $F(s)$ on gain and phase of $L_V(s)$ at $s = j\omega_{CV}$ is negligible. Since phase influence bandwidth of a resonant filter is much more significant than that of the gain [38], the following should hold

$$\left|\arg F(\omega_{CV})\right| = \tan^{-1}\frac{2\Delta\omega\cdot\omega_{CV}}{(2\omega_G)^2-\omega_{CV}^2} < \psi_{\max}, \quad (37)$$

where ψ_{max} is the maximum allowed phase margin reduction. Hence,

$$\Delta\omega < \tan(\psi_{\max})\frac{(2\omega_G)^2-\omega_{CV}^2}{2\omega_{CV}} \quad (38)$$

must be selected to retain stability.

D. Remarks

D1. Digital implementation issues

It was emphasized in [38] that finite word length and quantization effects, inevitably present upon digital implementation, typically cause notch filter center frequency shift, imposing corresponding gain increase. Moreover, grid frequency may typically possess up to 2% uncertainty range around the nominal value [39]. Consequently, notch filter bandwidth 2Δω should be increased to improve robustness to frequency variations. On the other hand, increasing the notch filter bandwidth widens the influence region of notch filter gain and phase beyond the frequency of interest and deteriorates stability, as stated in the preceding subsection.

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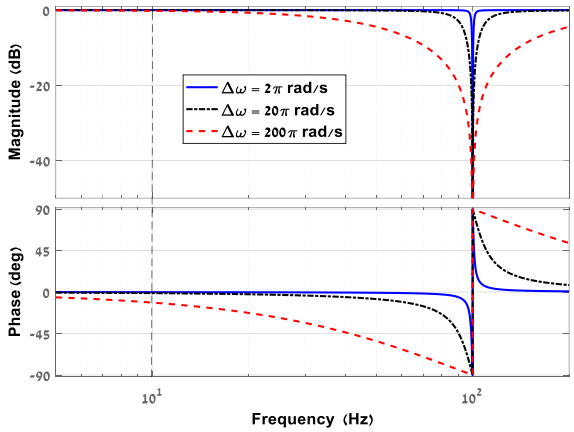

Fig. 6. Bode diagrams of (26) for $\omega_G = 2\pi\cdot 50$ rad/s and different Δω.

In order to prevent the notch filter from affecting DC link voltage loop performance, its gain and phase must be as close as possible to unity and zero, respectively, at the crossover frequency of the latter (cf. (38)). Fig. 6 depicts the Bode diagram of (26) for three different values of Δω and $\omega_G = 2\pi\cdot 50$ rad/s. It is well-evident that the filter with $\Delta\omega = 200\pi$ rad/s is superior to other two in terms of robustness to frequency variations, yet also contributes significant amount of negative phase around 10Hz.

D2. Concept generalization

In case residual harmonic content in (1) is significant, DC link voltage ripple in (9) may include additional multiples of ω_G, i.e.

$$\Delta v_{DC}(t) = \sum_{n\geq 1}^{N}\Delta V_{DCn}\sin\left(n\omega_G t+\varphi_n\right). \quad (39)$$

In such a case, (27) should be generalized as

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$$C_{DC}^{FS} = \begin{cases} \alpha_1 C_{DC}, & \omega_G - \Delta\omega_1 < \omega < \omega_G + \Delta\omega_1 \\ \alpha_2 C_{DC}, & 2\omega_G - \Delta\omega_2 < \omega < 2\omega_G + \Delta\omega_2 \\ \vdots & \vdots \\ \alpha_N C_{DC}, & N\omega_G - \Delta\omega_N < \omega < N\omega_G + \Delta\omega_N \\ C_{DC}, & elsewhere \end{cases} \quad (40)$$

and implemented by series connection of N corresponding notch filters instead of a single one, i.e. $F(s)$ in Fig. 5 should be replaced with

$$\prod_{n\geq 1}^{N} F_n(s), \quad F_n(s) = \frac{s^2 + \frac{2\Delta\omega_n}{\alpha_n} s + (n\omega_G)^2}{s^2 + 2\Delta\omega_n s + (n\omega_G)^2}. \quad (41)$$

Note that the center frequency of the highest-order notch filter $N{\cdot}\omega_G$ must reside well within the bandwidth of DC link voltage loop in Fig. 4 in order to preserve stability.

V. Verification

Consider a 350W commercial boost converter-based Texas Instruments UCC28180EVM-573 Power Factor Correction Rectifier (PFCR) board, shown in Fig. 7 [40]. The converter is managed by UCC28180 controller, operating under average current mode control at a fixed programmable switching frequency of 120 kHz, under external analog type-II voltage loop compensation with V_{DC}^{*} = 400V. The PFCR employs a 270μF electrolytic DC link capacitor. Manufacturer provided DC link voltage loop gain is depicted in Fig. 8 [40], indicating crossover frequency of $\omega_{CV} \approx 2\pi{\cdot}9$ rad/s with ~70° phase margin.

In order to verify the proposed methodology, the 270μF electrolytic capacitor was removed and replaced by EC as shown in Fig. 9(a), employing L_A = 320μH, C_A = 25μF and C_R = 4.7μF with the latter serving as switching-ripple absorbing capacitance. The EC was operated at 50kHz switching frequency and controlled digitally by a TMS320F28332 digital signal processor (DSP) with V_A^{*} = 270V, employing nonlinear control algorithm reported in [29]. DC link voltage controller H_{VOLT} (cf. Fig. 4) was realized by a cascaded dual-loop structure utilizing inductor current as inner variable to reduce the sensitivity to possible inductance value drifts [23]. It was experimentally validated in [29] that current loop behavior remains nearly unchanged within the whole load range allowing to increase EC DC link voltage loop bandwidth up to ~4000π rad/s. The resulting crossover frequency is thus significantly higher than $2\omega_G$ = 200π rad/s so that the influence of $F(s)$ in (32) would be negligible, as desired.

Switches S_1 and S_2 were implemented by Infineon 20N60C3 MOSFETs, driven via International Rectifier IR2113 driver by PWM ports of the DSP. Experimental setup is pictured in Fig. 9(b) with EC circuit data summarized in Table I. During experiments, the PFCR was fed by APS-7100 Gwinstek programmable AC power source operated as 50Hz, 230V mains and terminated by M9715B Maynuo DC electronic load, operated in constant power mode. EC ability to mimic the behavior of 270μF electrolytic DC link capacitor under both linear and nonlinear control algorithms was validated in [27] – [29] and is not examined here.

Fig. 7. UCC28180EVM-573 Power Factor Correction Rectifier board.

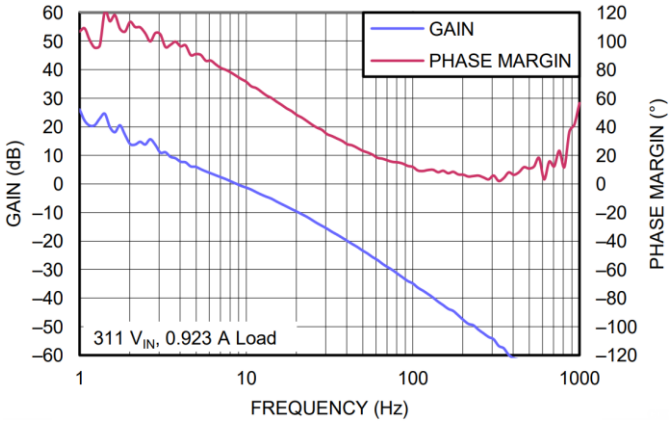

Fig. 8. Bode diagram of UCC28180EVM DC link voltage loop gain [40].

TABLE I. EC PARAMETER VALUES

Parameter	Value	Units
Switching and sampling frequency	50	*kHz*
Inductance, L_A	320	*μH*
Auxiliary capacitance, C_A	25	*μF*
Ripple capacitance, C_R	4.7	*μF*
Auxiliary reference voltage, V_A^{*}	270	*V*
Rated power, P_L	350	*W*

Prior to methodology verification, AC power source voltage *THD* was measured and found to be 0.5%, as shown in Fig. 10. This value should be taken into account in order to correctly interpret measured values of grid current *THD*. Two EC control algorithms were adopted: one employing classical capacitance emulation subsystem of Fig. 3(c) and the other implementing frequency-variant capacitance emulating subsystem of Fig. 4, employing a notch filter tuned to $\omega_G = 2\pi{\cdot}50$ rad/s with ψ_{max} = 1° (cf. (37), i.e. $\Delta\omega = 20\pi$ rad/s was selected according to (38). The band-stop filter was implemented using a typical second-order-section (SOS) IIR structure [41]. Corresponding voltage loop Bode diagrams are shown in Fig. 11. Note that voltage loop frequency characteristics of PFC terminated by EC employing classical capacitance emulation subsystem is nearly identical to that of PFC utilizing the original electrolytic capacitor (cf. Fig. 8). On the other hand, it is well-evident that utilizing the proposed frequency-variant EC has negligible effect on the voltage loop within PFC voltage loop bandwidth, as desired. Crossover frequency and phase margin remain nearly the same and the influence of band stop filter noticeable

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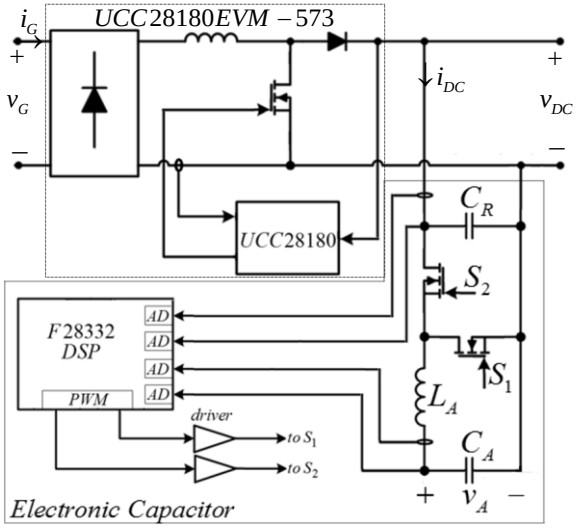
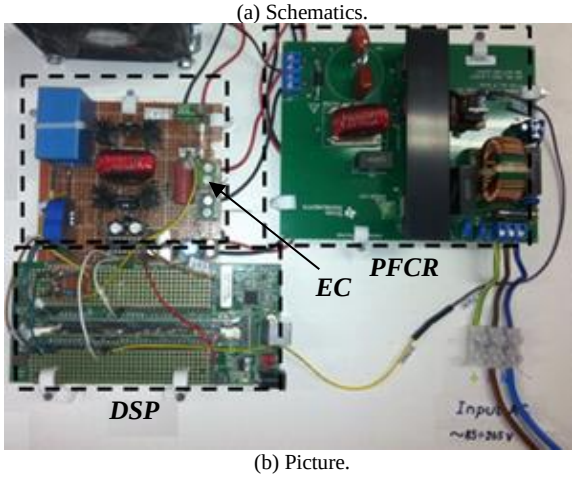
around double-mains frequency is characterized by 33dB gain margin, verifying the stability and assuring robustness.

Two experiments were conducted to examine the performance under each algorithm. In the first one, steady-state operation under rated load under nominal grid frequency (50Hz) as well as under ±2% deviations (49Hz and 51Hz) was inspected. Corresponding experimental results are depicted in Fig. 12.



(a) Schematics.



(b) Picture.

Fig. 9. Experimental setup.

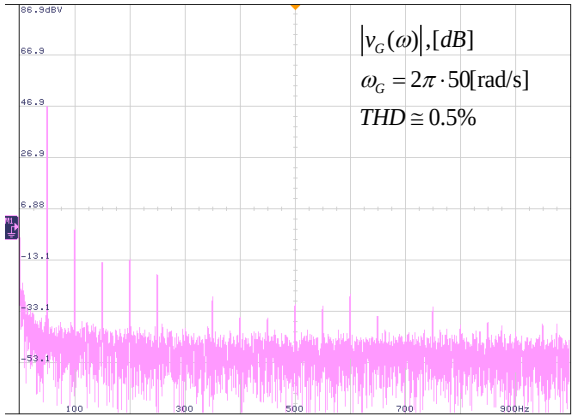


Fig. 10. Measured spectra and corresponding voltage *THD* of APS-7100 AC source.

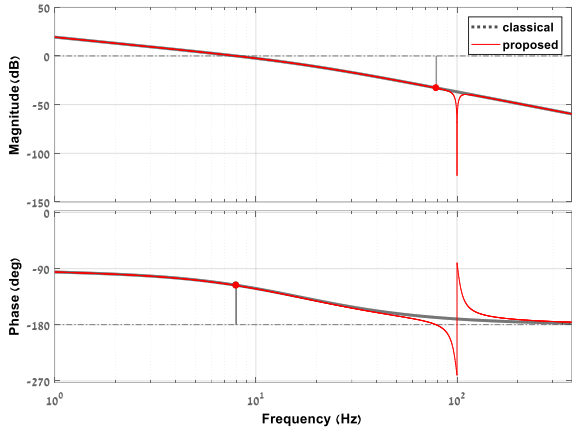


Fig. 11. Voltage loop Bode diagrams of EC-based PFC.

Performance of the system under classical control algorithm was not affected by mains frequency variation, thus only 50Hz-related results are shown for brevity. Similarly to the original UCC28180EVM-573 board operation, measured DC link ripple and THD_i were ~12Vpp and 4.5%, respectively. Taking into account AC power source voltage *THD*, measured value of THD_i correlates well with manufacturer-reported value under rated loading. On the other hand, both DC link voltage ripple magnitude and grid-side current *THD* were significantly reduced under the proposed control algorithm. Under nominal mains frequency of 50Hz, DC link voltage ripple was nearly eliminated and the residual high-frequency content was mainly imposed by switching frequency components. The value of THD_i was reduced more than twice due to significant third harmonic reduction, as shown in Fig. 13 demonstrating corresponding grid-side current spectra. As mentioned in Section III, complete elimination of ΔV_{DC} and THD_i is not practical.

When the notch filter was detuned by shifting the mains frequency from its nominal value by ±2%, system performance under proposed control algorithm has deteriorated as expected, yet remained superior to that employing the classical control algorithm. DC link voltage ripple magnitude increased yet remained 4 times lower than that of the system without notch filter. Likewise, the value of THD_i has risen yet remained significantly lower than that of the system utilizing the classical control algorithm. Fig. 14(a) summarizes measured values of THD_i versus grid frequency $f_G = \omega_G/(2\pi)$ under rated loading for both cases and Fig. 14(b) presents measured values of THD_i versus load current for f_G = 50Hz. Regarding the latter, it is important to emphasize that THD_i vs load current curve of PFC terminated by EC employing classical capacitance emulation subsystem is very close to that of original Texas Instruments UCC28180EVM-573 Power Factor Correction Rectifier (PFCR) board [40, Fig. 5]. Since the PFCR operates in discontinuous conduction mode for load currents below 0.8A, corresponding THD_i is formed by additional current harmonics (not just the 3rd one) and thus increases with load decrease. Nevertheless, band stop filter influence on THD_i remains nearly unchanged and therefore PFCR utilizing the proposed frequency-variant EC outperforms the one employing classical capacitance emulation subsystem for the whole load current range.

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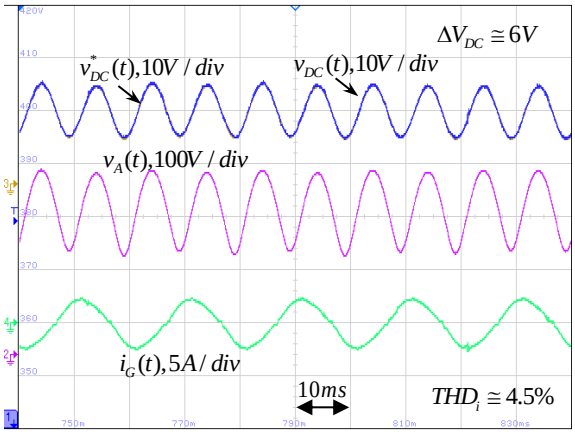
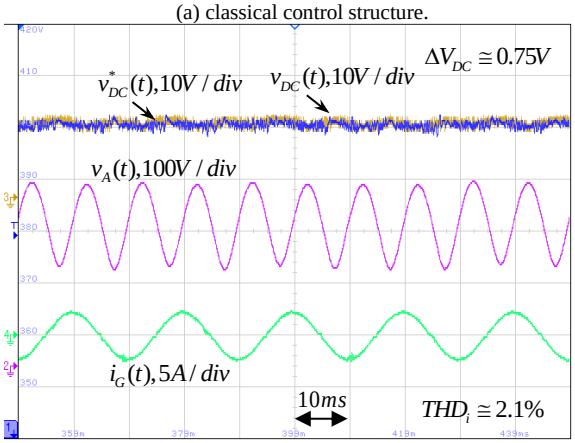
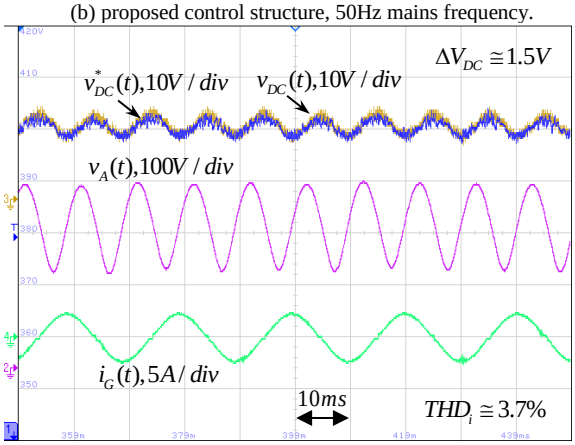


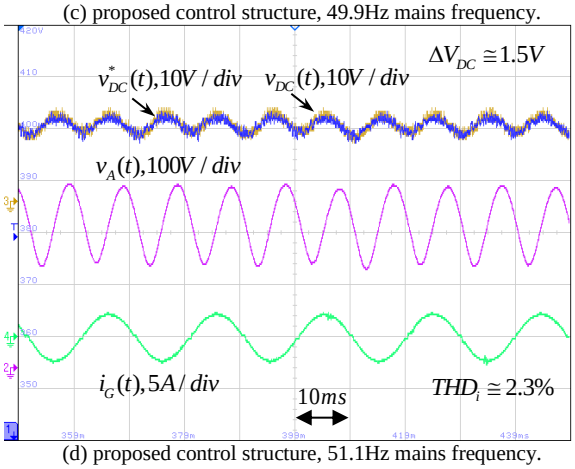
(a) classical control structure.



(b) proposed control structure, 50Hz mains frequency.

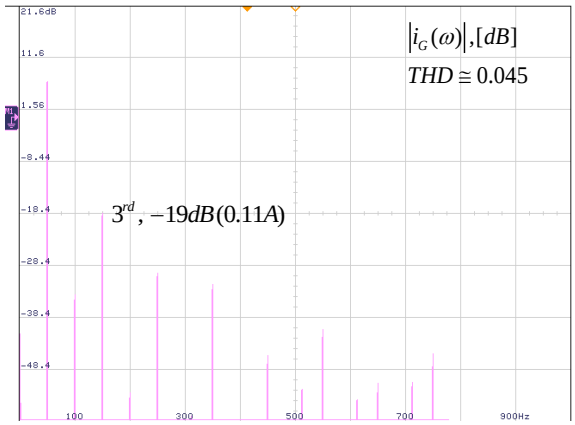


(c) proposed control structure, 49.9Hz mains frequency.

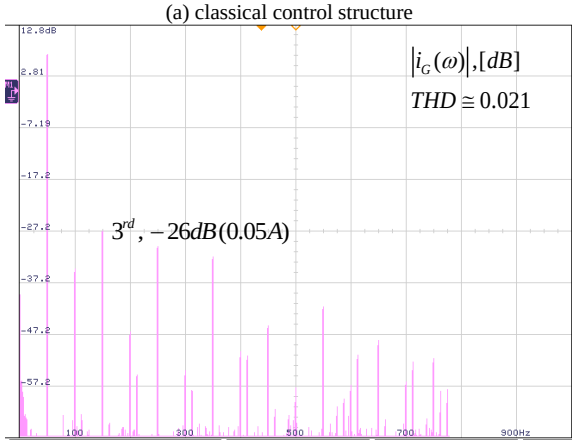


(d) proposed control structure, 51.1Hz mains frequency.

Fig. 12. Experimental results: steady-state performance under full load of EC-based system.

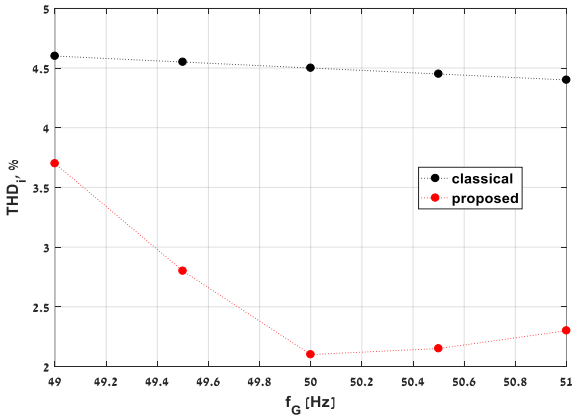


(a) classical control structure

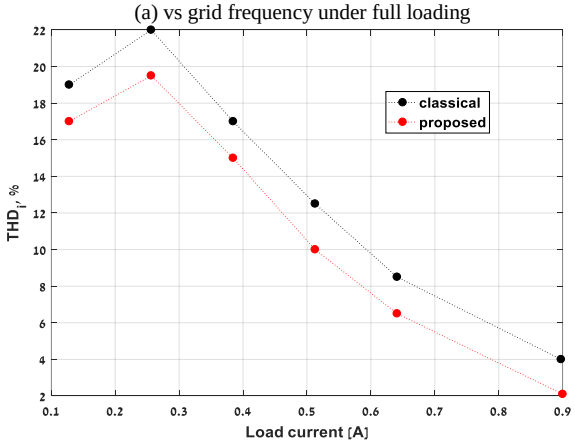


(b) proposed control structure

Fig. 13. Measured grid-side current spectra for main frequency of 50Hz.



(a) vs grid frequency under full loading



(a) vs load current for f_G = 50Hz.

Fig. 14. Measured *THDi* values summary.

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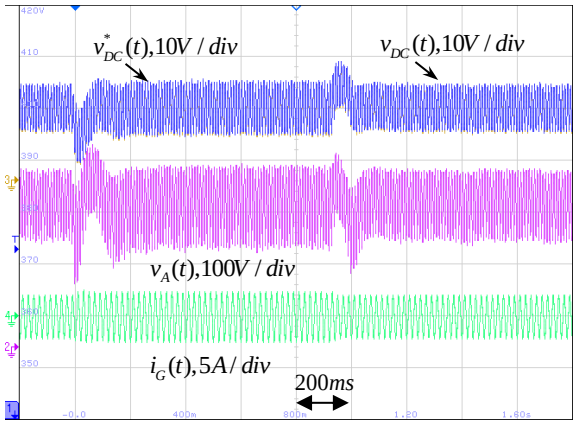
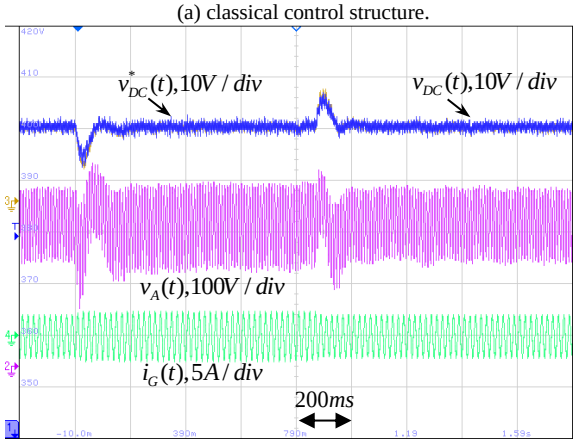
In the second experiment, transient response of the system to ±50W load power steps around rated loading was inspected. Corresponding experimental results are depicted in Fig. 15. It is well-evident that dynamic responses of both systems (6V overshoot/undershoot and 90ms settling time, matching well with expected values calculated according to [31] for 50W load step) are very close, verifying the fact that the performance of DC link voltage control loop was unaffected by band stop filter inclusion. It is interesting to emphasize that while DC link voltage of the system employing classical control algorithm possesses significant low-frequency ripple, its frequency-variant-capacitance algorithm based counterpart is nearly low-frequency ripple-free, as desired. Nevertheless, responses of auxiliary voltage and grid-side current are nearly identical, indicating that the value of DC link capacitance "seen" by the voltage controller of the PFCR is indeed the same in both cases, verifying the concept of frequency-variant capacitance.



(a) classical control structure.



(b) proposed control structure.

Fig. 15. Experimental results: transient responses to 300W-to-350W-to-300W load power steps of EC-based system.

VI. Conclusion

The paper proposed and validated a modified control algorithm allowing to achieve simultaneous reduction of DC link voltage ripple and grid-side current total harmonic distortion compared to those attained by classical solutions in grid-connected energy conversion systems, employing Electronic DC link Capacitor. The proposed modification, based on emulating a frequency-variant capacitance instead of a constant one, does not change either the ability of Electronic Capacitor to replace certain valued physical capacitance in a plug-and-play manner or DC link voltage loop dynamics of the grid-connected converter. Experiments validated the proposed method. Future work on the subject includes DC link dynamics improvement for a given value of grid-side current total harmonic distortion of grid-connected energy conversion systems, employing Electronic DC link Capacitor.

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