PFM-PWM Digital Controller for Miniaturized High-Frequency Isolated *LLC* Converters Integrated in Advanced IoT Devices

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***Abstract*—This article introduces a highly miniaturized soft-switched power supply suitable for advanced Internet-of-things applications. It incorporates an HB-LLC resonant converter operating in the megahertz range and a new pulse frequency modulation (PFM)-PWM digital controller that facilitates tight output voltage regulation carried out through a simple voltage loop controller hardware. The switching frequency and the duty cycle are adjusted simultaneously to enhance output voltage regulation capabilities while full continuity is achieved through a combined pulsewidth and frequency modulation scheme and the utilization of a new high-resolution digital pulsewidth modulator with time resolution of a single delay element. The controller's dual-loop architecture incorporates two proportional–integral compensators to guarantee smooth recovery from load transients or input voltage aberrations. The controller accounts for the nonmonotonicity attribute of asymmetrically driven *LLC* resonant converters by carrying out dedicated mitigation sequences for low-*Q* operation. The operation of the controller is experimentally verified on a 3–7 V input HB-LLC converter, demonstrating excellent voltage regulation capabilities and significant reduction of the passive components' stress during startup.**

***Index Terms*—Delay-line (DL), digital control, digital pulsewidth modulator (DPWM), *LLC* converter.**

I. Introduction

THE advent of highly compact portable electronics, such as smartphones and wearable Internet-of-things (IoT) devices, and the widespread adoption of cyber-physical systems across numerous automation and manufacturing environments as part of the industry 4.0 era has significantly increased the need for low-power highly-miniaturized and integrated power supplies [1], [2], [3], [4], [5], [6], [7]. These power supplies may be incorporated in low-power IoT devices, such as location beacons or asset tags which due to their limited power consumption and short operating periods are typically battery operated [8]. In these applications, the power delivery requirements are significantly eased compared to IoT and industry Internet-of-things (IIoT) devices that perform frequent and long-term paring with adjacent devices or cloud via complex and power-hungry communication protocols [9]. These devices, for example, play a key role in industrial automation by enabling the integration of industrial machinery and cloud computing through real-time data acquisition. This is achieved by continuously collecting data through a network of advanced IIoT devices, which incorporate sensors, computing accelerators, wireless communication modules, etc. Moreover, since a nonnegligible amount of power is required to perform the aforementioned tasks, energy harvesting taking advantage of mechanical movements [10], RF [11], [12], or heat [13] is employed, easing the power source requirements at the expense of noise injection.

These small-volume switched-mode power supplies (SMPS) can be incorporated to generate the main device's voltage rail or placed in critical locations regulating the input voltages to sensitive loads, such as sensors or communication modules, thus allowing each power consumer to operate with its nominal input voltage, which directly translates into improved overall system performance. When integrated into battery-powered or energy-harvesting-based devices, these power supplies are required to sustain regulated output voltage while drawing energy from a wide-ranging input that is a function of the battery state of charge [14], [15]. Moreover, they are required to support loads that draw power in pulses, such as instant-order IoT buttons, and to sustain well-regulated output voltage under significant input voltage variations, which may arise from draining the energy-harvesting storage element. In addition, distributed-power architectures of industrial, medical, and automotive applications require isolated point-of-use power conversion to minimize noise in sensitive analog circuitries, generate internal isolated power sources, and supply different voltage rails [16], [17], [18]. Such power supplies typically comprise a highly compact transformer and several separate ICs alongside off-chip passive components, which translate into increased overall solution volume [19].

In the context of IoT power-delivery architectures, advanced IoT devices are considered those with a power range of <1 W and input voltage of 4.5–5.5 V [20], [21]. Apart from the discussed miniaturization requirements, these SMPS are required to provide galvanic isolation and to maintain efficiency above 50% for substantial load conditions (>0.5 W). Moreover, they are required to support smooth transitions when the device initiates

Manuscript received 16 January 2023; revised 18 April 2023, 25 June 2023, and 17 August 2023; accepted 19 September 2023. Date of publication 25 September 2023; date of current version 6 December 2023. This work was supported by the Israel Science Foundation under Grant 2186/19. Recommended for publication by Associate Editor Q. Li. *(Corresponding author: Mor Mordechai Peretz.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3318645.

Digital Object Identifier 10.1109/TPEL.2023.3318645

or terminates various power-saving modes of operation and to ensure high-resolution (HR) steady-state voltage regulation for the entire range of conversion ratios and loading conditions.

Accordingly, low-power small-volume power supplies have been presented in [5], [21], [22], [23], [24], [25], and [26], which mainly rely on advancements in fabrication technology for the power-stage transistors and integrated peripheral units, such as analog-to-digital converters (ADCs), digital-to-analog converter (DACs), and pulsewidth modulation (PWM) modulators. In most cases, the need for inductive elements sets limitations on the integration level of such solutions since on-chip inductors require dedicated fabrication processes and come with a cost of high-order effects that need to be compensated by the controller [27], [28]. As a result, inductorless power converters have gained interest that allowed significant volume reduction at the expense of efficiency and limited voltage regulation capabilities [29], [30], [31]. Recent advancements in small-volume high-frequency monolithic [32], [26] and nonmonolithic [33], [34] transformer design and manufacturing have cleared the way for converter families that utilize the transformer's leakage and magnetizing inductances to minimize the overall solution volume while ensuring galvanic isolation, such as the *LLC* resonant converter [35], [36].

High efficiency and power-density attributes of the *LLC* resonant converter have made it the topology of choice in many medium- and high-power applications [37], [38], [39], [38]. Detailed loss analysis presented in [40] and [41] specifics the main loss contributors of FB- and HB-LLC configurations. However, integration in low-power applications remains a challenge due to the relatively high switching-frequency required to ensure compact realization and the strict voltage regulation requirements of state-of-the-art loads. To the best of the authors' knowledge, the realization of high-frequency *LLC*-based SMPS for low-power applications is a relatively new approach enabled by the above-mentioned advancements in transformer manufacturing but still restricted to conventional frequency-based control schemes and controller realizations.

Traditionally, frequency modulation (FM) control with a 50% duty cycle is employed to control the delivered power to the load [36], [42]. Nonlinear control schemes and mixed-signal controller realizations may also be incorporated in *LLC*-based power supplies, usually for medium and high output power ratings [43], [44]. While such solutions provide a superior transient response, their respective controllers comprise a relatively large number of costly peripherals, such as high-bandwidth amplifiers and comparators. When operating at high switching frequencies, FM control may lead to performance degradation due to the large frequency variations introduced by conventional PWM modulators, limiting the frequency resolution and thus the voltage regulation capabilities of the controller [45]. For example, in counter-based PWM modulators, the frequency resolution decreases according to the square of the converter's switching frequency [47], thus introducing undesirable gain oscillations and nonzero steady-state error during high switching-frequency operation. This issue can be addressed by increasing the internal clock frequency, which adds design complexity and increases power consumption, or by incorporating HR submodules [21], [46], [47]. To address this issue, hybrid pulse frequency modulation (PFM)-PWM control schemes have been presented in [42], [48], [49], [50], and [51] for high-Q loads for both half-bridge and full-bridge *LLC* configurations. Here, first-harmonic approximation and continuous conduction mode (CCM) have been assumed valid for the entire range of loading and switching conditions, which results in monotonic gain dependency on the duty cycle. For example, in [49], conventional frequency control is employed to eliminate the majority of the error while the duty cycle is slowly updated to maintain the output voltage within the zero-error bin. The controller realized in [49] assumes that the output voltage is a monotonic decaying function of the duty cycle, which allows a simple and straightforward compensator design. This, however, is not the case for low-Q operations where the gain characteristics are load-dependent and nonmonotonic. Since IoT devices include multiple sleep and hibernate modes to minimize power dissipation, the operation of the *LLC* converter is considered a low-Q operation, which requires dedicated control algorithms and procedures to ensure well-regulated output voltage for the full range of loading conditions.

In the context of low-volume SMPS, and specifically in resonant-based topologies, the modulator's drive capabilities have a nonnegligible impact on the miniaturization efforts and regulation capabilities. These modules are characterized by their time-resolution, frequency, duty-cycle ranges, and dynamic performance. The conventional approach to implement an HR digital pulsewidth modulator is by a fast-clocked counter-comparator scheme [52]. Here, the required resolution and switching frequency determine the internal clock resources and, therefore, the dissipated power. In this way, n-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n \cdot f_s$. This approach features a relatively small silicon area and low computational resources but results in increased power consumption and complex design to realize the high-speed circuitry and, therefore, not suitable for IoT applications. An alternative approach for FPGA-based realizations of digital controllers' takes advantage of modern FPGA resources, such as digital clock manager (DCM) modules, which enable clock frequency manipulations such as duplication, multiplication, division, and phase shifting [53]. However, this approach entails the utilization of very high-frequency clock resources and expensive analog components to realize the drive circuitry with additional extensive redesign efforts when transitioning between different programmable platforms or into a dedicated application-specified integrated circuit (ASIC) solution. An alternative approach that is suitable for cross-platform implementation relies on delay-line (DL) based structures to achieve HR attributes without increasing the internal clock frequency—this has been perused in this study.

The objective of this article is, therefore, to introduce a very light digital controller architecture and realization for highly miniaturized and low-power HB-LLC resonant converter-based power supplies, as shown in Fig. 1. The new digital controller supports operation in the megahertz range and, therefore, is suitable for integration in highly compact IoT devices. The two control variables, i.e., the switching frequency and the duty

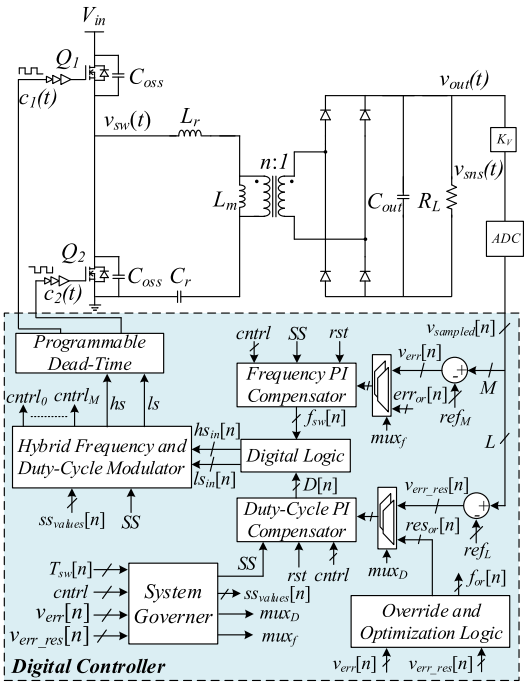

Fig. 1. Simplified block diagram of the PFM-PWM digital controller regulating the output voltage of an HB-LLC resonant converter.

cycle, are adjusted simultaneously without any noncontinuities in their controllers' operation to compensate for load transients and input-voltage aberrations and to ensure tight output voltage regulation. The implemented control law is based on a conventional single-loop control scheme with lean hardware requirements and is designed to support converters with load-dependent gain characteristics, such as the HB-LLC resonant converter. It is a further objective of this study to describe the entire controller in hardware description language (HDL) using standard-cell libraries without extensive custom design to allow fast adoption and implementation regardless of fabrication technology and to produce an ASIC-ready version of key modules that may also be applicable in additional controller architectures. Among them is a new DL-based digital HR variable-frequency variable-pulsewidth modulator (VFVDM) that produces gating signals with time resolution of a single delay element.

The rest of this article is organized as follows: Section II describes the controller architecture and covers the structure and operation of an asymmetrical HB-LLC resonant converter. Section III details the dual-variable control law, optimized start-up sequence, and a simulation case study. The design of a DL-based variable-frequency variable-duty-cycle pulsewidth modulator is discussed in Section IV. Experimental verification is provided in Section V. Finally, Section VI concludes the article.

II. PFM-PWM Digital Controller Architecture and Operation

The HB-LLC resonant converter shown in Fig. 1 comprises a half-bridge switch network and a resonant tank followed by a transformer and a rectification stage. The transistors of the half-bridge network Q_1, and Q_2 are alternately driven with a short deadtime to produce a unipolar square wave $v_{sw}(t)$, which is the input of the *LLC* resonant tank. It consists of a resonant capacitance C_r and two inductances: the transformer's leakage inductance L_r and the transformer's magnetizing inductance L_m. The excited resonant network produces a sinusoidal-like resonant current $i_r(t)$ that is transferred to the transformer's secondary side when the diodes of the rectification stage are forward-biased. The resonant capacitor also acts as a blocking capacitor, sustaining a dc value according to

$$\bar{v}_{cr} = D \cdot V_{in} \tag{1}$$

where D is the duty cycle of the half-bridge PWM drive signals. The rectified ac current is then filtered by the output capacitor C_{out} to maintain a steady output dc voltage. The power-stage design procedure and the allowed switching range in this study follow traditional design guidelines to ensure soft-switching of the HB transistors and zero current switching (ZCS) for the bridge rectifier's diodes [36], [37], [38]. This entails sufficient current flowing at the switching instance to charge or discharge the junction capacitances (discussed next). The control objective in this article is to sustain a regulated output voltage for any setting of the input voltage and loading conditions (within the design specifications) by adjusting the converter's switching frequency and duty-ratio settings.

A. Controller Architecture and Operation

As can be seen in Fig. 1, the controller follows a conventional single-loop configuration based on an all-digital voltage loop. The output voltage $v_{out}(t)$ is sampled by an ADC to produce a digital representation of the output voltage $v_{sampled}[n]$, which is internally divided into two sections. The *Frequency Compensator* (see Fig. 1) produces a digital representation of the switching frequency $f_{sw}[n]$ based on the M-MSBs of the digitized output voltage and its corresponding error signal $v_{err}[n]$. The LSB section of $v_{sampled}[n]$ is compared with an L-bit long reference signal $ref_L[n]$ to generate the residual error signal $v_{err\_res}[n]$, which during normal operation is the input of the *Duty-Cycle Compensator*, as shown in Fig. 1. Therefore, two error signals are derived from a single controlled variable, i.e., v_{out}, by dividing the digitized error result into MSB and LSB sections. These fractions of the digitized error are utilized to produce two correction signals, i.e., the instantaneous duty cycle and switching frequency commands, as shown in Fig. 1.

The LSB and MSB sections of the digitized output voltage are tailored from the controller's PWM modulator frequency resolution Δf and the ADC's resolution v_{adc}. The first dictates the controller's voltage regulation capabilities, defined by the smallest output voltage change Δv_{min} as a result of Δf change in the switching frequency and the latter sets the overall zero-error bin. The LSB section is chosen to assure $2^L v_{adc} < \Delta v_{min}$ for the entire range of operating and loading conditions and the MSB section comprises the remaining bits of the sampled output voltage $v_{sampled}[n]$, as illustrated in Fig. 1.

In some cases, due to the nonmonotonicity of the converter's gain with respect to the duty cycle, the controller ignores the internal error signals and imposes values with known polarity

and magnitude on the inputs of the two proportional–integral (PI) compensators to guarantee convergence. This is carried out by the *System Governor*, which dictates the operation mode of the controller and by the *Override Logic* block that calculates its override values $err_{or}[n]$ and $res_{or}[n]$. The inputs of the HR VFVDM are produced by the *Digital Logic* block that translates the digital representation of the switching frequency ($f_{sw}[n]$) and the duty cycle ($D[n]$) into two on-time commands $hs_{in}[n]$ and $ls_{in}[n]$. Finally, the *Programmable Deadtime* adds the required deadtime to ensure ZVS and generates the drive signals to the power stages $c_1(t)$ and $c_2(t)$.

The digital controller is entirely described in HDL and segmented into distinct submodules, each carrying a specific control-related task, as shown in Fig. 1. This allows for strict timing constraints enforcement during the synthesis process. These constraints are written as SDC files and allow for sufficient time intervals per submodule to execute its task while taking into account the potential variations in the reference clock signal due to PVT variations. For example, the dedicated mitigation sequences that account for the nonmonotonicity attribute of the converter are executed in a digital manner by the *System Governor* and *Override Logic Blocks* (see Fig. 1), and therefore, their operation is validated during the static timing analysis phase of the design.

The controller adjusts the switching frequency to compensate for relatively large deviations of the output voltage ($v_{err}[n] \neq 0$) while duty-cycle adjustments are made as fine-tuning to eliminate small voltage aberrations and to enforce zero steady-state error. This results in an asymmetric operation of the HB-LLC resonant converter, which introduces charge-transfer rate and overall voltage gain dependency on the duty-cycle ratio. Regardless of the operating mode, i.e., symmetric or asymmetric, the *LLC* resonant tank has two resonant frequencies as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$f_n = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}. \tag{3}$$

In case the secondary winding is conducting, the tank's current resonates according to f_r since a constant voltage of nV_{out} is imposed on the primary winding, which eliminates L_m participation in the resonance operation. In case the secondary winding is not conducting, the tank's current resonates according to (3). Here, the voltage on the primary winding is dictated by the effective *LC* resonant tank in which the magnetizing and the leakage inductances resonate with the resonant capacitor. Over the course of a single switching cycle, the resonant current $i_r(t)$ may resonate according to (2), (3), or a combination of the two frequencies, which dictates the conduction mode of the bridge rectifier, i.e., CCM or DCM, and as a result, the power delivered to the load. The controller of Fig. 1 exploits this phenomenon and divides the switching cycle into time intervals with different effective resonant frequencies and rectification stage conduction statuses to maintain the tightly regulated output voltage.

To ensure proper regulation of the output voltage for all conversion ratios, i.e., for the full range of input voltages, the controller supports cross-resonance operation. The allowed switching frequency range is derived from the maximum and minimum input voltages to ensure sufficient gain for any operating conditions and ZVS for the half-bridge transistors [29]. In case $V_{in} < V_{nom}$, the controller operates in the below-resonance mode in which the gain of the resonant tank is greater than unity and step-up voltage-conversion is attained. For the case of $V_{in} > V_{nom}$, the controller operates in the above-resonance mode and the output voltage is decreased due to the reduced gain of the resonant tank. In this mode, the controller may produce drive signals with $D > 50\%$ to compensate for the degraded frequency resolution at high switching frequencies [32]. Asymmetrical operation is enabled for the entire frequency range but is typically carried out when the controller operates in the above-resonance mode. It should be noted that lowering the switching frequency at light load conditions can reduce switching losses but at the cost of lowering regulation accuracy. As discussed above, the dual-variable controller achieves soft switching for the power transistors throughout the operating range, and since the primary goals are miniaturization and enhanced voltage regulation accuracy, lowering the switching frequency is not considered in the controller design.

The timing diagrams of Fig. 2 illustrate key current and voltage waveforms of asymmetrically driven HB-LLC resonant converter operating in closed-loop conditions below [see Fig. 2(a)] and above resonance [see Fig. 2(b)]. As can be seen, ZVS for the power switches is maintained for both operating modes given that enough deadtime is ensured by the controller to allow the resonant current in the tank at the switching instances to charge the parasitic capacitances C_{oss} to the appropriate voltage, i.e., V_{in}-V_F or -V_F. As opposed to symmetrical operation [29], the half-cycle instance cannot be regarded as a focal point for the converter's current and voltage waveforms. Here, the turn-OFF instance of the high-side transistor divides the switching cycle into two asymmetrical time intervals. The first (marked as "I" in Fig. 2) exhibits the operation of a symmetrically-driven HB-LLC resonant converter below resonance in which the resonant current reaches the magnetizing current before the turn-OFF instance of Q_1. At the beginning of this time interval, the rectification stage conducts current and $i_r(t)$ resonates according to (2). Once the resonant current reaches the magnetizing current, the load is supplied by the output capacitor until the end of this phase, and $i_r(t)$ resonates according to (3). As can be seen in Fig. 2, the duration of each subinterval is a function of the converter's switching frequency and the applied duty-cycle ratio. For the entire second time interval (marked as "II" in Fig. 2), the magnetizing current remains smaller than the resonant current (in absolute value) and charge is continuously transferred to the load, which matches the above-resonance operation of symmetrically driven HB-LLC resonant converter operating in CCM. It should be noted that the current and voltage waveforms may differ from the typical cases of Fig. 2 for higher switching frequencies, light-load conditions, or smaller duty-cycle ratios. Regardless, the switching cycle can be divided into two asymmetrical intervals and analyzed in the same manner.

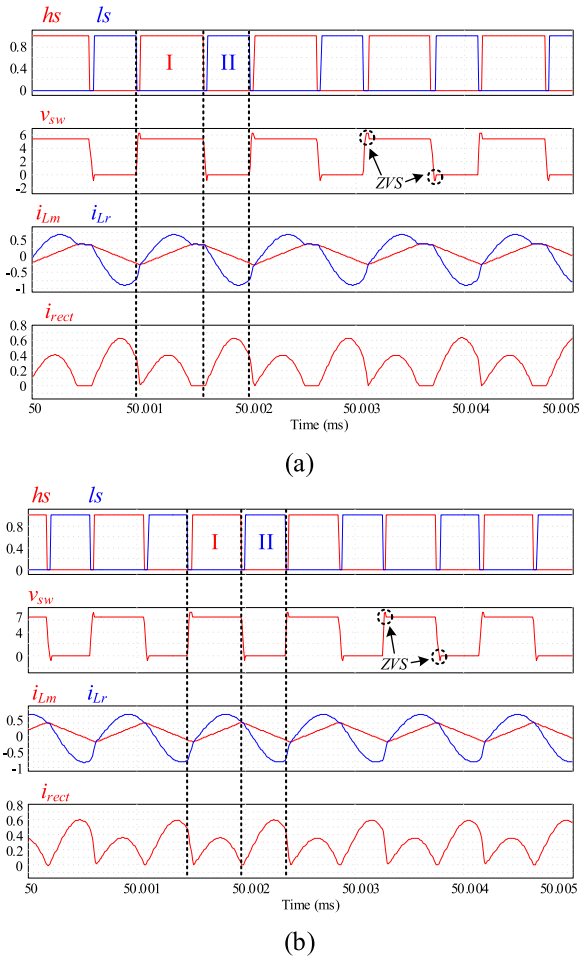

Fig. 2. Timing diagram of an asymmetrical HB-LLC resonant converter operating in closed-loop conditions. (a) Below resonance mode, $f_{sw} < f_r$. (b) Above resonance mode, $f_{sw} > f_r$.

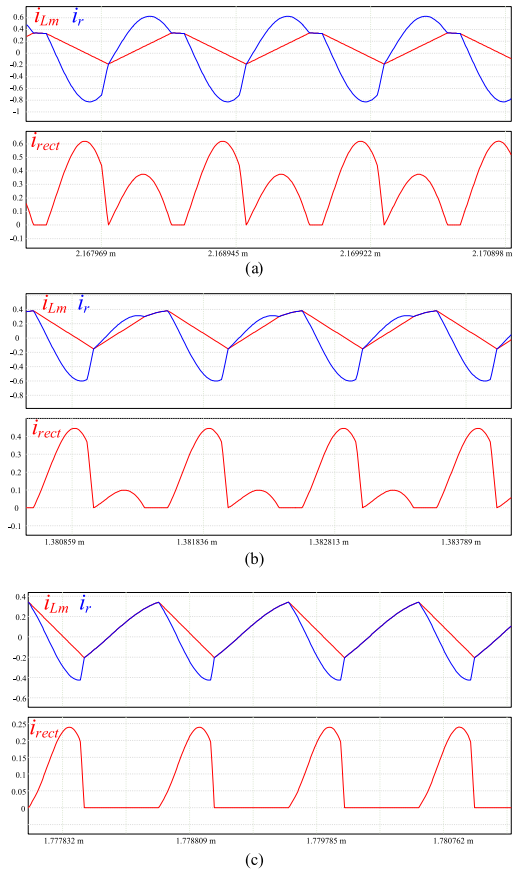

Fig. 3. Timing diagrams of an HB-LLC resonant converter operating with $D = 60\%$ and different loads. (a) $R_L = R_1 < R_{crit}$. (b) $R_1 < R_L = R_2 < R_{crit}$. (c) $R_L = R_3 > R_{crit}$.

B. Impact of the Load Status on the Converter Gain

As the load decreases, the power delivered during the conduction time of Q_1 decreases as well [shown in Fig. 3(a) and (b)] until it reaches zero for $R_L = R_{crit}$, as illustrated in Fig. 3(c). For $R_L > R_{crit}$, the bridge rectifier conducts current only during the conduction time of Q_2 and the HB-LLC resonant converter operates in a similar manner to an asymmetrical half-bridge flyback converter (AHBFC). Regardless of the operating conditions, the overall converter gain can be calculated by the generalized first-harmonic-based expression as follows:

$$A_{DC} = \frac{V_{out}}{V_{in}} \approx \frac{v_{sw}^{\text{rms}} \cdot M\left(f_{sw}, R_{ac}\right)}{\sqrt{R_{ac}/R_L} \cdot V_{in}} \tag{4}$$

where the RMS value of $v_{sw}(t)$ is expressed as

$$v_{sw}^{rms} = \frac{V_{in}}{\sqrt{2}\pi}\sqrt{\sin\left(2\pi D\right)^2 + \left(1 - \cos(2\pi D)\right)^2} \tag{5}$$

and D is the duty cycle of the high-side transistor Q_1. The equivalent resistance R_{ac} and the *LLC* resonant tank gain $M(f_{sw},R_{ac})$ are a function of the conduction status of the bridge rectifier, the switching frequency, the duty-cycle ratio, and the load status [29].

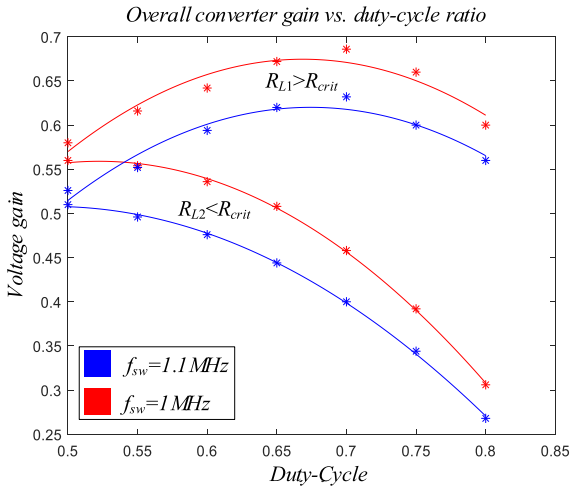

Fig. 4. Asymmetrically driven HB-LLC resonant converter gain curves operating above resonance (blue) and below (red) for two load values: $R_{L1} > R_{crit}$ and $R_{L2} < R_{crit}$.

Shown in Fig. 4 are gain values extracted from the simulation carried out in PSIM for an asymmetrically driven HB-LLC resonant converter along with their respective extrapolated gain curves. The resonant inductor and capacitor values are 37 nH and 0.68 μF, respectively, resulting in a resonance frequency of

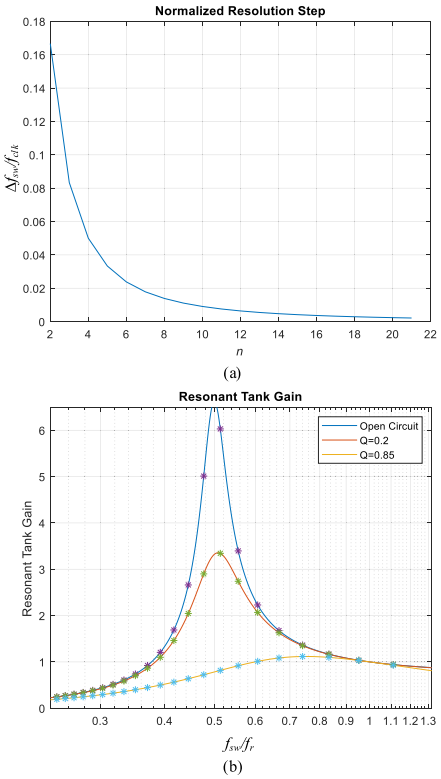

Fig. 5. (a) Normalized frequency resolution as a function of n. (b) Exemplary optional operating points of a symmetrically-driven HB-LLC resonant converter.

1 MHz. Here, the duty cycle is varied from 0.5 to 0.8 for two operating frequencies, $f_1 = 1$ MHz (red) and $f_2 = 1.1$ MHz (blue), and two load values, $R_{L1} > R_{crit}$ and $R_{L2} < R_{crit}$. As can be seen, operating with $D > 50\%$ results in nonmonotonic behavior of the gain with respect to the duty cycle when $R_L > R_{crit}$. The controller's Override Logic block monitors the control variables, i.e., f_{sw} and D, with respect to the output voltage and initiates dedicated control sequences to maintain regulated output voltage during all possible modes of operation [see Fig. 3(a)–(c)].

C. Impact of PWM Resolution on Regulation Accuracy

The voltage regulation accuracy, i.e., the controller's zero-error bin width, is a function of its PWM modulator's frequency and duty-cycle resolutions, as indicated in (4) and (5). For a conventional digital counter-based PWM module, the frequency resolution is a function of the operating frequency as follows:

$$\Delta f_{sw} = f_{clk}\left(\frac{1}{n} - \frac{1}{n+1}\right) \tag{6}$$

where f_{clk} is the base-clock frequency and n is an integer related to the switching period according to

$$f_{sw} = \frac{f_{clk}}{n}. \tag{7}$$

As the switching frequency increases, the frequency resolution decreases exponentially, as shown in Fig. 5(a). Fig. 5(b) demonstrates the relationship between frequency resolution and the operating regions of an HB-LLC resonant converter. Here, the resonant tank gain for various loads is plotted along with its possible operating points. As can be seen, for low switching frequencies, where n is large, the gain difference between two adjacent operating points is small due to the relatively high-frequency resolution, which agrees with Fig. 5(a). For high switching frequencies, where n is small, the frequency variation between two consecutive operating points is much larger, and therefore, the gain difference is significantly bigger. Since the resonant tank's gain is a function of the switching frequency [see (4)], voltage regulation of high-switching frequency converters driven by conventional PWM modulators may lead to resolution-related issues and output voltage deviations.

This can be addressed by increasing the base clock frequency (f_{clk}) or realizing more complex HR frequency modulators operating with a constant 50% duty cycle. Another alternative is easing the resolution requirements from the frequency attribute and utilizing the duty cycle as an additional control variable for the voltage regulation task. This can be carried out, as shown in Fig. 2, for the half-bridge configuration. For a given base-clock frequency, such an approach will result in increased operating points, i.e., a combination of switching frequencies and duty cycle commands, which according to (4) and (5) translates into enhanced voltage regulation accuracy. For that reason, the PWM modulator shown in Fig. 1 is designed to produce gating signals with the time resolution of a single delay element for both its frequency and duty cycle attributes. Its structure and realization are discussed in Section IV.

III. Hybrid PFM-PWM Control Scheme

A. PFM-PWM Voltage Regulation

The voltage regulation task is carried out by two digital PI compensators operating continuously and simultaneously to ensure regulated output voltage while maintaining optimized switching conditions for any load status. The control algorithm is described here with the aid of the flowchart of Fig. 6 and the time-domain simulations of Figs. 7 and 9 with emphasis on the relationship between the two control loops. In this study, *PWM operation* is referred to variations in the duty ratio, while *PFM operation* indicates modifications to the switching frequency. The primary regulation is achieved by typical frequency variation as in *LLC* (PFM), while residual error elimination is achieved by duty-ratio adjustments with a much slower control bandwidth (PWM).

In case $v_{err}[n] \neq 0$, the frequency PI compensator adjusts the converter's switching frequency to eliminate the coarse section of the digitized error signal and to maintain it within its zero-error bin. Switching-frequency modifications are carried out based on the M-MSBs of the error signal without any information on the controller's current duty-cycle ratio or residual error signal $v_{err\_res}[n]$. This is because the frequency loop, which determines the operating mode of the converter, i.e., step-up or step-down mode, is designed with superior control bandwidth compared to the duty-cycle control loop to ensure smooth recovery from abrupt load changes or input voltage aberrations. This is an important control objective since many IoT submodules draw energy in pulses or abruptly change their

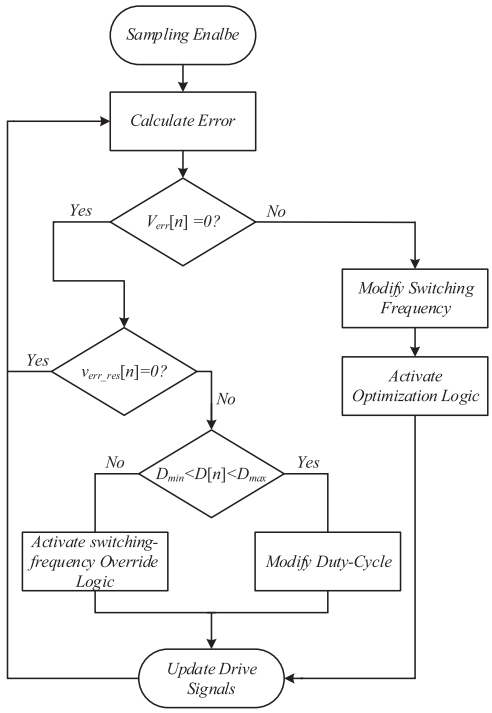

Fig. 6. Simplified flowchart of the PFM-PWM control scheme.

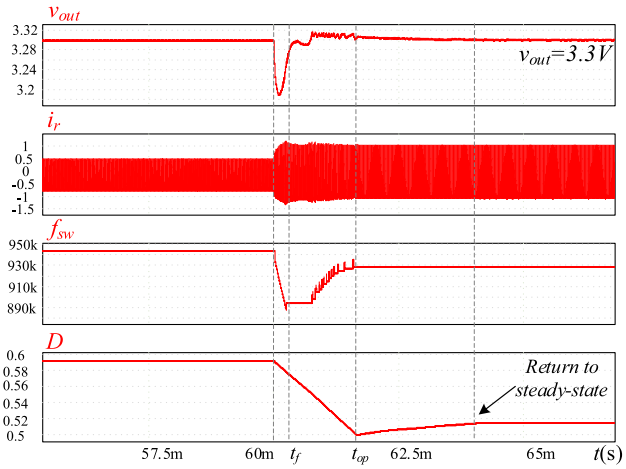

Fig. 7. Hybrid PFM-PWM controller response to a loading-transient event.

power consumption which may result in a significant voltage drop if not properly addressed. This is illustrated in the loading-transient event of Fig. 7, where the frequency loop modifies the switching frequency from transient detection until the MSB section of the digitized output voltage returns to its steady-state window at t_f (see Fig. 7). Nonzero $v_{err}[n]$ value also triggers the control scheme's optimization procedure, as shown in Fig. 6. Upon activation, the duty cycle is slowly and gradually decreased until it reaches the conventional value of 50% used in single variable PFM control schemes. The optimization phase in the loading-transient event of Fig. 7 starts at transient detection and ends at t_{op}. This is carried out by enforcing predetermined negative error at the input of the duty-cycle PI compensator by setting mux_f to logic high, as shown in Fig. 1. Due to the high

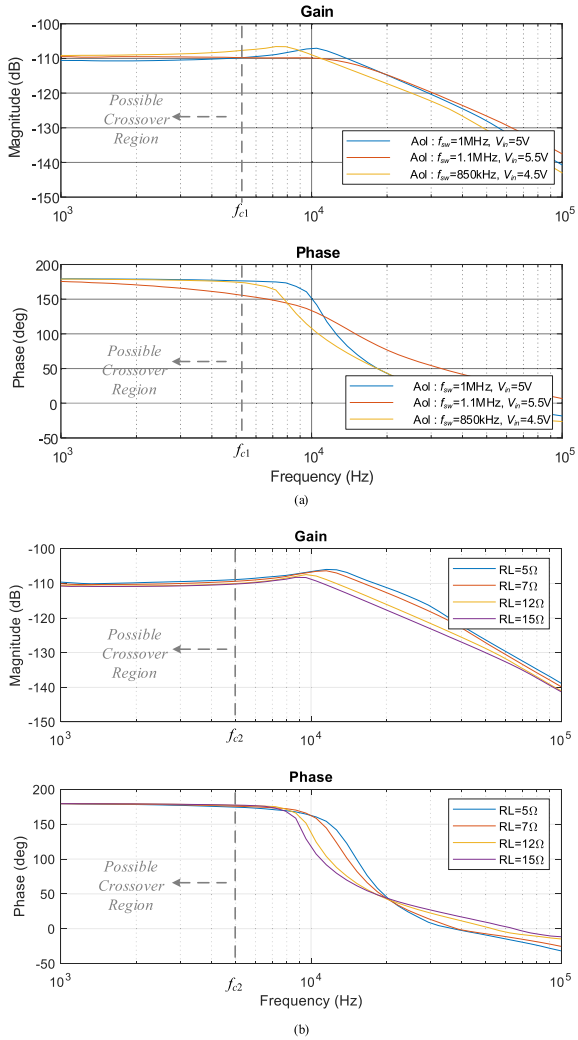

Fig. 8. Control-to-output transfer functions. (a) Multiple input voltage and switching conditions with a constant load resistor, $R_L = 10\ \Omega$. (b) Multiple loading conditions with constant input voltage $V_{in} = 5$ V and switching frequency $f_{sw} = 1$ MHz.

control bandwidth of the frequency loop, the MSB section of the output voltage reaches its zero-error bin before the slowly changing duty-cycle command affects the internal error signals. In case the forced change in $D[n]$ results in nonzero $v_{err}[n]$ value, the frequency PI compensator performs additional modifications to the switching frequency. Such an operation inherently drives the converter toward its optimal operating point, i.e., as close as possible to symmetrical operation for any load status or required conversion ratio. The optimization procedure is terminated when the duty cycle reaches 50% and mux_f is set to logic low, which marks the beginning of the control scheme's fine-tuning phase carried out by the duty-cycle control loop. Shown in Fig. 8 are control-to-output transfer functions for various loading and operating conditions. These transfer functions can be obtained analytically, as described in [54] and [55], or extracted from simulation environments, such as SIMPLIS or PSIM. As can be seen, they exhibit second-order behavior with notable phase and gain differences between the different operating points and loading conditions, which correspond to an IoT device operation

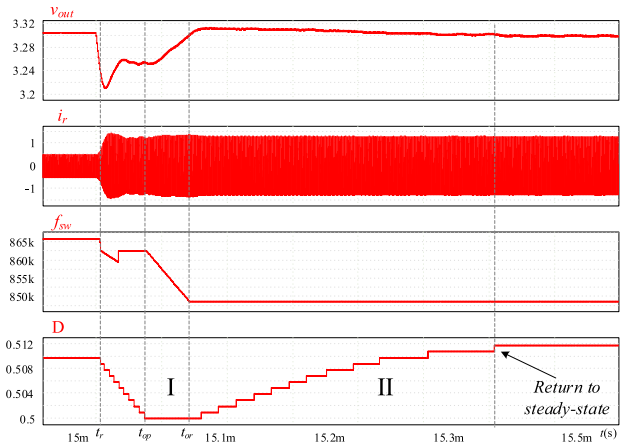

Fig. 9. Hybrid PFM-PWM controller's switching-frequency override and optimization procedures.

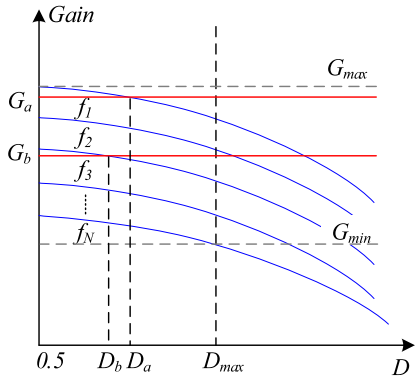

Fig. 10. Illustration of a discrete set of gain curves covering the entire range of required conversion ratios G_{min}–G_{max}.

at nominal load and in hibernate or sleep modes. Therefore, to ensure stable operation for the entire range of loading conditions and input voltages, a simple PI compensator is used to close the loop with a crossover frequency according to the pole locations with adequate margins (f_{c1} and fc_2 in Fig. 8) [54], [57]. Such an approach ensures stable operation with zero steady-state error and very lean hardware requirements with sufficient control bandwidth for the target applications, which focuses on regulation accuracy rather than dynamics [55]. Enhancing the control bandwidth can be carried out by realizing a two-loop structure with a penalty of increased hardware resources, i.e., current sensing circuitry, and therefore is not a viable solution for the target application [57], [58].

During normal operation, $D_{min} < D[n] < D_{max}$, the duty-cycle command is produced as a function of the residual error signal $v_{err\_res}[n]$, as shown in Fig. 6. However, since linear compensators assume monotonicity of their respective plants, additional control routines are included in the control scheme to account for regions where the HB-LLC resonant converter's gain is not monotonic with respect to the control variable, i.e., to $D[n]$, or in case the control variables reach their maximum or minimum allowed values. These routines are initiated during very low-Q operation, i.e., when $R_L > R_{crit}$, to maintain a well-regulated output voltage during hibernate, power-saving, and sleep modes of the IoT device or module. For example, such a routine may be initiated in case $R_L > R_{crit}$ and $v_{err\_res}[n]<0$, which will eventually result in the lowest value allowed for the duty-cycle command, i.e., $D[n] = D_{min}$. Here, the switching frequency is gradually and slowly decreased by setting mux_f to logic high and enforcing a predetermined error signal $\mathrm{err_{or}}[n]$ on the frequency-loop compensator. This results in an increased output voltage, as shown in the timing diagram of Fig. 9 (marked as "I"). Once a positive residual error signal is obtained at the input of the duty-cycle PI compensator (t_{or} in Fig. 9), the override procedure is terminated and the duty cycle is adjusted to comply with the new switching frequency, as shown in Section II of Fig. 9. Additional override routines are also implemented in the control scheme to account for cases where the switching frequency or the duty cycle reaches f_{max} or D_{max}, respectively.

The realized control method described above indicates that the controller does not execute distinct transitioning between two sequencing schemes, i.e., PFM and PWM, but rather varies both control attributes f_{sw} and D simultaneously. In other words, each control loop modifies its control variable as a function of its respective error segment, which may result in frequency modifications, duty-cycle adjustments, or simultaneous alterations of both control variables. The differentiation between consecutive frequency and duty-cycle settings is calculated according to the instantaneous error segments (v_{err} and v_{err_res} in Fig. 1) and the control parameters of the two compensation units, which also dictate the respective bandwidth of each internal control loop. Furthermore, the override control sequences are employed in an open-loop manner upon transient detection, reference voltage modification, or input voltage aberration, which ensures convergence to the new steady-state point, as shown in Figs. 7 and 9. Such an approach significantly simplifies the controller's design since it utilizes the same resources and compensators for both gain regions (see Fig. 4) while ensuring oscillations-free and stable operation. It should be noted that it comes at a cost of fine-tuning mechanism with reduced bandwidth compared to the main control loop since it relies on predefined values for the compensators' inputs rather than on the actual error signals (v_{err} and v_{err_lsb}).

The configurable structure of the dual-loop controller allows increased flexibility in terms of dividing the voltage regulation task between the two control loops and adjusting the HB-LLC resonant converter's operation to comply with application-specific requirements. For example, the internal error signals' widths M and L can be reprogrammed based on the frequency and duty-cycle resolutions and the desired zero-error bin width. As a result, the contribution of the duty-cycle control loop can be restricted to obtain more symmetrical waveforms and, therefore, lower RMS value for the resonant current at the expense of output voltage regulation accuracy. On the other hand, the maximum allowed duty-cycle range can be expanded to allow operation in a discrete set of switching frequencies, f_1–f_N, as a function of the required overall converter gain, as shown in Fig. 10. This attribute significantly reduces filtering efforts typically found in extremely sensitive analog circuitries and alleviates the conditions for limit cycle oscillations in controllers with

limited resolution, particularly when operating at high switching frequency [59], [60]. Moreover, typical *LLC* operation relies on frequency variation for regulation purposes with a significantly narrower frequency band compared to other resonant-based topologies, which eases EMI-related considerations. The inclusion of the additional control variable, i.e., the duty cycle, does not change the fundamental operation of the converter but only improves the control characteristics. Therefore, the design procedure of the EMI filter is simplified and its size can be optimized, yielding reduced EMI-related issues compared to conventional single-variable control schemes. For example, in case the required instantaneous gain is G_a, the converter's switching frequency will be set to f_1 and the duty-cycle value to D_a, while for a gain of G_b, the switching frequency and duty cycle will be f_3 and D_b, respectively.

In this controller architecture, large transitions in frequency are avoided by incorporating a new HR modulator (discussed in Section IV), which allows continuous modifications of both attributes of the drive signals. Therefore, a transition algorithm between PFM and PWM is not required as opposed to controllers that operate with discrete frequency settings [61], which are prone to prolonged interferences or aberrations following modifications of the switching frequency unless a transition algorithm is implemented.

B. Hybrid PFM-PWM Start-Up Procedure

Prior to the closed-loop operation, the controller executes a dedicated start-up sequence to ensure gradual ramping of the output voltage, which significantly reduces potentially harmful inrush currents and voltage spikes. The start-up sequence makes bulky passive filters or extremely high-frequency drive circuitry redundant, thus easing integration efforts and allowing a highly compact design of the IoT device. Moreover, since internal modules of advanced IoT devices may require a unique start-up pattern that is a function of their respective input voltage rails or passive filters, a programmable and adjustable start-up sequence is designed.

Upon procedure initiation, both output and resonant capacitors are fully discharged and the resonant tank's current is zero. As in conventional resonant soft-start procedures, a higher switching frequency is employed compared to f_r to minimize energy flow and to keep the HB-LLC resonant converter in the inductive region. As a result, the tank's current can be regarded as triangular, and assuming constant resonant capacitor voltage per switching cycle, the peak inductor current at the nth switching cycle can be described as

$$I_{peak}^{n} = \frac{V_{in} - v_{cr}}{L_r} T_{on} + I_{n0} = \frac{V_{in} - v_{cr}}{L_r} D T_{sw} + I_{n0} \quad (8)$$

where I_{n0} is the tank's initial current. The maximum peak inductor current I_{peak}^{max} is obtained at the first switching cycle and, therefore, can be used as a design metric for the passive components' stress during startup.

According to (8), both the duty cycle and the switching frequency can be used to limit the peak inductor values and shorten the start-up duration without increasing the passive components' stress. This is carried out by exploiting the PFM-PWM digital controller submodules to produce high-frequency gating signals with below 50% duty cycle. By including both control variables in the start-up sequence, i.e., decreasing the switching frequency while simultaneously increasing the duty cycle, the switching frequency can be lowered and the drive circuitry requirements are significantly eased. This is carried out by the *System Governor,* which calculates the on-time commands, $SS_{\text{values}}[n]$ in Fig. 1, with respect to the initial switching frequency and start-up sequence duration. The timing diagram of Fig. 11 demonstrates the controller's start-up procedure. The initial switching frequency is 1.8× the resonant frequency, the duty cycle is zero and the duration of the start-up sequence is 5 ms. As can be seen, the output voltage gradually increases as does the voltage across the resonant capacitor without any current or voltage spikes. Once the switching frequency reaches the nominal resonant frequency f_r and the duty cycle reaches 50%, the start-up procedure is concluded and closed-loop operation is enabled.

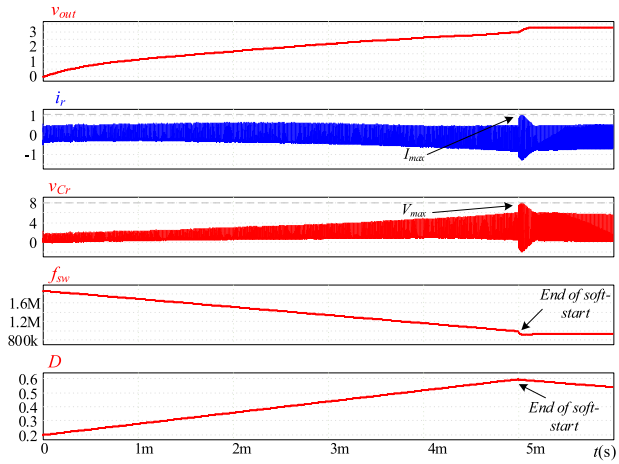

Fig. 11. Hybrid PFM-PWM start-up procedure.

C. Comparison With Single-Variable Control Scheme

Using the analysis and observations from previous sections, a set of simulations has been conducted in PSIM (PowerSim) to verify the effectiveness of the hybrid control scheme and to provide a comparison with single-variable schemes. In this case study, special emphasis is given to the extended regulation capabilities, such as steady-state accuracy and smooth transitions, as a result of load transients. Fig. 12 shows a case of a load step from 10 to 5 Ω of an HB-LLC resonant converter operating with an input voltage of 4 V and a regulated output voltage of 1.8 V. The nominal values of the resonant capacitance resonant inductance and leakage inductance are 0.68 μF, 37 nH, and 2 μH, respectively. Therefore, the resultant nominal resonance frequency of the *LLC* tank is 1 MHz, according to (2). To allow comparison for the applications of interest and to comply with the low-power requirements of IoT devices, the HR-DPWM modules operate at a maximum frequency of 50 MHz.

Closed-loop operation of the asymmetrically-driven HB-LLC converter is shown in Fig. 12(a). As can be seen, the output

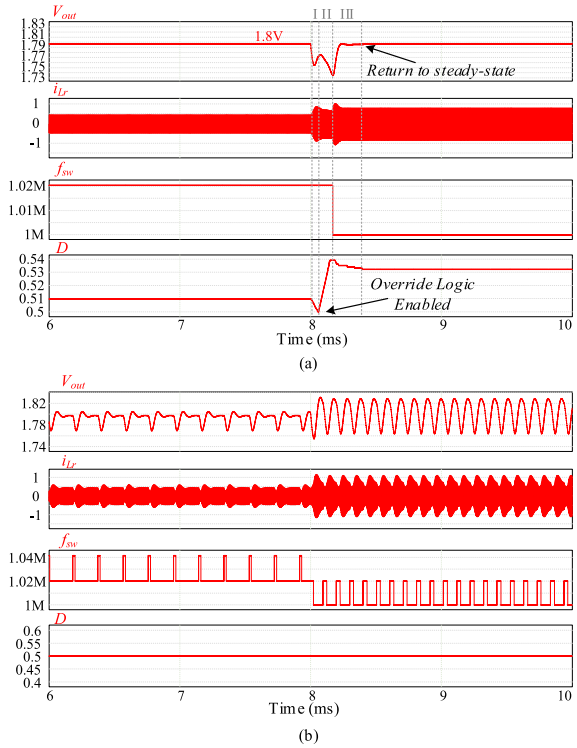

Fig. 12. Simulated response of the hybrid PFM-PWM controller and a conventional frequency controller to a load step from 10 to 5 Ω with $V_{in} = 4$ V and $v_{out} = 1.8$ V. (a) Hybrid PFM-PWM digital controller. (b) Conventional frequency digital controller.

voltage is well positioned within the steady-state window for the two steady-state intervals with different duty-cycle values set by the secondary loop of the hybrid controller, as discussed in Section III-A. Moreover, the switching frequency remains constant (per loading status), which results in small output voltage ripple and resonant current aberrations. Following the transient event, i.e., the increase in output power, the output voltage decreases and the controller modifies the duty cycle according to the flowchart of Fig. 6 [marked as "I" in Fig. 12(a)]. Once the duty cycle reaches 50%, the override logic is activated (marked as Section II) followed by the final phase of duty-cycle adjustments to eliminate the LSB error (v_{err_res} in Fig. 1).

The operation of the same converter driven with symmetrical gate signals, i.e., controlled by a conventional frequency-based digital controller, is shown in Fig. 12(b). While the dynamic performance is comparable, this exemplary case demonstrates the main issues related to conventional PFM control at high switching frequencies, among them limit-cycle oscillations and nonzero steady-state error. This is largely due to the limited number of achievable gain regions, as discussed in Section II-B. At steady state, the switching frequency toggles between two consecutive values (1.04–1.02 MHz and 1.02–1 MHz), which results in large output voltage deviations and resonant current aberrations compared to Fig. 12(a). Moreover, these low-frequency variations require nonnegligible hardware and design efforts to filter, which is a challenging and expensive task in low-volume SMPS design.

It should be emphasized that avoiding limit cycle oscillations by increasing the error band will result in reduced output voltage

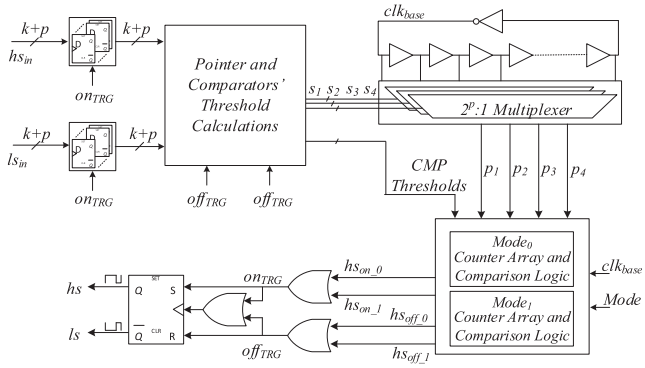

Fig. 13. Simplified structure of the HR variable frequency variable duty-cycle module.

regulation accuracy and, therefore, not suitable for target applications that require a very narrow zero error bin [62]. Moreover, increasing the modulator drive capabilities by utilizing modern FPGA resources such as DCMs, DPLLs, or dedicated HR channels can also be carried out to enhance regulation capabilities. However, this approach entails the utilization of very high-frequency clock resources and expensive analog components to realize the drive circuitry with additional extensive redesign efforts when transitioning to a different programmable platform or a dedicated ASIC solution. Moreover, enhancing the regulation accuracy by increasing the time resolution alone without modifying the modulation technique becomes impractical at higher switching frequencies, an issue that can be avoided by implementing the hybrid control scheme. Therefore, maintaining stringent voltage regulation in this study is achieved by utilizing two control loops and partitioning the digitized error signal alongside carrying an asymmetrical gating scheme as discussed earlier. Such an approach, together with HR drive capabilities (discussed next) introduces additional gain regions, as shown in Fig. 10, which supports the usage of a narrow zero-error bin while at the same time eliminating undesired low-frequency oscillations of the output voltage. This is further discussed in Section V.

IV. High-Resolution Variable-Frequency Variable-Duty-Cycle Modulator

The modulator in this study supports operation in the megahertz range with HR attributes for both f_{sw} and D without utilizing expensive clock circuitry, thus allowing power efficiency with lean hardware requirements modulator realization. Its time resolution is a function of the fabrication process for an integrated realization or the FPGA delay elements for a controller realization on a programmable platform. Here, a single delay-element resolution is attained for both attributes of the drive commands, which enables implementation of hybrid control laws at high switching frequencies thus allowing the use of miniaturized transformer and rectification stages without compromising on accuracy.

The operation of the VFVDM (functionality block depicted in Fig. 13) is described through the details of its configuration and its main building blocks. It comprises a single DL-based ring-oscillator to generate the base clock signal (clk_{base}), a

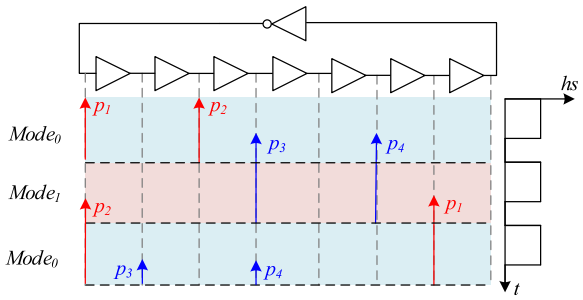

Fig. 14. Illustrative example of the internal pointers of the HR drive logic.

multiplexer array to produce its time-delayed replicas (p_1–p_4), and several computation modules, all described in HDL using standard cell libraries alone. This is carried out to allow integration of the PWM modulator with the controller as a single ASIC solution and to provide technology-independent modulator architecture. The ON-time of each PWM output, *hs* and *ls*, is produced with the time resolution of a single delay-element's propagation time without any limitation on the corresponding duty cycle, making this module an attractive candidate for integration in high-frequency PFM-PWM controllers. Moreover, this modulator allows single-cycle convergence, which is a key enabler for both the voltage regulation task and the hybrid PFM-PWM start-up procedure described in Section III without realizing power-hungry high-frequency internal clock circuitry. The VFVDM has been validated on multiple programmable development platforms and fabrication processes and is ASIC-ready.

The VFVDM samples the ON-time commands ($hs_{in}[n]$ and $ls_{in}[n]$) at the beginning of each switching cycle and stores them in dedicated registers, as shown in Fig. 13. Each ON-time command is separated into coarse and fine segments, which indicate the number of internal clock cycles required to produce the coarse section of the PWM signals and the number of delay elements required for their respective fine-tuning addition. As shown in Fig. 13, the coarse and fine segments are the k-MSBs and p-LSBs of the input on-time commands, respectively. These inputs are internally processed to generate two sets of control signals: threshold values for the countercomparator schemes (*CMP Thresholds)* and selection commands for the multiplexer-array (s_1–s_4), as shown in Fig. 13. The resulting time-delayed replicas of the internal clock (p_1–p_4) are not confined to specific locations along the DL, which is the key enabler for the HR attributes of this module. The countercomparator schemes are fed with these signals at their respective clock ports and generate the set and reset signals to the VFVDM output stage (on_{TRG} and off_{TRG}) by comparing the counters' values with the *CMP Thresholds*. The multiplexer array pointers and time-delayed replicas of the internal clock are divided into two, $Mode_0$ and $Mode_1$, which are utilized in a cyclic manner to enable cycle-by-cycle update rate while eliminating miscalculations due to internal delays, as shown in the illustrative example of Fig. 14. Here, the pointers' movement along the DL is illustrated for a simple case of $p = 3$ and different fine-tuning segments for the two ON-time commands. The p_1- and p_3-fed countercomparator modules control the falling edge of the PWM output for $Mode_0$ and $Mode_1$, respectively while p_2 and p_4 are utilized in the same manner to control its rising-edge instance. As can be seen, the pointers' locations are modified on a cycle-by-cycle basis according to the following relations:

$$\begin{cases} S_1 = S_4 + hs_{in}[p-1:0] \\ S_2 = S_4 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \\ S_3 = S_2 + hs_{in}[p-1:0] \\ S_4 = S_2 + hs_{in}[p-1:0] + ls_{in}[p-1:0] \end{cases}. \quad (9)$$

Logical simulations carried out in QuestaSim for a 13-bit VFVDM are shown in Fig. 15. Here, the DL consists of 128 delay elements ($p = 7$) and the multiplexer array comprises four 128:1 multiplexer units. The inputs of the module, i.e., the ON-time commands, are specified at the top of the timing diagram along with the mode status ($Mode_0$ or $Mode_1$). According to (9), the fine-segment of the ON-time commands is derived and equals to 24 and 4 for the high-side and low-side drive signals, respectively, until the change in both duty cycle and switching frequency is enforced in the marked time location of t_c. As can be seen, the pointers are interchangeably updated every switching cycle according to (9) at the falling edge of the *hs* signal, marked as t_u instances in Fig. 15. To best showcase the capabilities of this module, both ON times are abruptly changed from 13'd664 and 13'd644 to 13'd5664 and 13'd1644. As can be seen, the resultant PWM signals nor the internal control signals suffer from noncontinuities and single-cycle convergence is achieved.

In this modulator implementation, clock jitter is considered a delay variation in the DLs mechanisms, as detailed in [22], [63], and [64]. This is addressed in the physical design phase where meticulous design based on timing constraints has been carried out resulting in less than 10% of a single delay element error. Moreover, the VFVDM is designed with high symmetry to ensure equal paths from the ring oscillator and the multiplexer array which significantly reduces jitter. Furthermore, the DEs' locations are fixed and confined to a compact region to reduce variations in the propagation time due to PVT variations which may affect the resultant time-resolution attribute of the VFVDM. Such variations will affect the small-signal gain of the modulator, which is derived from the alteration of the drive signal as a result of a change in the LSB of the drive command, i.e., a single DE. It is common practice to consider a range for the modulator's gain when calculating the control coefficients, and therefore, PVT variations are not required to be completely eliminated but rather taken into consideration.

Linearity and monotonicity characteristics are necessary for accurate operation of DL-based structures which are achieved by following the design and implementation guidelines discussed in [63], [64], and [68]. If properly followed, PVT variations will not jeopardize the correctness of the modulator's operation since the linearity and monotonicity characteristics are inherently derived from the utilization of the DL's propagating signals (p_1–p_4 in Fig. 13) and not from the DEs' timing characteristics which may vary due to temperature or aging.

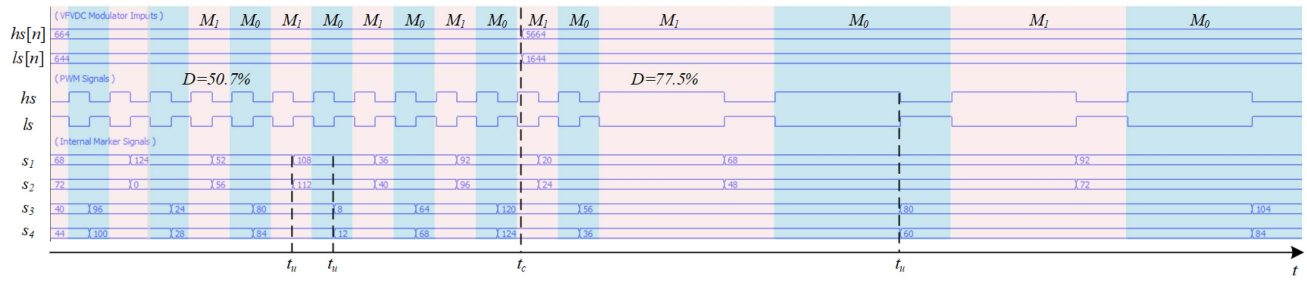

Fig. 15. QuestaSim logical Simulations of a 13-bit VFVDM.

V. Experimental Results

In order to validate the operation of the HB-LLC-based miniaturized power supply including the PFM-PWM digital controller, a 3–7 V input voltage prototype has been built and tested. The switching frequency range is 700 kHz–1.8 MHz to maintain regulation for the entire input voltage range and loading conditions as well as to enable the dual-variable start-up procedure. The input voltage range is derived from standard IoT device specifications and can be extended without any adjustments to the controller hardware or control law and the output voltage can be easily varied by modifying the digital reference values (ref_M and ref_L in Fig. 1). The power stage has been intentionally designed to withstand high voltage and current spikes to allow system exploration under extreme loading conditions and start-up scenarios. The digital controller has been entirely realized on Altera Cyclone V FPGA, including the HR VFVDM. The total gate counts to implement the controller sum to 2500, all standard cells. The transformer design is pot core based and the windings are 3:4 realized with a sectioned bobbin. The nominal values of the resonant capacitance C_r, resonant inductance L_r, and leakage inductance L_m are 0.68 μF, 37 nH, and 2 μH, respectively. Therefore, the resultant nominal resonance frequency of the *LLC* tank is 1 MHz, according to (2). The switch network, Q_1 and Q_2, is realized with si4168DY n-channel transistors (Vishay) and their respective drivers are TI's UCC2722, which exhibit robustness and flexibility suitable for the experimental prototype of this study. The experimental prototype incorporates an off-the-shelf AD9200 ADC (Analog Devices) with 10-bit resolution and a maximum sampling rate of 20MSPS. Its power consumption is 80 mW on a 3 V supply and below 5 mW in sleep mode. For an integrated realization of the controller, low-power monolithic ADCs can be incorporated to lower the power consumption of the sampling circuitry [22]. Shown in Fig. 16 are the transformer and the half-bridge transistors. The IoT load is mimicked in the experimental prototype by an adjustable switched load with variable power settings to allow the validation of steady-state operation as well as loading and unloading transients. This is realized by two independently driven low R_{DSon} power switches connected in series with resistive loads. Each test scenario comprises a set of time intervals and corresponding gating signals to the parallel loads' switches, thus dictating the load during startup as well as the magnitude and profile of the loading and unloading transients.

Fig. 16. HB-LLC converter power-stage transistors and transformer.

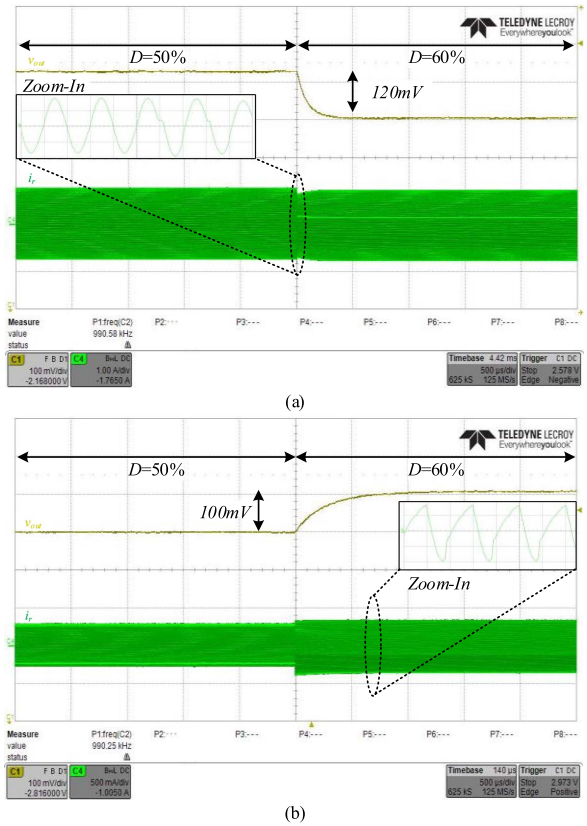

Fig. 17. Open-loop HB-LLC resonant converter load-dependent gain demonstration for $D_1 = 50\%$ and $D_2 = 60\%$. (a) $R_L < R_{crit}$. Output voltage (top-yellow) 100 mV/div and resonant inductor current 500 mA/div (bottom-green). (b) $R_L > R_{crit}$. Output voltage (top-yellow) 100 mV/div and resonant inductor current 500 mA/div (bottom-green).

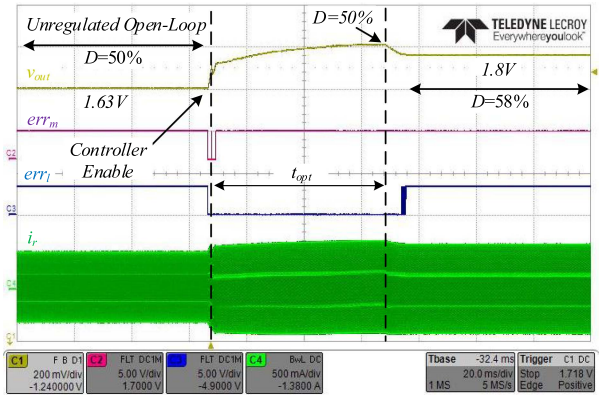

Fig. 18. Transition from open-loop to closed-loop conditions for an HB-LLC resonant converter. Output voltage (top-yellow) 200 mV/div, internal error signals (red-v_{err} and blue-v_{err_res}) and resonant inductor current 500 mA/div (bottom-green).

Fig. 17 shows a case of the open-loop transition from a symmetrical operation, i.e., 50%, to an asymmetrical operation with $D = 60\%$ for an HB-LLC resonant converter operating at 990 kHz with $R_L < R_{crit}$ [see Fig. 17(a)] and $R_L > R_{crit}$ [see Fig. 17(b)]. As can be seen, when $R_L < R_{crit}$, the output voltage decreases and the resonant current i_r, shown in the zoom-in of Fig. 17(a), indicates that power is delivered to the load during both sections of the switching cycle, in agreement with Fig. 3(a) and (b). However, for the case of $R_L > R_{crit}$, the change in duty cycle ratio results in an increased output voltage. Here, the bridge rectifier conducts current only during the ON-time of the low-side transistor Q_2 and the converter operates as an AHBFC, in agreement with Fig. 3(c).

Fig. 18 shows a case of open-loop to closed-loop transition for $V_{in} = 3.6$ V and $R_L = 10\ \Omega$. As can be seen, prior to the controller-enable command, the duty cycle is kept at 50% and the output voltage is approximately 1.63 V. During a closed-loop operation, the internal signals of err_m and err_l are high in case an MSB or LSB error exists, respectively. Once closed-loop operation is enabled, the switching frequency is adjusted to eliminate the MSB section of the error signals and the duty cycle is decreased until it reaches 50%, according to the optimization procedure discussed in Section III. Then, the duty cycle control loop modifies the duty cycle to eliminate the LSB section of the output voltage error resulting in asymmetrical operation with $D = 58\%$.

Fig. 19 demonstrates the importance of a dedicated start-up procedure for the HB-LLC resonant converter. Fig. 19(a) shows experimental waveforms for the hybrid PFM-PWM soft-start procedure with $V_{in} = 4.3$ V and $R_L = 10\,\Omega$. The initial switching frequency is 1.8× the resonant frequency, i.e., 1.8 MHz, the initial duty cycle is approximately zero and the sequence duration is set to 2.5 ms. As can be seen, the resonant inductor current i_r and resonant capacitor voltage v_{cr} do not exhibit any current or voltage spikes and the transition to closed-loop operation is executed in a seamless manner. Fig. 19(b) shows the current and voltage waveforms of the same HB-LLC resonant converter with closed-loop enabled operation upon turn-ON, without any soft-start procedure. As can be seen, the maximum resonant

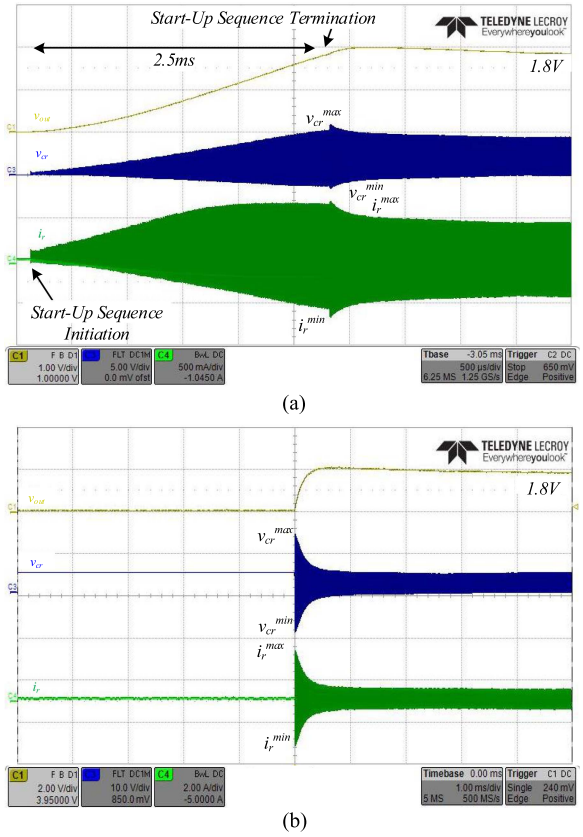

Fig. 19. HB-LLC resonant converter turn-ON. (a) With hybrid PFM-PWM start-up sequence. Output voltage 1 V/div (top-yellow), resonant capacitor voltage 5 V/div (middle-blue) and resonant inductor current 0.5 A/div (bottom-green). (b) Without soft-start procedure. Output voltage 2 V/div (top-yellow), resonant capacitor voltage 10 V/div (middle-blue) and resonant inductor current 2 A/div (bottom-green).

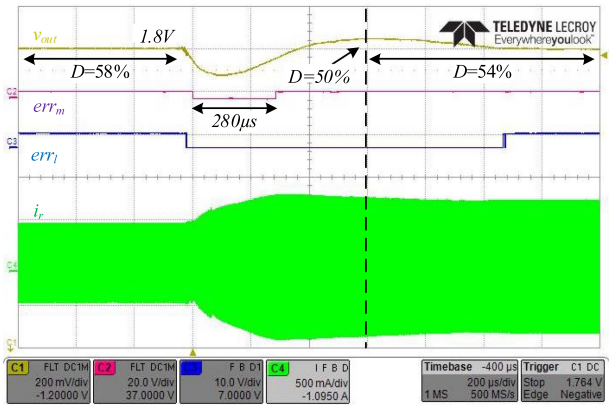

Fig. 20. HB-LLC resonant converter's response to a loading transient including optimization and fine-tuning phases. Output voltage (top-yellow) 200 mV/div, internal error signals (red-v_{err} and blue-v_{err_res}), and resonant inductor current 500 mA/div (bottom-green).

current as well as the resonant capacitor's voltage is significantly higher compared to those obtained when implementing the hybrid PFM-PWM start-up procedure, as shown in Fig. 19(a).

Fig. 20 shows a loading transient recovery for a 10–5 Ω resistive load step with input voltage of 4 V and initial switching

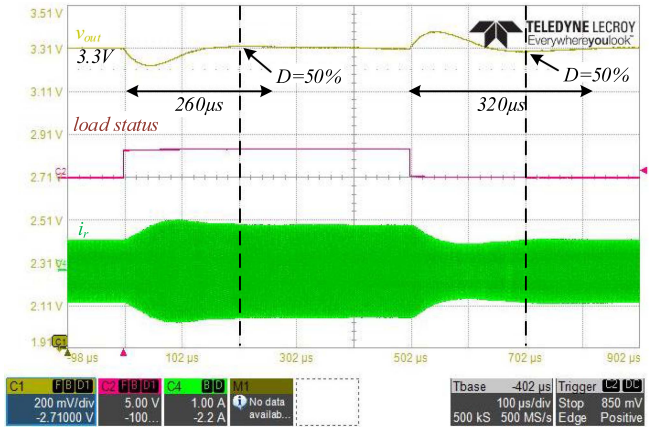

Fig. 21. HB-LLC resonant converter's response to consecutive loading and unloading transients including optimization and fine-tuning phases. Output voltage (top-yellow) 200 mV/div, loading status (red), and resonant inductor current 1 A/div (bottom-green).

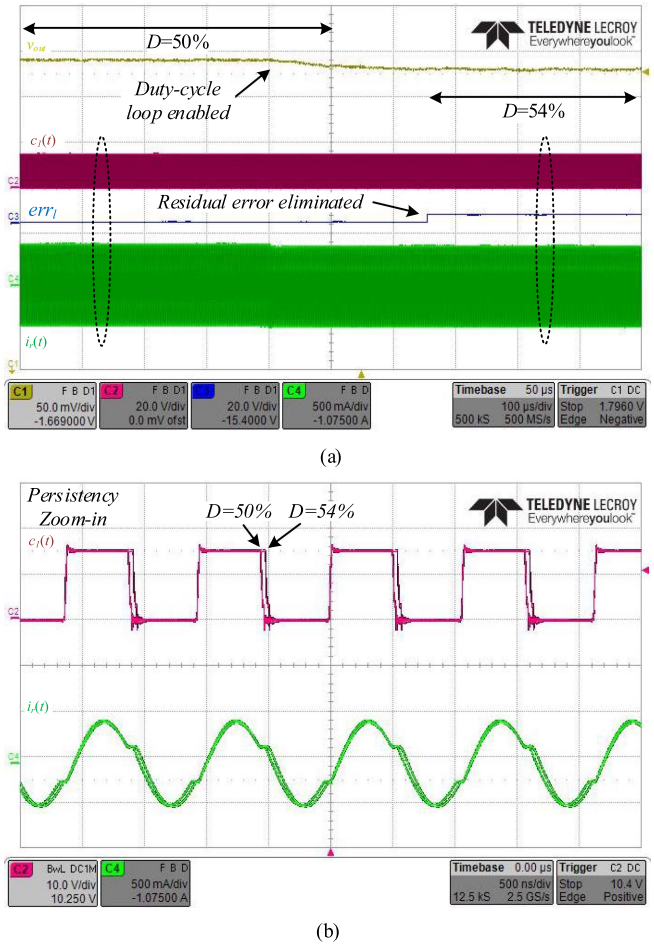

Fig. 22. (a) Residual error elimination event by the duty-cycle control loop. (b) Zoom-in measurements of the marked locations. Output voltage (top-yellow) 50 mV/div, high-side gate signal (red), residual error flag (blue), and resonant inductor current 500 mA/div (bottom-green).

frequency and duty-cycle values of 1 MHz and 58%, respectively. Upon transient detection, i.e., $v_{err}[n]\neq 0$, the frequency loop decreases the switching frequency until the MSB error is eliminated after 280 μs while the duty-cycle control loop initiates the optimization procedure. Once the duty cycle reaches 50%, the fine-tuning operation is carried out until the residual voltage error is eliminated as well. In this case, the final switching frequency is 790 kHz and the duty cycle is 54%. As can be seen, the experimental results of Fig. 20 largely agree with the simulation case study of Fig. 12 carried out with similar loading conditions and controller coefficients in terms of recovery duration and output voltage deviation. It should be noted that transient-oriented nonlinear or state-space-based control schemes can be incorporated into the controller to be activated under transient conditions. However, this will entail significant hardware additions such as high-speed comparators, DACs, and sensing circuitries [64], [65], [66].

Fig. 21 shows consecutive loading and unloading transient recovery patterns for the input voltage of 7 V and output voltage of 3.3 V. The load varies between 10 and 6.6 Ω as indicated by the load status signal in Fig. 21, which toggles between logic low and high values, respectively. The initial switching frequency prior to the loading event is 1.124 MHz and the duty cycle is 53%. Once $v_{err}[n]\neq 0$ is obtained, the frequency loop decreases the switching frequency to eliminate the MSB section of the error signal and initiates the optimization procedure, which results in a switching frequency of 1.035 MHz and a duty cycle of 52%. Similar patterns can be observed for the unloading transient event for which the controller adjusts the switching frequency and duty cycle to comply with the initial loading conditions. As can be seen, the transient recovery durations are 260 μs and 320 μs for the loading and unloading cases, respectively.

Fig. 22 shows a scenario in which the frequency loop has eliminated the MSB section of the error v_{err} but the LSB section v_{err_res} is nonzero as a result of the duty-cycle loop being intentionally disabled. Prior to the duty-cycle loop enable command, the switching frequency is 940 kHz and the duty cycle is 50%, i.e., symmetrical gating signals are generated. Once the duty-cycle loop is enabled, its respective compensator modifies the duty-ratio settings until the residual error is eliminated, marked by the rising edge of the err_l signal in Fig. 22(a). As can be seen, increasing the duty cycle results in a decrease in the output voltage, in agreement with the discussion in Section II, until it reaches its zero-error bin and the duty-cycle ratio is settled at 54%. The zoom-in of Fig. 22(b) comprises two separate switching states shown on the same scale and aligned to the rising edge of the drive signal: before and after the duty-cycle loop enable command. It allows a visual representation of the resonant current under two relatively close duty-cycle settings with the same switching frequency alongside the clear effect on the output voltage shown in Fig. 22(a). This figure highlights the ability of each internal loop to modify a given switching attribute and to eliminate its assigned section of the error. It should be noted that capturing a transition between the two switching states of Fig. 22(b) is not feasible since it occurs over a significant number of switching cycles. For that same reason, Figs. 20 and 21 in which both the switching frequency and the duty cycle are modified simultaneously showcase complete response to load changes.

Fig. 23 shows the closed-loop steady-state operation at the megahertz range of two HB-LLC resonant converter-based SMPS with an input voltage of 4 V and a resistive load of 10 Ω. In Fig. 23(a) and (b), a conventional PFM digital controller is utilized to regulate the output voltage. Since the drive capabilities are derived from the modulator's architecture and its respective internal clock frequency (clk_{base} in Fig. 13), which is limited due to the power requirements of the target applications, the DPWM module operates with comparable clock resources. Here, the counter-based modulator operates with a 50 MHz clock, while the internal clock frequency of the HR-VFVDM is considerably lower and equals approximately 20 MHz, which highlights the merits of the new modulator architecture. As discussed in the case study of Section III, the single-variable-based controller interchangeably modifies the switching frequency (1.08 and 1.04 MHz), which results in a nonzero steady-state error and significant output voltage ripple. This is due to a reduced number of gain regions at high switching frequency, as discussed in Section II. The zoom-in of Fig. 23(b) shows a transition from 1.08 MHz operation to 1.04 MHz and sinusoidal resonant current as a result of the symmetrical drive signals. Shown in Fig. 23(c) and (d) are the resultant waveforms of a PFM-PWM digitally controlled SMPS. Here, two compensation units are employed to maintain the output voltage within its zero-error bin, alongside the HR-VFVDM. As can be seen, the steady-state error is completely eliminated and the converter is operated with constant switching frequency, which significantly reduces output voltage ripple and resonant current aberrations. Here, the converter operates with above 50% duty-cycle ratio set by the controller following its optimization procedure, as discussed in Section III.

Shown in Fig. 24 are experimentally extracted gain curves of the proposed hybrid PFM-PWM control scheme as well as of a single variable control scheme for the same power-stage and loading conditions. Here, the voltage gain is extracted for various switching frequencies and duty-cycle values to demonstrate the extended regulation capabilities. As can be seen, for a symmetrical modulation scheme the output voltage gain is restricted to a singular value per switching frequency, while for the asymmetrical scheme, the added control variable results in continuous voltage gain curves, limited only by the resolution of the DPWM. Marked in dashed lines is the graphical illustration of the controller's optimization procedure discussed in Section III.

Fig. 25 shows efficiency curves as a function of the output power for an input voltage of 5 V and a regulated output voltage of 1.8 V. The efficiency analysis is carried out with and without the optimization procedure based on ten measurements taken for each case, as marked inn Fig. 25. While in both cases the output voltage is well positioned within its zero-error bin, the overall efficiency is boosted for the full range of loading conditions due to the optimization procedure described in Section III, keeping the efficiency for substantial output power (>500 mW) above 55%. Compared to the best-in-class commercial solution [21] and realizations published in the literature [25], [26], the experimental prototype achieves comparable efficiencies with improved input voltage and output power ranges. It should be noted that a

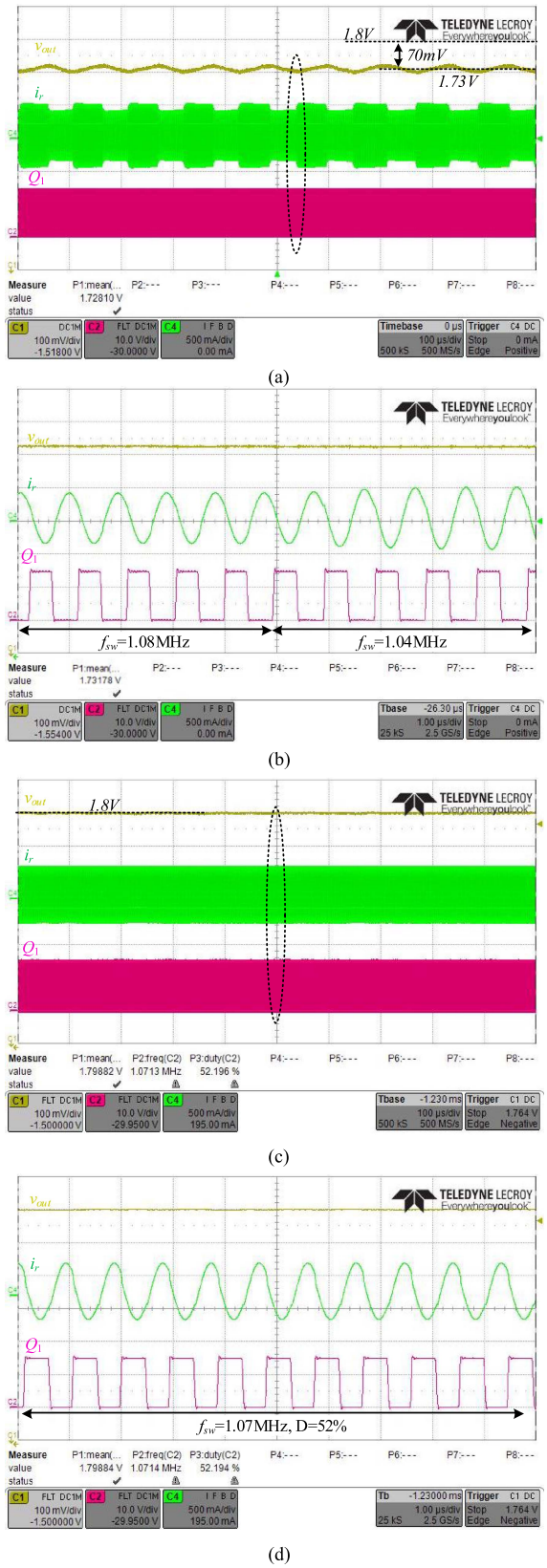

Fig. 23. Closed-loop steady-state operation at the megahertz range with $V_{in} = 4$ V, $V_{out} = 1.8$ V, and $R_L = 10$ Ω. (a)–(b) Conventional frequency digital controller with $D = 50\%$. (c)–(d) Hybrid PFM-PWM digital controller with $D > 50\%$. Output voltage (top-yellow) 100 mV/div, resonant inductor current 500 mA/div (middle-green), and high-side gate signal (bottom-red).

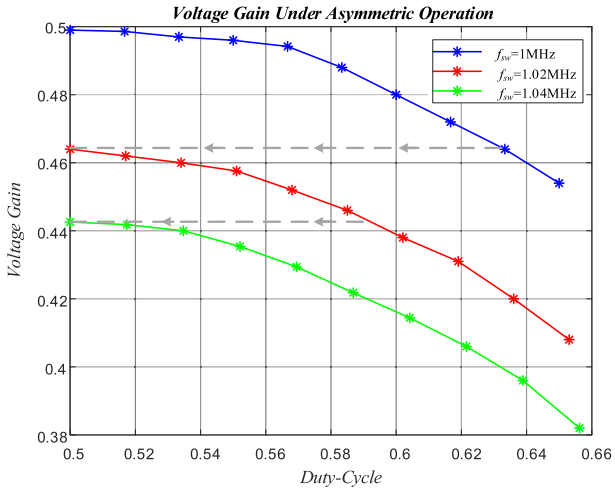

Fig. 24. Exemplary experimentally extracted gain curves and optimization procedure illustration (dashed - gray) for various switching frequencies and duty-cycle ratios in open-loop conditions with $R_L < R_{crit}$.

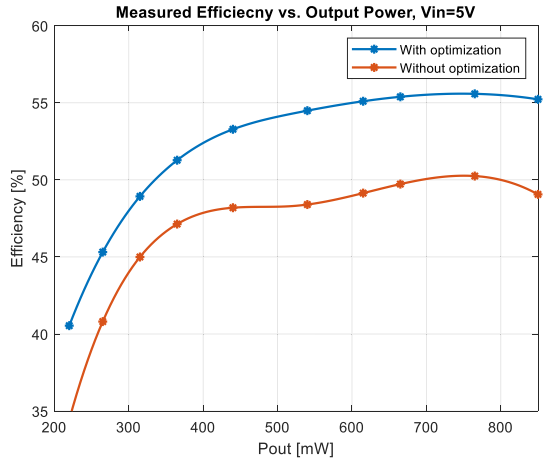

Fig. 25. Efficiency curves with and without optimization procedure.

dedicated PCB rather than an experimental one and components that are not expected to operate under extreme conditions will result in higher efficiency and smaller overall volume.

VI. Conclusion

A miniaturized power supply architecture based on an HB-LLC resonant converter and an all-digital hybrid PFM-PWM controller has been presented in this article. The controller adjusts the switching frequency and the duty ratio of the converter to compensate for any change in the operating conditions, i.e., load status or input voltage. The realized control law is based on a conventional single-loop control scheme with lean hardware requirements and computational resources and includes a hybrid PFM-PWM start-up routine that significantly reduces the stress on the passive components. In addition, an asymmetrical operation of an HB-LLC resonant converter is discussed and dedicated control sequences are presented to maintain a tight output voltage regulation for regions where the converter's gain is nonmonotonic with respect to the duty cycle command.

Experimental results of a 3–7 V HB-LLC resonant converter are provided. A well-regulated output voltage is achieved for a wide range of operating conditions with significantly reduced frequency-resolution requirements due to the controller's ability to produce asymmetrical drive signals. Finally, a new HR variable-frequency variable-duty-cycle modulator has been presented that produces asymmetrical drive signals with time resolution of a single delay element using a single shared DL structure.

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