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אוניברסיטת בן-גוריון בנגב

מדור - בחינות

מס' נבחן: ____

תאריך הבחינה: 2/7/91 13

שם המורה: פרופ' שמואל בן-יעקב

מבחן ב: ממירי DC-DC ממותגים

מס' הקורס: 361.1.4561

מיועד לתלמידי: הנדסת חשמל

שנה תשנ"א סמ' ב' מועד א'

משך הבחינה: 3 שעות

חומר עזר: כל חומר כתוב מותר, כל מחשב מותר, אין להעביר חומר ו/או מחשבים בין הנבחנים

יש לענות על 2 שאלות.
השאלות שוות בערכן, שאלה שלישית לא תבדק

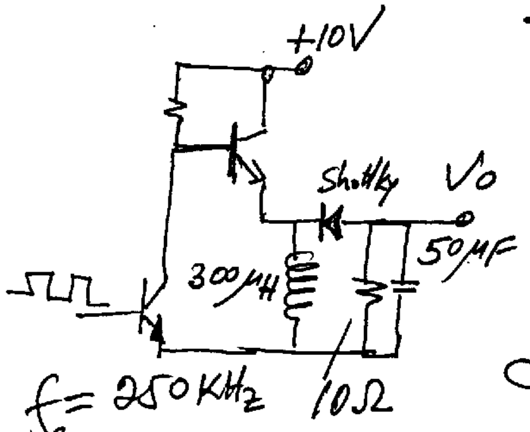
שאלה מס 1

נתון מבנה עקרוני של ספק/ממיר

$D = 0.5$

התנגדות אומית של הסליל 0.01Ω

מניחים מתגים אידיאליים



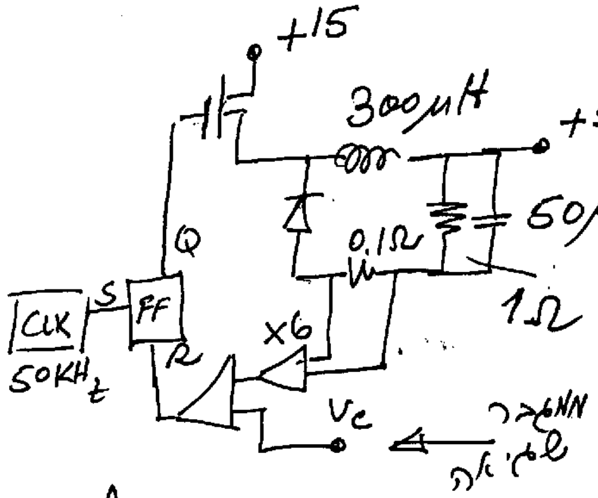
$f_s = 250KHz$

(40%) 1.1 חשב מתח מוצא DC וצורת הזרם בסליל (שרטט)

(60%) 1.2 בעזרת מודל הסליל המתמתג חשב ושרטט $\frac{\hat{v}_o}{\hat{d}}(f)$

שאלה מס 2

נתון מבנה עקרוני של מייצב בשיטת Current Mode



(50%) 2.1 חשב V_c במצב היציב (בחוג סגור)

(50%) 2.2 חזור על 2.1 אם $R_L = 100\,\Omega$

שאלה מס 3

נתון $V_{in} = 10V$, תכנן בעזרת 3524 ספק ממותג מוצא 5V בזרם מקסימלי 100mA. הזרם המינימלי 30mA Continuous. הגלי מוצא 50mV. התכנון יכלול ערכי סליל, קבל, נגדים, תדר מיתוג (50KHz) ורשת הפיצוי במשוב. יש לעמוד בקביעות מתח מוצא. דפי נתונים מצורפים.

National Semiconductor

LM1524D/LM2524D/LM3524D
Regulating Pulse Width Modulator

General Description

The LM1524D family is an improved version of the industry standard LM1524. It has improved specifications and additional features yet is pin for pin compatible with existing 1524 families. New features reduce the need for additional external circuitry often required in the original version.

The LM1524D has a ±1% precision 5V reference. The current carrying capability of the output drive transistors has been raised to 200 mA while reducing V_{CEsat} and increasing V_{CE} breakdown to 60V. The common mode voltage range of the error-amp has been raised to 5.5V to eliminate the need for a resistive divider from the 5V reference.

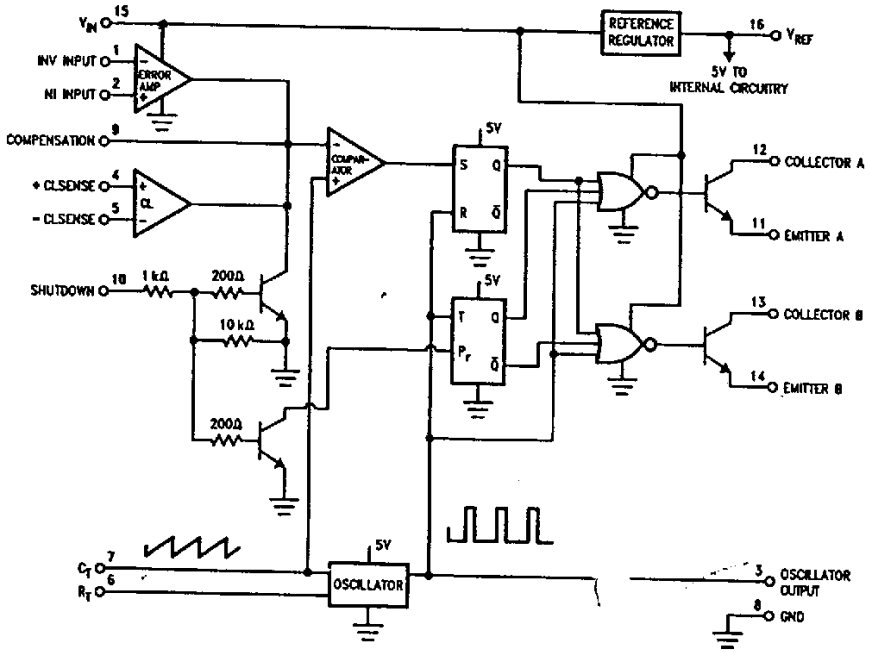
In the LM1524D the circuit bias line has been isolated from the shut-down pin. This prevents the oscillator pulse amplitude and frequency from being disturbed by shut-down. Also at high frequencies (≈300 kHz) the max. duty cycle per output has been improved to 44% compared to 35% max. duty cycle in other 1524s.

In addition, the LM1524D can now be synchronized externally, through pin 3. Also a latch has been added to insure one pulse per period even in noisy environments. The LM1524D includes double pulse suppression logic that insures when a shut-down condition is removed the state of the T-flip-flop will change only after the first clock pulse has arrived. This feature prevents the same output from being pulsed twice in a row, thus reducing the possibility of core saturation in push-pull designs.

Features

- Fully interchangeable with standard LM1524 family
- ±1% precision 5V reference with thermal shut-down
- Output current to 200 mA DC
- 60V output capability
- Wide common mode input range for error-amp
- One pulse per period (noise suppression)
- Improved max. duty cycle at high frequencies
- Double pulse suppression
- Synchronize through pin 3

Block Diagram



Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	40V
Collector Supply Voltage	
(LM1524D)	60V
(LM2524D)	55V
(LM3524D)	40V
Output Current DC (each)	200 mA
Oscillator Charging Current (Pin 7)	5 mA
Internal Power Dissipation	1W
Operating Junction Temperature Range J Package (Note 2)	
LM1524D	−55°C to +150°C
LM2524D	−40°C to +150°C
Operating Maximum Junction Temperature N Package (Note 2)	
LM2524D	−40°C to +125°C
LM3524D	0°C to +125°C
Maximum Junction Temperature	150°
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec.) J Pkg.	300°C
Lead Temperature (Soldering 4 sec.) N Pkg.	260°C

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	LM1524D Typ	LM1524D Tested Limit (Note 3)	LM1524D Design Limit (Note 4)	LM2524D Typ	LM2524D Tested Limit (Note 3)	LM2524D Design Limit (Note 4)	LM3524D Typ	LM3524D Tested Limit (Note 3)	LM3524D Design Limit (Note 4)	Units
REFERENCE SECTION												
V_{REF}	Output Voltage		5	4.95 **4.90**		5	4.85	**4.80**	5	4.75		V_{Min}
				5.05 **5.10**			5.15	**5.20**		5.25		V_{Max}
V_{RLine}	Line Regulation	V_{IN} = 8V to 40V	10	**20**		10	15	**30**	10	25	50	mV_{Max}
V_{RLoad}	Load Regulation	I_L = 0 mA to 20 mA	5	**15**		10	15	**25**	10	25	50	mV_{Max}
$\frac{\Delta V_{IN}}{\Delta V_{REF}}$	Ripple Rejection	f = 120 Hz	66			66			66			dB
I_{OS}	Short Circuit Current	V_{REF} = 0	50	25 150		50	25 180		50	25 200		mA Min mA Max
N_O	Output Noise	10 Hz ≤ f ≤ 10 kHz	40		100	40		100	40		100	μV_{rms} Max
	Long Term Stability	T_A = 125°C	20			20			20			mV/kHr
OSCILLATOR SECTION												
f_{OSC}	Max. Freq.	R_T = 1k, C_T = 0.001 µF (Note 7)	550		500	550		500	350			kHz_{Min}
f_{OSC}	Initial Accuracy	R_T = 5.6k, C_T = 0.01 µF (Note 7)	20	18.5 21.5		20	17.5 22.5		20	17.5 22.5		kHz_{Min} kHz_{Max}
		R_T = 2.7k, C_T = 0.01 µF (Note 7)	38	36 40		38	34 42		38	30 46		kHz_{Min} kHz_{Max}
Δf_{OSC}	Freq. Change with V_{IN}	V_{IN} = 8 to 40V	0.5	1		0.5	1		0.5	1.0		$\%_{Max}$
Δf_{OSC}	Freq. Change with Temp.	T_A = −55°C to +125°C at 20 kHz R_T = 5.6k, C_T = 0.01 µF	5			5			5			%
V_{OSC}	Output Amplitude (Pin 3) (Note f	R_T = 5.6k, C_T = 0.01 µF	3	2.4		3	2.4		3	2.4		V_{Min}
t_{PW}	Output Pulse Width (Pin 3)	R_T = 5.6k, C_T = 0.01 µF	0.5	1.5		0.5	1.5		0.5	1.5		μs_{Max}

Typical Applications (Continued)

From the relation $V_L = L\frac{di}{dt}$, $\Delta i_L = \frac{V_L T}{L1}$

$$\Delta i_L^+ = \frac{(V_{IN} - V_O)\, t_{ON}}{L1}, \quad \Delta i_L^- = \frac{V_O\, t_{OFF}}{L1}$$

Neglecting V_{SAT}, V_D, and setting $\Delta i_L^+ = \Delta i_L^-$:

$$\boxed{V_O = V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right) = V_{IN}\left(\frac{t_{ON}}{T}\right)}$$

where T = Total Period

The above shows the relation between V_{IN}, V_O and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)} V_{IN} = (I_{O(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right) V_{IN}$$

$$P_O = I_O V_O$$

The efficiency, η, of the circuit is:

$$\eta MAX = \frac{P_O}{P_{IN}} = \frac{I_O V_O}{I_O \frac{(t_{ON})}{T} V_{IN} + \frac{(V_{SAT}\, t_{ON} + V_{D1} t_{OFF})}{T} I_O}$$

$$= \boxed{\frac{V_O}{V_O + 1}} \text{ for } V_{SAT} = V_{D1} = 1V.$$

ηMAX will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} = \frac{(\Delta i_L^+) \times L1}{(V_{IN} - V_O)}, \quad t_{OFF} = \frac{(\Delta i_L^-) \times L1}{V_O}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta i_L^+) \times L1}{(V_{IN} - V_O)} + \frac{(\Delta i_L^-) \times L1}{V_O}$$

$$= \frac{0.4 I_O L1}{(V_{IN} - V_O)} + \frac{0.4 I_O L1}{V_O}$$

Since $\Delta i_L^+ = \Delta i_L^- = 0.4 I_O$

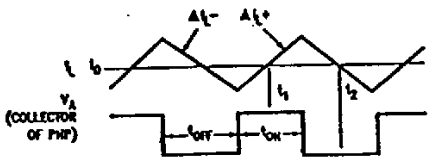


FIGURE 14

Solving the above for L1

$$\boxed{L1 = \frac{2.5\, V_O (V_{IN} - V_O)}{I_O V_{IN} f}}$$

where: L1 is in Henrys

f is switching frequency in Hz

Also, see LM1578 data sheet for graphical methods of inductor selection.

CALCULATING OUTPUT FILTER CAPACITOR C_O:

Figure 14 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times. This current must flow to the load and C_O. C_O's current will then be the difference between i_L and I_O.

$$i_{C_O} = i_L - I_O$$

From *Figure 14* it can be seen that current will be flowing into C_O for the second half of t_{ON} through the first half of t_{OFF}, or a time, $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta i_L/4$. The resulting ΔV_O or ΔV_O is described by:

$$\Delta V_{O\,p\text{-}p} = \frac{1}{C} \times \frac{\Delta i_L}{4} \times \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta i_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

Since $\Delta i_L = \frac{V_O(T - t_{ON})}{L1}$ and $t_{ON} = \frac{V_O T}{V_{IN}}$

$$\Delta V_{O\,p\text{-}p} = \frac{V_O\left(T - \frac{V_O T}{V_{IN}}\right)}{4C\,L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_O) V_O T^2}{8 V_{IN} C_O L1} \text{ or}$$

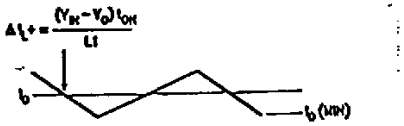
$$\boxed{C_O = \frac{(V_{IN} - V_O) V_O T^2}{8 \Delta V_O V_{IN} L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$

ΔV_O is p-p output ripple

For best regulation, the inductor's current cannot be allowed to fall to zero. Some minimum load current I_O, and thus inductor current, is required as shown below:

$$I_{O(MIN)} = \frac{(V_{IN} - V_O)\, t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_O) V_O}{2 f V_{IN} L1}}$$



Typical Applications (Continued)

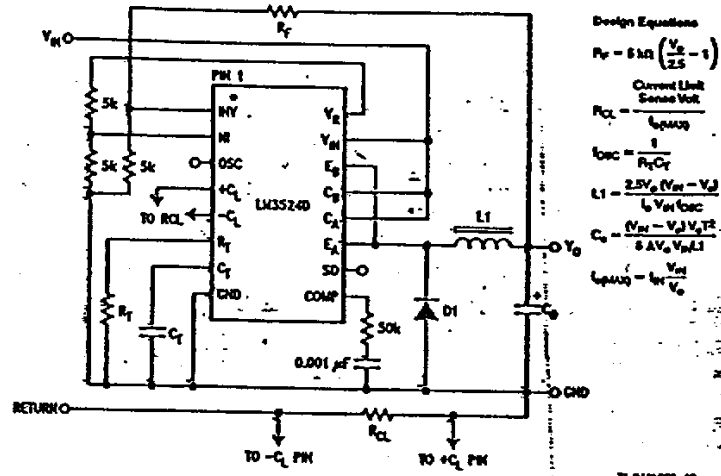


FIGURE 9. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

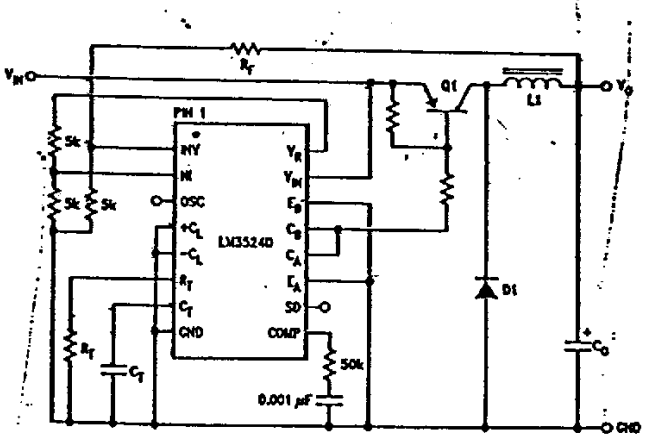


FIGURE 10. Positive Regulator, Step-Down Boosted Current Configuration

Functional Description (Continued)

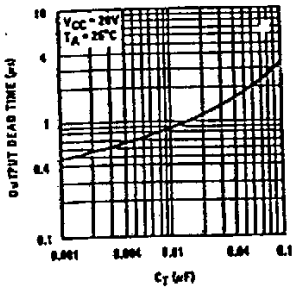


FIGURE 3

ERROR AMPLIFIER

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 86 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in *Figure 4*.

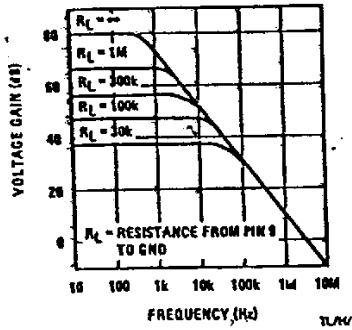


FIGURE 4

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \approx 5$ MΩ). For this reason a DC voltage can be applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in *Figure 5*.

The duty cycle is calculated as the percentage ratio of each output's ON-time to the oscillator period. Paralleling the outputs doubles the observed duty cycle.

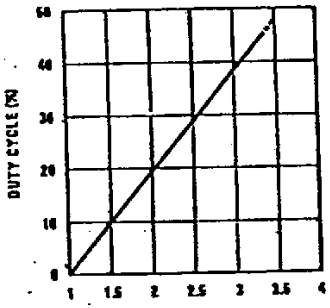


FIGURE 5

The amplifier's inputs have a common-mode input range of 1.5V–5.5V. The on board regulator is useful for biasing the inputs to within this range.

CURRENT LIMITING

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$ sense terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

OUTPUT STAGES

The outputs of the LM1524D are NPN transistors, capable of a maximum current of 200 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in *Figure 6*.

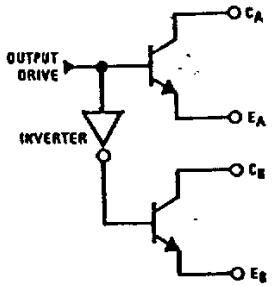
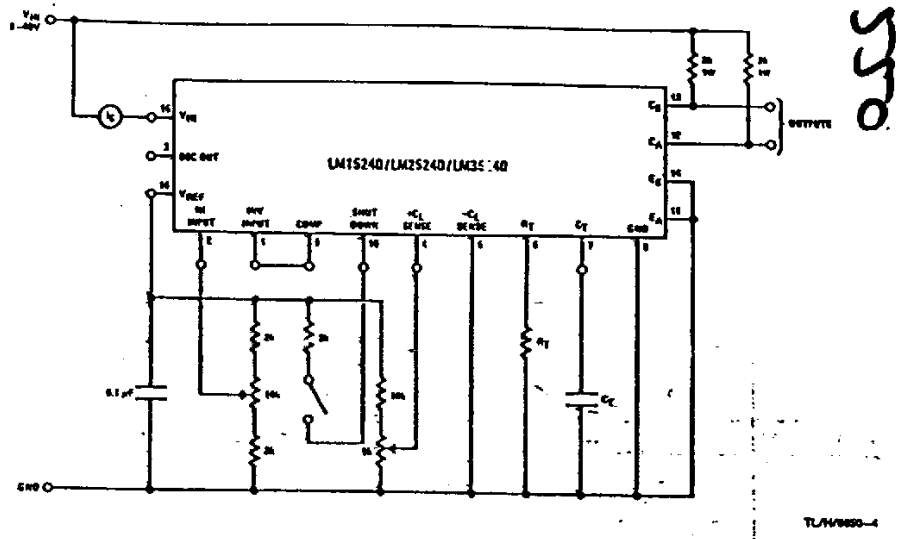


FIGURE 6

Test Circuit

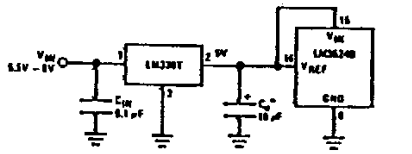


Functional Description

INTERNAL VOLTAGE REGULATOR

The LM1524D has an on-chip 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6V–8V are to be used, a pre-regulator, as shown in *Figure 1*, must be added.



*Minimum C_O of 10 μF required for stability.

FIGURE 1

OSCILLATOR

The LM1524D provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown is *Figure 2*. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in *Figure 3*. The recommended values of are 1.6 kΩ to 100 kΩ, and for C_T, 0.001 μF to 0.1 μ.

If two or more LM1524D's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's (together) to a single C_T, and leave all pin 6's open except one which is connected to a single R_T. This method works well unless the LM1524D's are more than 6" apart.

A second synchronization method is appropriate for any circuit layout. One LM1524D, designated as master, must have its R_TC_T set for the correct period. The other slave LM1524D(s) should each have an R_TC_T set for a 10% longer period. All pin 3's must then be interconnected to allow the master to properly reset the slave units.

The oscillator may be synchronized to an external clock source by setting the internal free-running oscillator frequency 10% slower than the external clock and driving pin 3 with a pulse train (approx. 3V) from the clock. Pulse width should be greater than 50 ns to insure full synchronization.

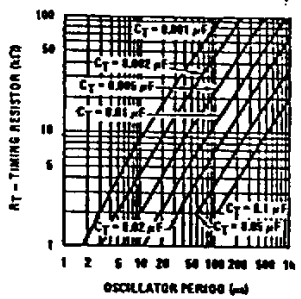


FIGURE 2