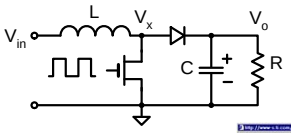
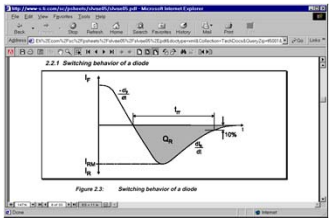
Parasitic effects
Snubbers and clamps

- Turn on and turn off effects
  - Turn on - diode reverse recovery
  - Turn off – dI/dT effect on transistor
  - Turn off – diode forward recovery
  - Mosfet gating
- Transistor protection - Clamp
  - Flyback leakage problem
  - Clamp configuration
  - Component selection
- Diode protection – Snubber
- Switching snubbers and lossless (ZVS) snubber

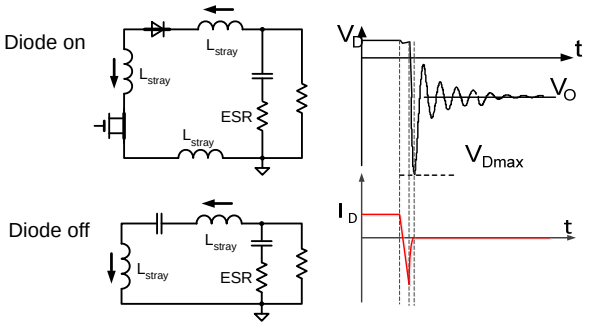
Diodes reverse recovery



Diode on – bidirectional current flow

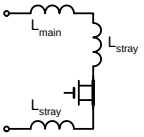


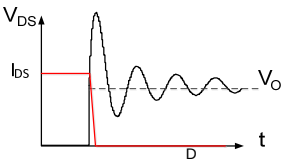
Diodes recovery – spike and oscillations



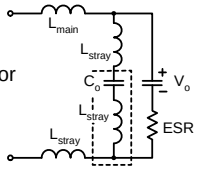
Transistor turn off - parasitics

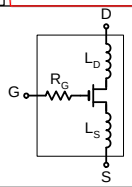
Transistor on



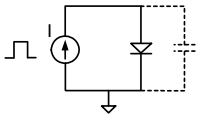


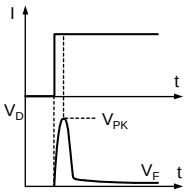
Transistor off



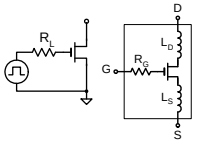


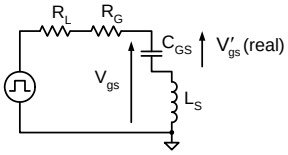
Transistor turn off – diode forward recovery

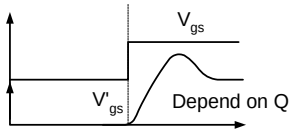




Mosfef gating

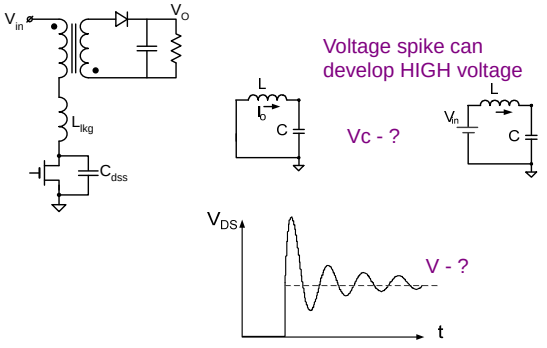






$$Q = \frac{\sqrt{\frac{L_S}{C_{gs}}}}{R_L + R_G}$$

Flyback leakage problem

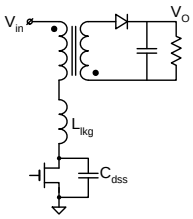


Voltage spike can develop HIGH voltage

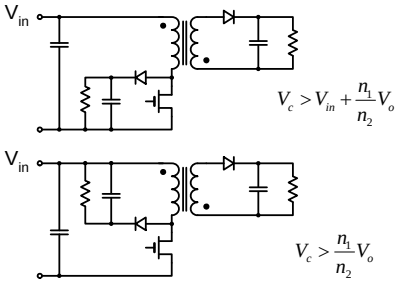
Clamp

Zener diode

D – C - R



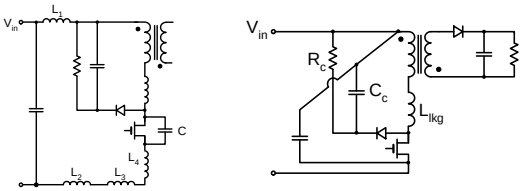
Clamp configurations



$$V_c > V_{in} + \frac{n_1}{n_2} V_o$$

$$V_c > \frac{n_1}{n_2} V_o$$

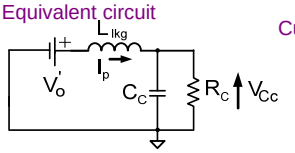
Parasitic inductance and physical placement



Connection of the clamp/snubber should be **directly** on the element

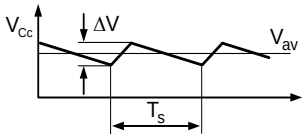
Clamp design

Equivalent circuit

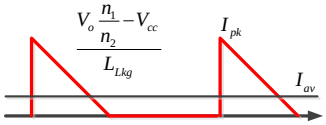


Current waveform

Assuming small ripple on the clamp capacitor (will be designed that way)



Calculation of clamp components



$$I_{av} = \frac{I_{pk} \cdot t_p}{2} \cdot f_s$$

$$I_{av} R_c > V_{cc\_av}$$

$$C_c R_c > T_s$$

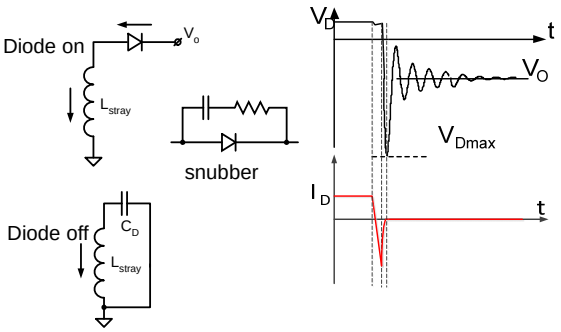
$$\frac{dI_p}{dt_p} = \frac{V_o \frac{n_1}{n_2} - V_{cc}}{L_{Lkg}}$$

Design procedure

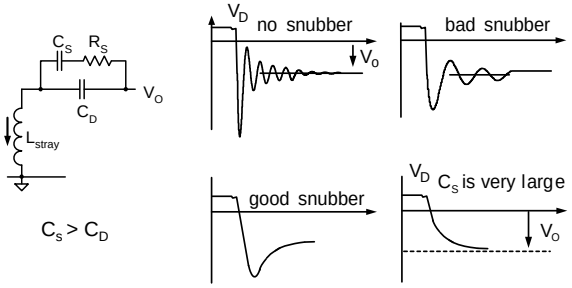
1. Select $V_{Cc\,av}$ > Vo'
2. Calculate $I_{p\,av}$
3. Select $R_c = \frac{V_{cc\_av}}{I_{av}}$
4. Select C_c $T > T_s$
5. Adjust values

$$I_{av} = \frac{I_{pk} \cdot t_p}{2} \cdot f_s$$

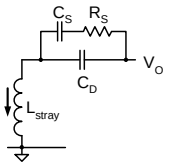
Diode turn off snubber



Diode turn off snubber



Snubber design



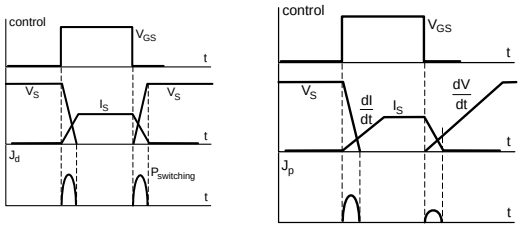
Required values
Ipk (reverse current)
Stary inductance

$$\frac{L_{stray} I_{pk}^{\ 2}}{2} = \frac{C_s \left(V_o + \Delta V\right)^2}{2}$$

Resistor for damping $C_s R_s < T_s$
Cs needs to discharge

Use simulation to optimize the snubber

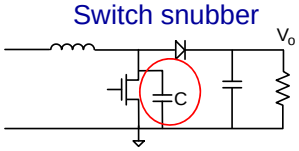
Switching snubber



The objective: avoid overlap of current and voltage

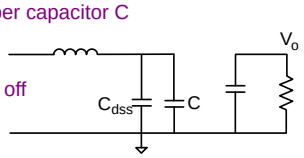
Slow the rise of either current or voltage

Switch snubber



dV/dT (at turn off) can be slow down by adding external snubber capacitor C

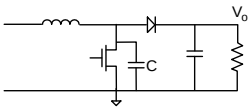
Turn off



$$\frac{dV}{dt} = \frac{I}{C + C_{dss}}$$

Switch snubber

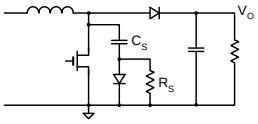
Problem at turn on



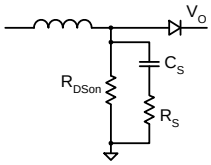
$$E_C = \frac{CV_O^2}{2} \qquad P_d = \frac{CV_O^2}{2} \cdot f_s$$

Dissipated through the transistor

Solution



Switch snubber design



If $R_{ds\ on} < R_s$ most energy will be lost to $R_s \rightarrow$ Heat

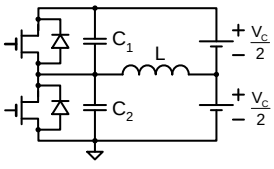
Selection of $C_s \rightarrow$

Selection of $R_s \rightarrow$ to ensure reset

$$T = \frac{1}{R_s C_s} << t_{on} \qquad t_{on} \approx 4R_s C_s$$

Question: how VDS will look if Cs is not fully discharged?

Lossless (ZVS) snubber



C_1, C_2 of transistor plus external