



Control of switch-mode converters



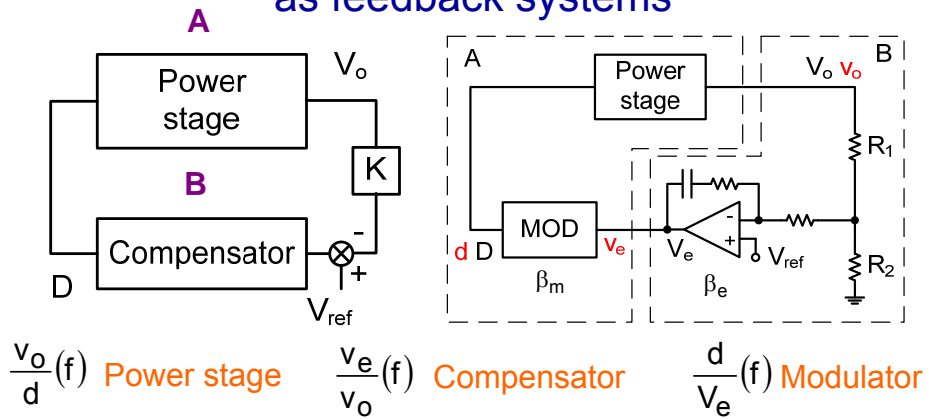
Control objectives

Produce control command to

- Regulate the output voltage
- Obtain zero or small steady-state (DC) error
- Quick response to reference changes
- Fast recovery
- Immunity to input and load changes
- Reasonable overshoot



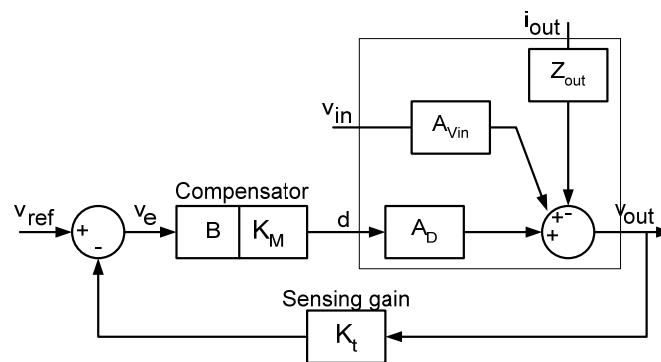
Switch-mode converters as feedback systems



- Power stage is a Switching System (non-linear)
- Compensator is an analog or digital controller
- Linear control theory based design → small signal response

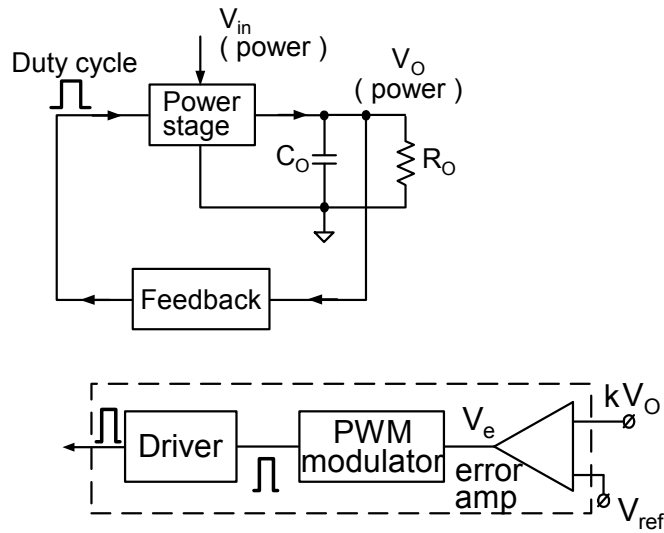


Control of PWM converters disturbances in voltage mode

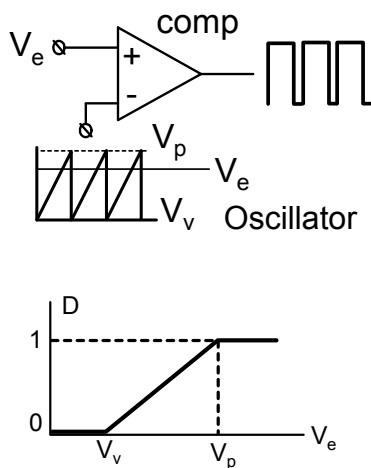




Voltage regulation



PWM modulator



$$V_t = \frac{(V_p - V_v)t}{T_s} + V_v$$

$$V_t = V_e = \frac{(V_p - V_v)t_{on}}{T_s} + V_v$$

$$\frac{t_{on}}{T_s} = D_{on} = \frac{(V_e - V_v)}{V_p - V_v}$$

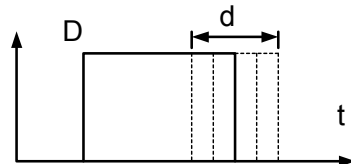
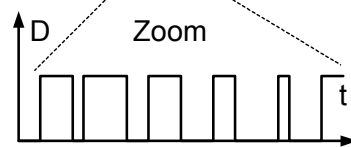
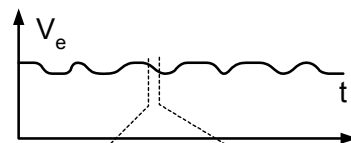
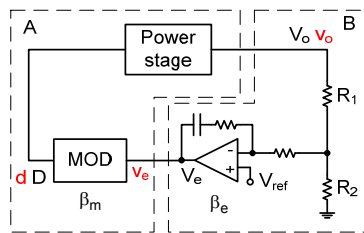
Practical $D_{on\ max} \approx 0.8 \div 0.9$



Sawtooth generator

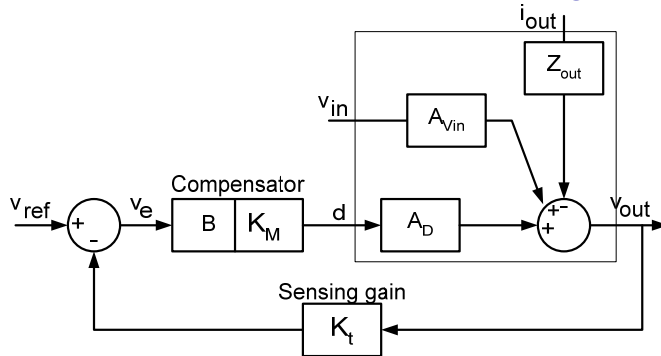


Transfer functions





Control of PWM converters disturbances in voltage mode



$$A_d = \left. \frac{v_{out}}{d} \right|_{v_{in}=0, i_{out}=0}$$

$$A_{vin} = \left. \frac{v_{out}}{v_{in}} \right|_{d=0, i_{out}=0}$$

$$Z_{out} = \left. \frac{v_{out}}{i_{out}} \right|_{v_{in}=0, d=0}$$

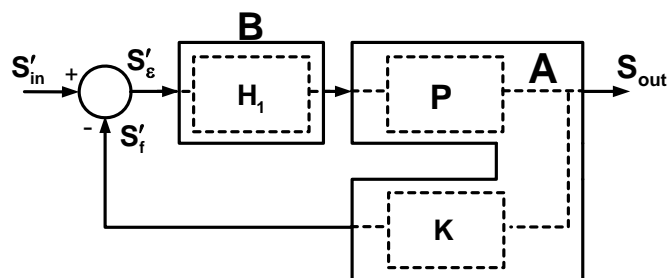
$$v_{out} = dA_d + v_{in}A_{vin} - i_{out}Z_{out}$$

$$v_{out} = v_{ref} \frac{1}{K_t} \frac{LG}{1+LG} + v_{in} \frac{A_{vin}}{1+LG} - i_{out} \frac{Z_{out}}{1+LG}$$

$$LG = K_t K_M B A_d$$



Dynamics of feedback systems Block diagram division



$$LG(f) = AB$$

A – known (power stage + divider)

B – unknown (have to be designed)



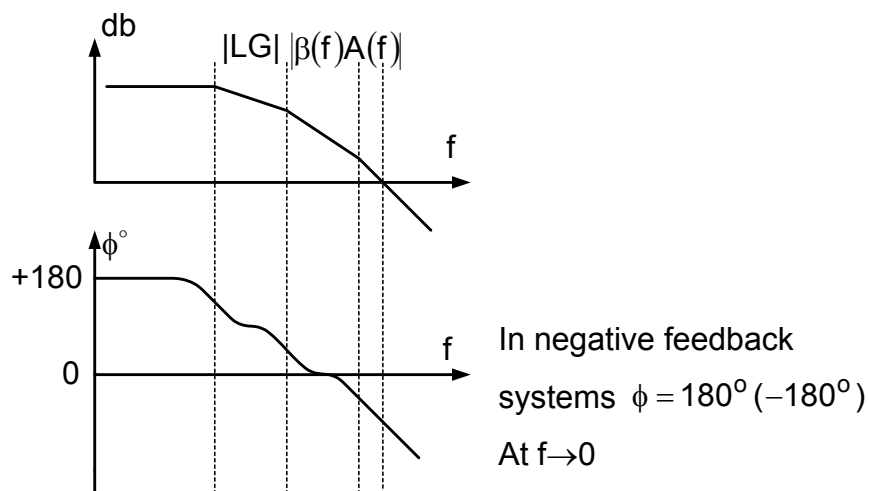
LoopGain test Nyquist Criterion

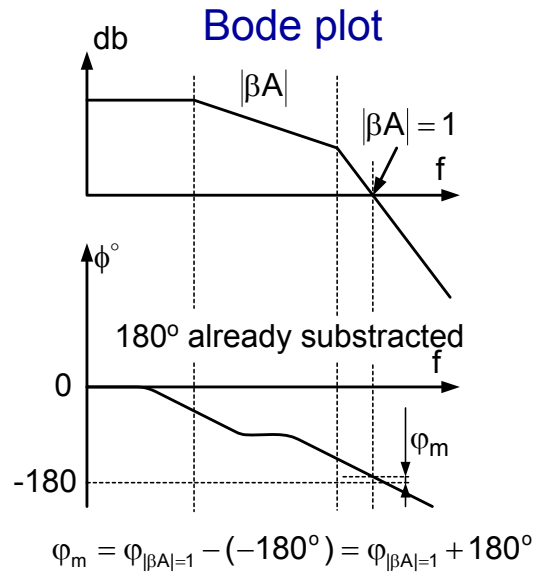
$$A_{CL} = \frac{A(s)}{1+LG(s)}$$

- The system is unstable if $\{1+LG(s)\}$ has roots in the right half of the complex plane.
- Nyquist criterion is a test for location of $\{1+LG(s)\}$ roots.
- Nyquist criterion is normally translated into the Bode plane (frequency domain)

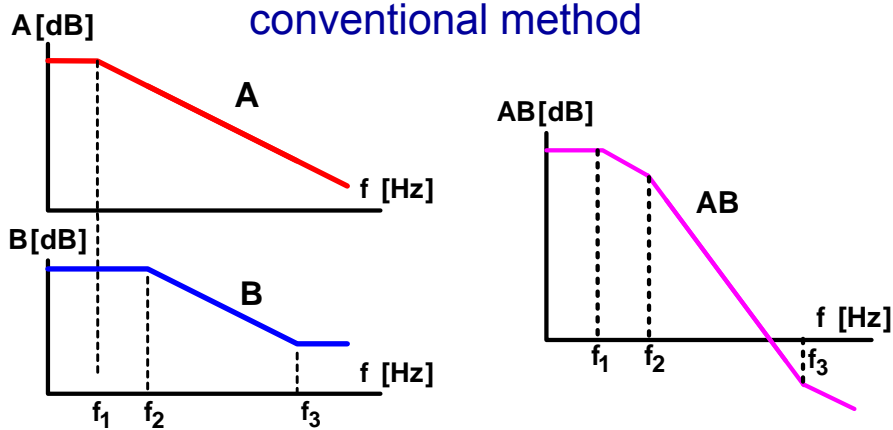


LoopGain test





Graphical representation of BA conventional method



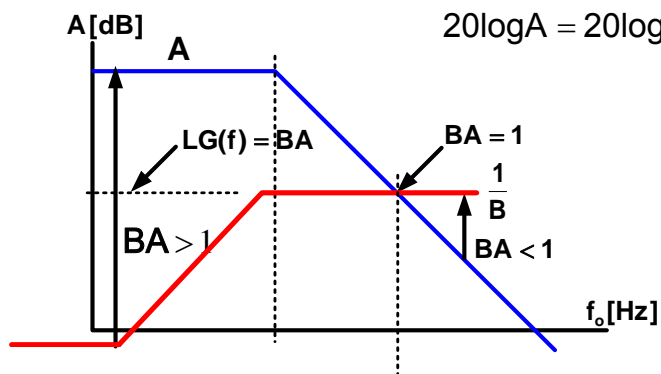
- Tedious – need to re-plot BA
- Analysis (not design) oriented
- Requires iterations



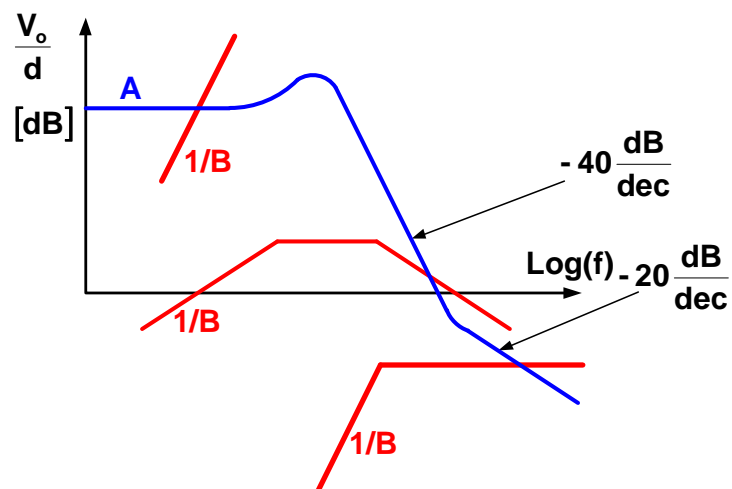
Graphical Representation of BA

$$20\log A - 20\log \frac{1}{B} = 20\log(BA)$$

$$20\log A = 20\log \frac{1}{B} \Rightarrow B \cdot A = 1$$

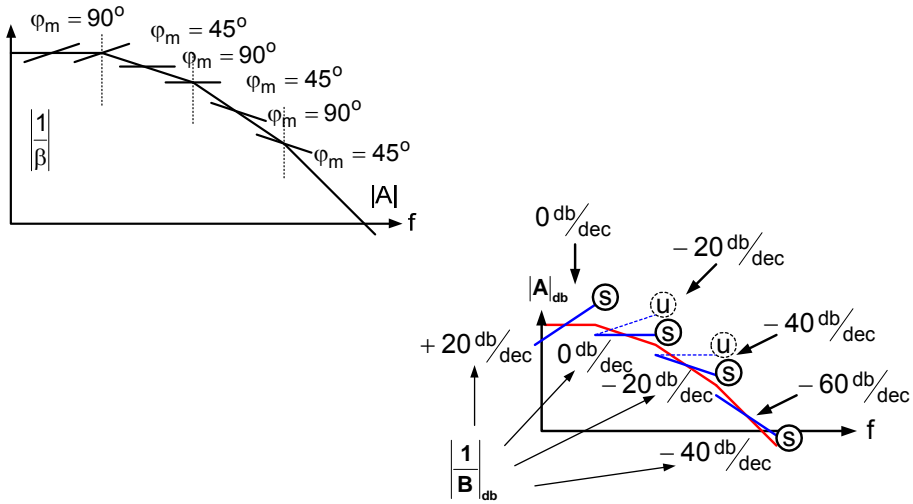


Possible compensations

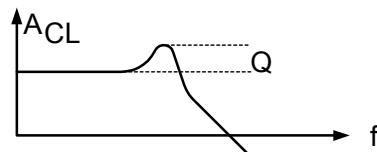
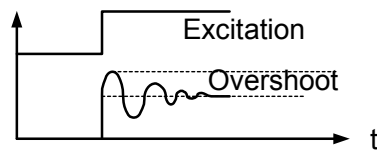




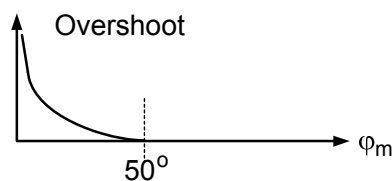
Possible compensations



Overshoot and Q in Closed Loop in Response to step in S_{in}



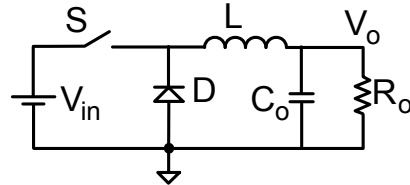
$$Q \cong \frac{\sqrt{\cos\phi_m}}{\sin\phi_m} \text{ for } \phi_m < 50^\circ$$



Design target $\phi_m \geq 45^\circ$



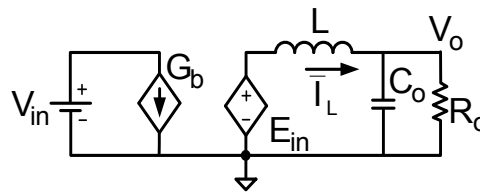
Extracting the power stage control-to-output transfer function



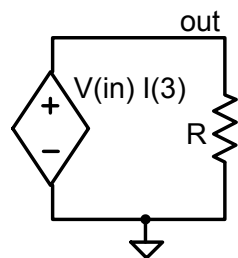
$$E_m = V_{in} \cdot D_{on}$$

$$G_b = \bar{I}_L \cdot D_{on}$$

$$E_{in} - V_o \rightarrow \bar{V}_L$$



Linearization



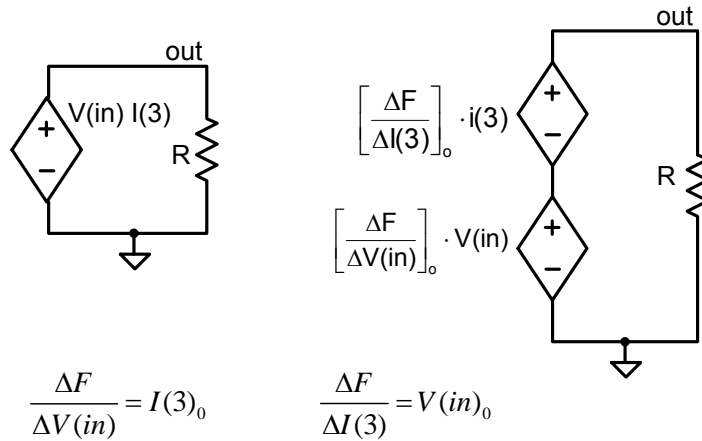
$$V(out) = V(in) * I(3)$$

$$d(V(out)) = \frac{\partial(V(out))}{\partial(V(in))} v(in) + \frac{\partial(V(out))}{\partial(I(3))} i(3)$$

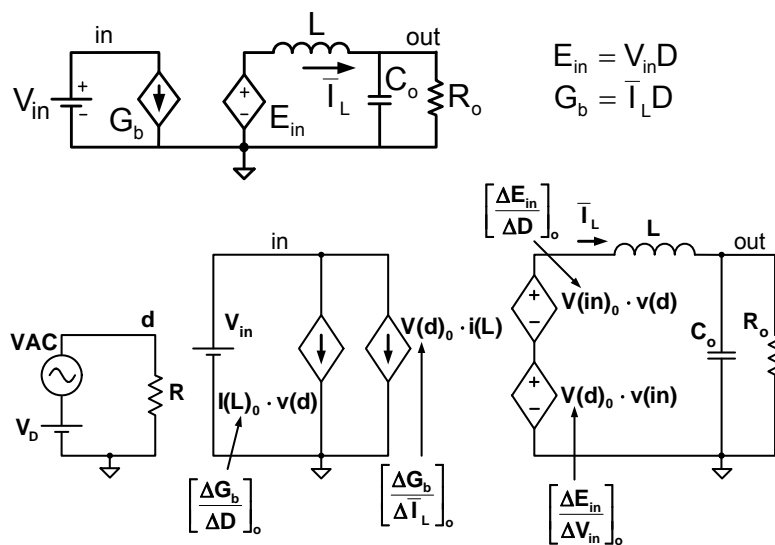
$$V(out) = \frac{\Delta V(out)}{\Delta V(in)} v(in) + \frac{\Delta V(out)}{\Delta I(3)} i(3)$$



SPICE Linearization (AC Analysis)



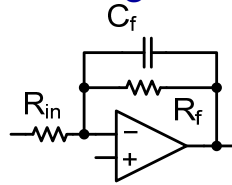
Buck linearization



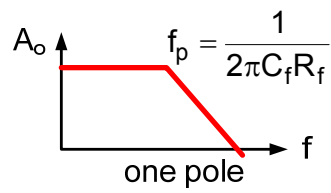


Possible phase compensation schemes

Lag network



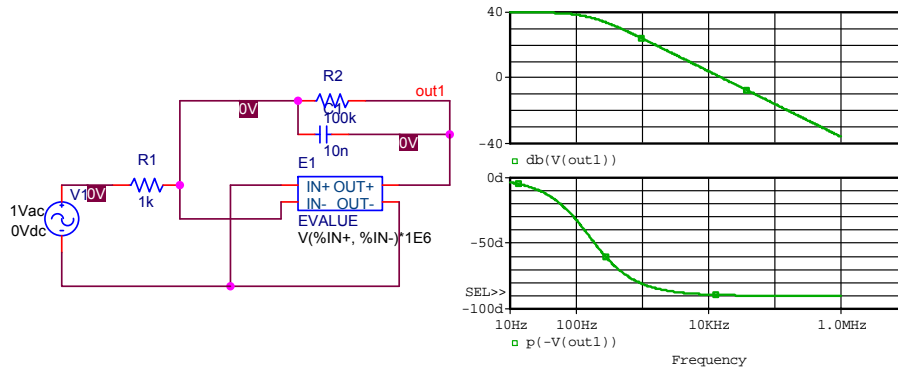
$$A_o = \frac{R_f}{R_{in}}$$



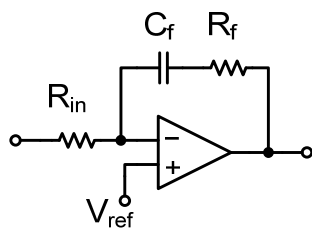
Design example



Lag network



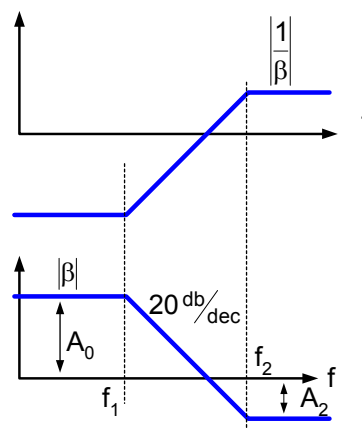
Lag – Lead network



$$A_o = A_{oL}(\text{ampl.})$$

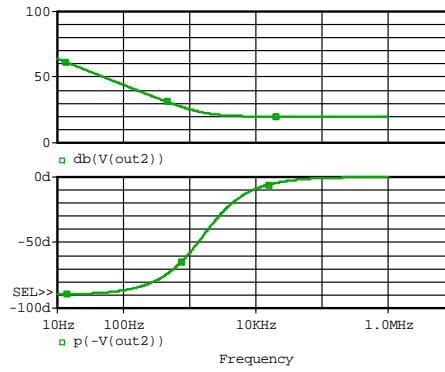
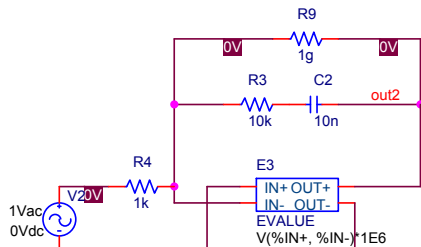
$$f_L = \frac{1}{2\pi C_f R_f}$$

$$A_2 = \frac{R_f}{R_{in}}$$

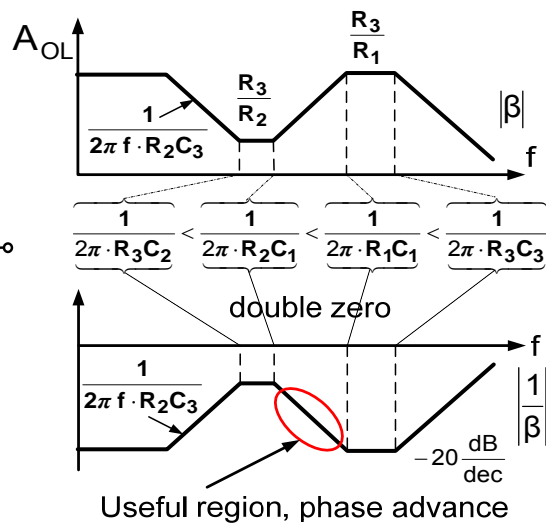
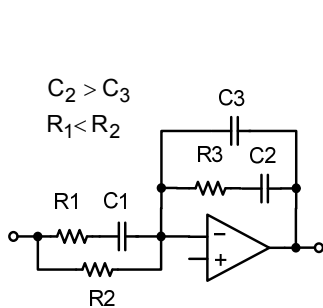




Lag-Lead network

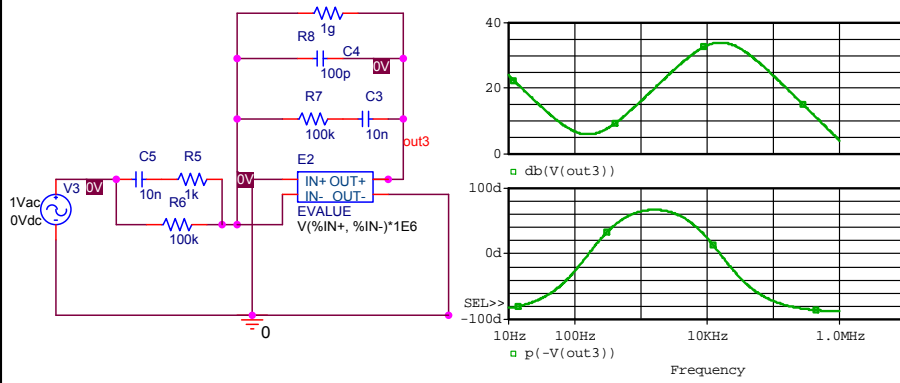


Double zero compensation scheme



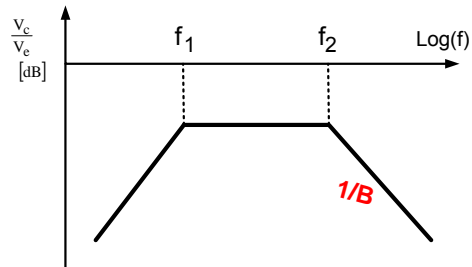
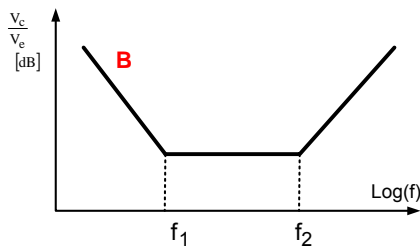


Double Zero



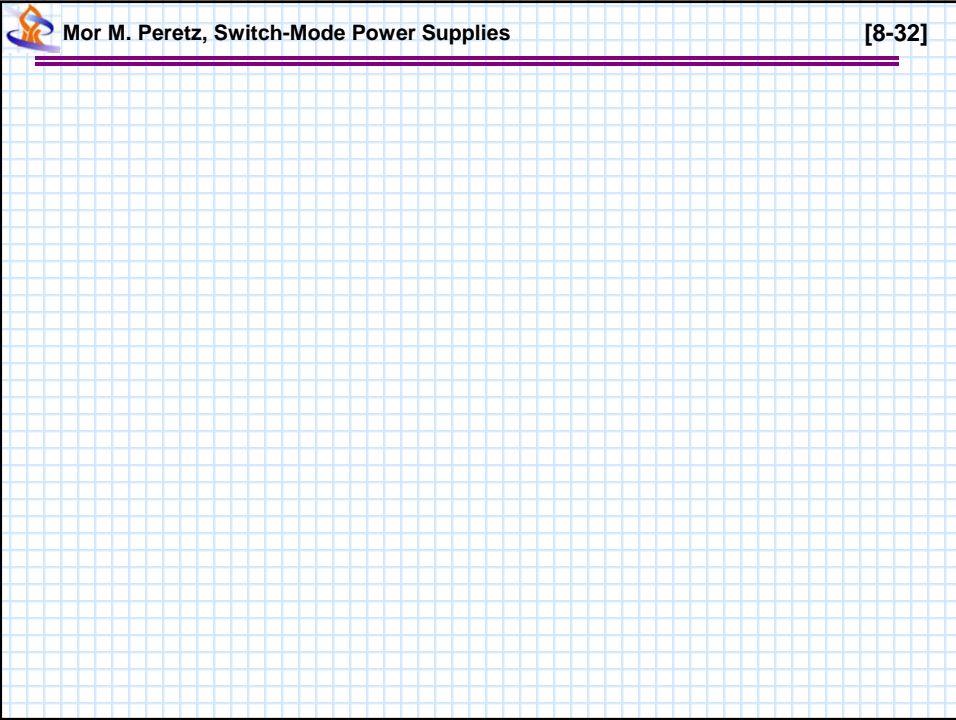
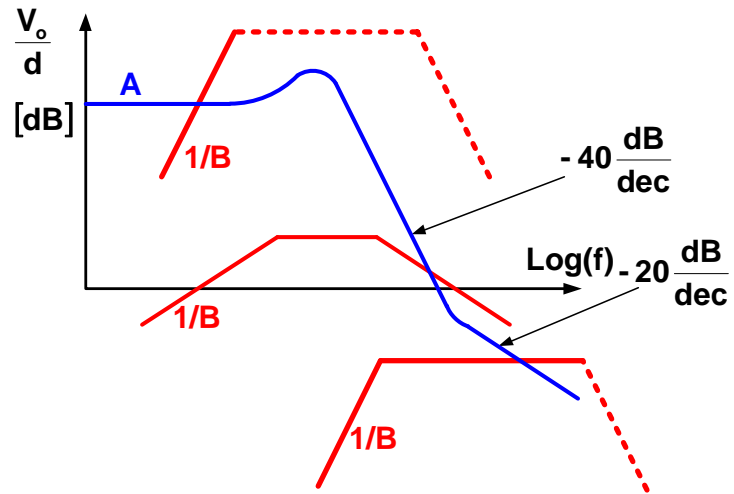
The relationship to PID compensators


$$\frac{v_c}{v_e} = K_p + \frac{K_I}{s} + s \cdot K_d = \frac{K_d}{K_I} \frac{(s + \omega_{z1}) \cdot (s + \omega_{z2})}{s}$$

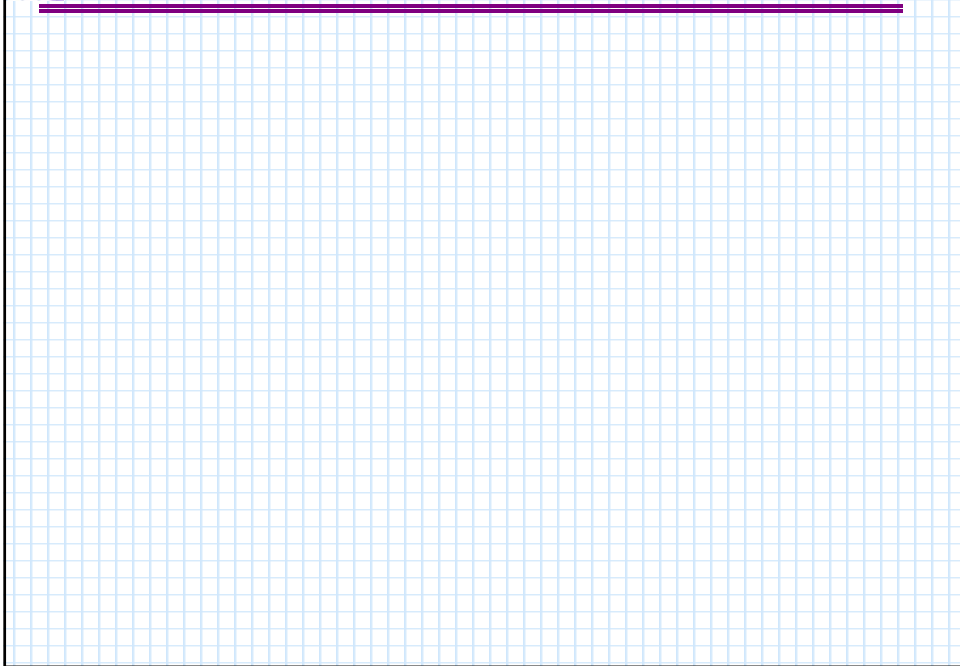





The relationship to PID compensators



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